CS44130

60 W Quad Half-Bridge Digital Amplifier Power Stage

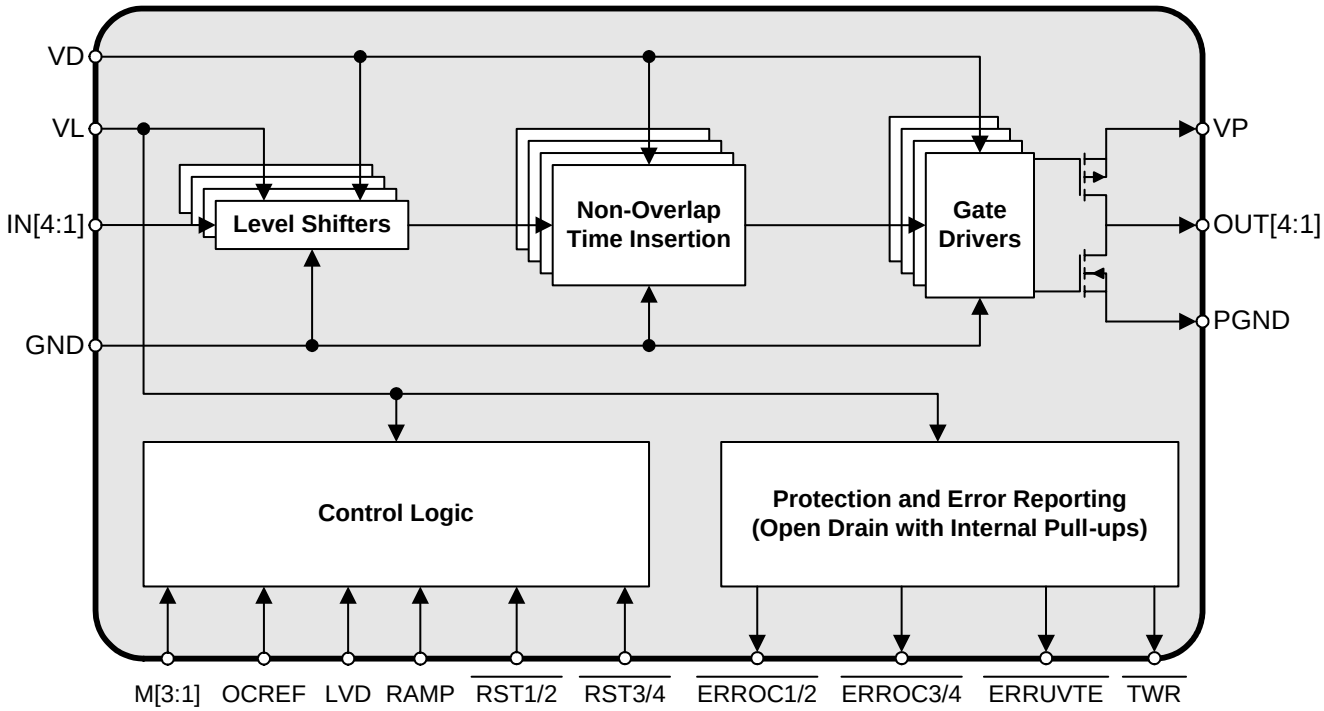
Features

- Configurable Outputs (10% THD+N)
  - 2 x 30 W into 8 Ω, Full-Bridge
  - 1 x 60 W into 4 Ω, Parallel Full-Bridge
  - 4 x 15 W into 4 Ω, Half-Bridge
  - 2 x 15 W into 4 Ω, Half-Bridge + 1 x 30 W into 8 Ω, Full-Bridge
- Space-Efficient, Thermally-Enhanced QFN Package
- PWM Popguard® Technology for Quiet Startup
- > 100 dB Dynamic Range - System Level
- < 0.12% THD+N @ 1 W - System Level
- Built-In Protection with Error Reporting
  - Over-Current
  - Thermal Warning
  - Thermal Fault
  - Under-Voltage
- Single (+10.8 V to +21 V) High Voltage Supply
- High Efficiency (90%)
- Low $R_{DS(ON)}$
- Low Quiescent Current
- Low Power Standby Mode

Common Applications

- Digital Televisions
- MP3 Docking Stations
- Mini Shelf Systems
- Networked Audio/POE Systems
- Desktop Speakers

General Description provided on page 2.



Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

General Description

The CS44130 is a high-efficiency power stage for digital Class-D amplifiers designed to recieve PWM signals from a modulator such as the CS44800/600. The power stage outputs can be configured as four half-bridge channels, two half-bridge channels and one full-bridge channel, two full-bridge channels, or one parallel full-bridge channel.

The CS44130 integrates on-chip protection for over-current, under-voltage, and over-temperature events. Addtionally, it integrates error reporting for these events, as well any thermal warning events. The low $R_{DS(ON)}$ of the outputs allows the part to operate at up to 90% efficiency. This efficiency provides for a smaller device package, no heat sink requirements, and smaller power supplies.

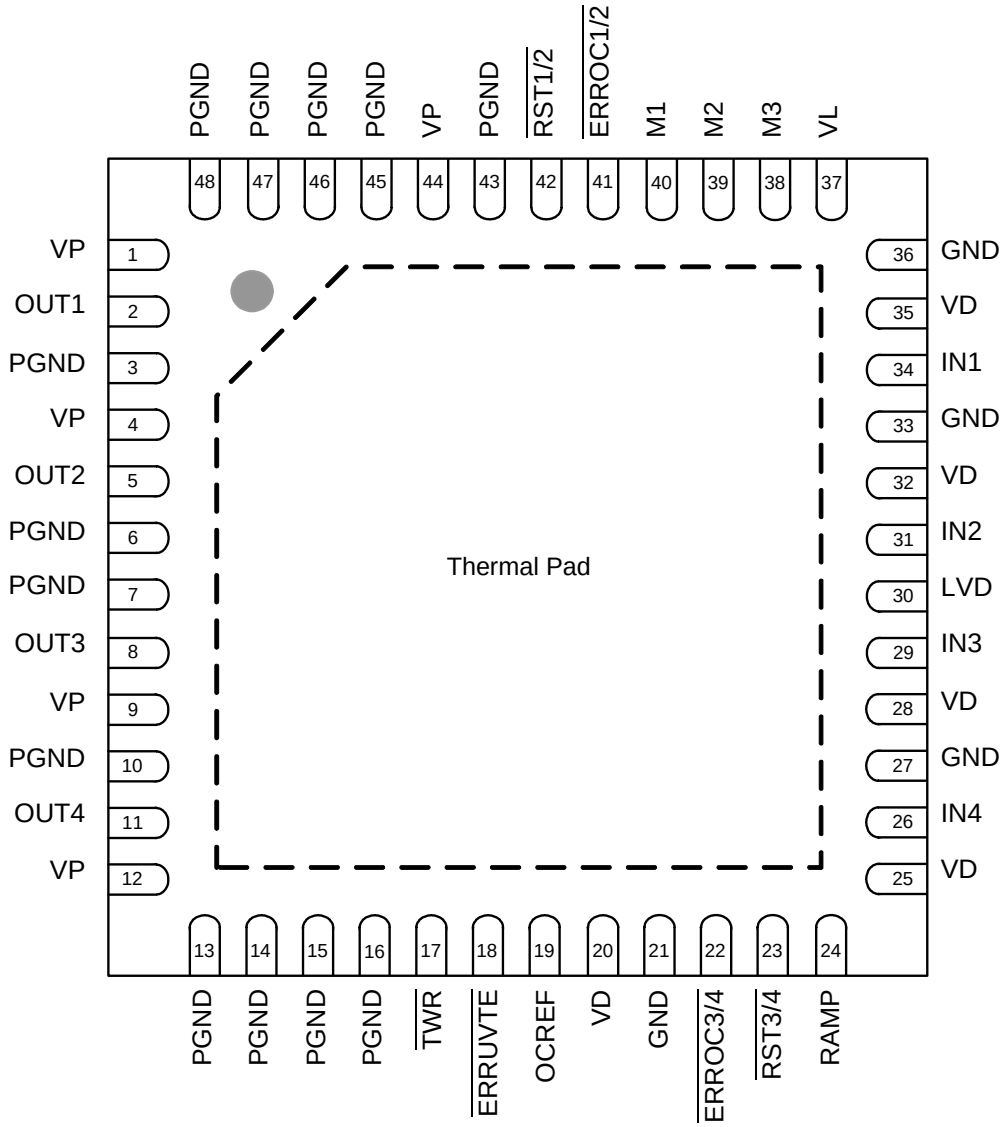
The CS44130 is available in a 48-pin QFN package for commercial grades (-10° to +70° C). The CRD44130-FB is also available for device evaluation and implementation suggestions. Please refer to “Ordering Information” on page 23 for complete ordering information.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. PIN DESCRIPTION



Pin Name	Pin #	Pin Description
VP	1 4 9 12 44	**High Voltage Output Power** (*Input*) - High voltage power supply for the individual output power half-bridge devices.
PGND	3, 6 7, 10 13, 14 15, 16 43, 45 46, 47 48	**Power Ground** (*Input*) - Ground for the individual output power half-bridge devices. These pins should be connected to the common system ground.

Pin Name	Pin #	Pin Description
VD	20, 25 28, 32 35	**Core Logic Power** (*Input*) - Low voltage power supply for internal logic.
VL	37	**Control Interface and PWM Input Power** (*Input*) - Supply for the I/O.
GND	21 27 33 36	**Ground** (*Input*) - Ground for the internal logic and I/O. These pins should be connected to the common system ground.
OUT1 OUT2 OUT3 OUT4	2 5 8 11	**PWM Output** (*Output*) - Amplified PWM power half-bridge outputs.
IN1 IN2 IN3 IN4	34 31 29 26	**PWM Input** (*Input*) - Inputs from a PWM modulator. These pins should not be left floating.
$\overline{\text{RST1/2}}$ $\overline{\text{RST3/4}}$	42 23	**Reset Input** (*Input*) - Reset inputs for channel 1, 2, 3, and 4; active low. These pins should not be left floating.
$\overline{\text{ERROC1/2}}$ $\overline{\text{ERROC3/4}}$	41 22	**Over-Current Error Output** (*Output*) - Over-current error flag for OUTx. Open drain with internal pull-up, active low. See Protection and Error Reporting on page 18 for details.
$\overline{\text{ERRUVTE}}$	18	**Thermal and Under-Voltage Error Output** (*Output*) - Error flag for thermal shutdown and under-voltage. Open drain with internal pull-up, active low. See Protection and Error Reporting on page 18 for details.
$\overline{\text{TWR}}$	17	**Thermal Warning Output** (*Output*) - Thermal warning output. Open drain with internal pull-up, active low. See Protection and Error Reporting on page 18 for details.
LVD	30	**Input Voltage Level Select** (*Output*) - Input voltage indicator of VD. A high level indicates VD is set to 5.0 V. A low level indicates VD is set to 3.3 V. This pins should not be left floating.
M1 M2 M3	40 39 38	**Mode Select** (*Input*) - Used to set the operating mode. See Output Mode Configuration on page 15 for details. These pins should not be left floating.
OCREF	19	**Over-Current Reference** (*Input*) - Over-current trip level setting. This pin should be connected through a 60 kΩ resistor to GND. See Protection and Error Reporting on page 18 for details. This pins should not be left floating.
RAMP	24	**Ramp-Up/Down Select** (*Input*) - When set high, ramping is enabled. When set low, ramping is disabled. See PWM Popguard Transient Control on page 19 for details. This pin should not be left floating. Ramp should only be used in half bridge mode or in full bridge configuration modes 010 and 011.

1.1 I/O Pin Characteristics

Signal Name	Power Rail	I/O	Driver	Receiver
OUT1	VP	Output	10.8 V-21.0 V Power MOSFET	-
OUT2	VP	Output	10.8 V-21.0 V Power MOSFET	-
OUT3	VP	Output	10.8 V-21.0 V Power MOSFET	-
OUT4	VP	Output	10.8 V-21.0 V Power MOSFET	-
IN1	VL	Input	-	2.5 V to 5.0 V Compatible.
IN2	VL	Input	-	2.5 V to 5.0 V Compatible.
IN3	VL	Input	-	2.5 V to 5.0 V Compatible.
IN4	VL	Input	-	2.5 V to 5.0 V Compatible.
$\overline{\text{RST1/2}}$	VL	Input	-	2.5 V to 5.0 V Compatible.
$\overline{\text{RST3/4}}$	VL	Input	-	2.5 V to 5.0 V Compatible.
$\overline{\text{ERROC1/2}}$	VL	Output	Open Drain, Internal pull-up	-
$\overline{\text{ERROC3/4}}$	VL	Output	Open Drain, Internal pull-up	-
$\overline{\text{ERRUVTE}}$	VL	Output	Open Drain, Internal pull-up	-
$\overline{\text{TWR}}$	VL	Output	Open Drain, Internal pull-up	-
LVD	VL	Input	-	2.5 V to 5.0 V Compatible.
RAMP	VL	Input	-	2.5 V to 5.0 V Compatible.
M1	VL	Input	-	2.5 V to 5.0 V Compatible.
M2	VL	Input	-	2.5 V to 5.0 V Compatible.
M3	VL	Input	-	2.5 V to 5.0 V Compatible.

All input pins should be connected and not left floating.

2. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND/PGND = 0 V, all voltages with respect to ground, unless otherwise specified)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supply						
PWM Outputs	Power Stage Supply	VP	10.8	-	21.0	V
Core Logic	3.3 V 5.0 V	VD	3.14 4.75	3.3 5.0	3.47 5.25	V V
Control Interface and PWM Inputs	2.5 V 3.3 V 5.0 V	VL	2.37 3.14 4.75	2.5 3.3 5.0	2.63 3.47 5.25	V V V
Ambient Operating Temperature						
Commercial	-CNZ	T_A	-10	-	+70	°C
Junction Temperature		T_J		-	+150	°C

ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

(GND/PGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	PWM Outputs Core Logic Control Interface and PWM Inputs	VP VD VL	-0.3 -0.3 -0.3	23.0 7.0 7.0	V V V
Input Current	(Note 1)	I_{in}	-	±10	mA
Digital Input Voltage	(Note 2)	V_{IN}	-0.4	VL+0.4	V
Ambient Operating Temperature	Commercial	T_A	-20	+85	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes:

1. Any pin except supplies. Transient currents of up to ±100 mA on the input pins will not cause SCR latch-up.
2. The maximum over/under-voltage is limited by the input current.

DC ELECTRICAL CHARACTERISTICS

(GND/PGND = 0 V, all voltages with respect to ground; PWM Switch Rate = 384 kHz unless otherwise specified. VD = 3.3 V and VL = 3.3 V, unless otherwise specified.)

Parameter		Symbol	Min	Typ	Max	Units
Normal Operation (Note 3)						
Power Supply Current (Note 4)	VL = 2.5 V	I_L	-	0.29	-	
	VL = 3.3 V	I_L	-	0.01	-	
	VL = 5.0 V	I_L	-	2.29	-	mA
	VD = 3.3 V	I_D	-	1.60	-	
	VD = 5.0 V	I_D	-	2.00	-	
Power Dissipation ($P_{total} = P_{dl} + P_{dd}$)	VL = 2.5 V	P_{dl}	-	6.00	-	
	VL = 3.3 V	P_{dl}	-	5.30	-	
	VL = 5.0 V	P_{dl}	-	16.73	-	mW
	VD = 3.3 V	P_{dd}	-	5.30	-	
	VD = 5.0 V	P_{dd}	-	10.00	-	
Power-Down Mode (Note 5)						
Power Supply Current	VL = 2.5 V	I_L	-	17.10	-	µA
	VL = 3.3 V	I_L	-	16.80	-	µA
	VL = 5.0 V	I_L	-	16.40	-	µA
	VD = 3.3 V	I_D	-	1.30	-	nA
	VD = 5.0 V	I_D	-	1.50	-	nA

3. Normal operation is defined with $\overline{\text{RSTx/y}}$ = HI.
4. Current consumption increases with increasing PWM switch rates.
5. Power-Down Mode is defined as $\overline{\text{RSTx/y}}$ = LOW with all input lines held low.

PWM OUTPUT CHARACTERISTICS

(Unless otherwise noted: GND/PGND = 0 V, all voltages with respect to ground, VP = 21 V, R_L = 8 Ω in Full-Bridge Mode, R_L = 4 Ω in Half-Bridge Mode, PWM Switch Rate = 384 kHz, Modulation Index = 0.88; Measurement bandwidth is 10 Hz to 20 kHz; Performance measurements taken with a full scale 997 Hz and AES17 filter.)

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Power Output per Channel						
Half-Bridge		THD+N =10%	-	15	-	
		THD+N =1%	-	11	-	
Full-Bridge	P_O	THD+N = 10%	-	30	-	W
		THD+N = 1%	-	20	-	
Parallel Full-Bridge		THD+N = 10%	-	60	-	
		THD+N = 1%	-	40	-	
Total Harmonic Distortion + Noise						
Half-Bridge		P_O = 1 W	-	.20	-	
		P_O =7.8 W (0 dBFS)	-	.35	-	
Full-Bridge	THD+N	P_O = 1 W	-	.12	-	%
		P_O = 15.9 W (0 dBFS)	-	.19	-	
Parallel Full-Bridge		P_O = 1 W	-	.14	-	
		P_O = 30.8 W (0 dBFS)	-	.29	-	
Dynamic Range						
Half-Bridge		P_O = -60 dBFS, A-Weighted	-	102	-	
		P_O = -60 dBFS, Unweighted	-	99	-	
Full-Bridge	DR	P_O = -60 dBFS, A-Weighted	-	107	-	
		P_O = -60 dBFS, Unweighted	-	105	-	dB
Parallel Full-Bridge		P_O = -60 dBFS, A-Weighted	-	102	-	
		P_O = -60 dBFS, Unweighted	-	99	-	
MOSFET On Resistance	$R_{DS(ON)}$	I_d = 1 A, T_A = 25°C	-	450	550	mΩ
Efficiency (Full Bridge)	h	0 dBFS P_O = 2 x 24 W	-	90	-	%
Minimum Output Pulse Width	PW_{min}	No Load	-	60	-	ns
Rise Time of OUTx	t_r	Resistive Load	-	20	-	ns
Fall Time of OUTx	t_f	Resistive Load	-	20	-	ns
Junction Thermal Warning Trip Point	T_{TW}		-	125	-	°C
Junction Overtemperature Trip Point	T_{OT}		-	150	-	°C
VP Under-voltage Trip Point	V_{UV}	T_A = 25°C	-	6	-	V
Ramp Up Time (Half-Bridge Mode)	T_{RU}	DC Blocking Cap = 1000 µF	-	1.5	-	s
Ramp Down Time (Half-Bridge Mode)	T_{RD}	DC Blocking Cap = 1000 µF	-	50	-	s

DIGITAL INTERFACE CHARACTERISTICS

(GND/PGND = 0 V, all voltages with respect to ground)

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VL)	V_{IL}	-	-	30%	V
Low-Level Output Voltage at I_o=2 mA	(% of VL)	V_{OL}	-	-	20%	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	-	8	pF

3. TYPICAL CONNECTION DIAGRAMS

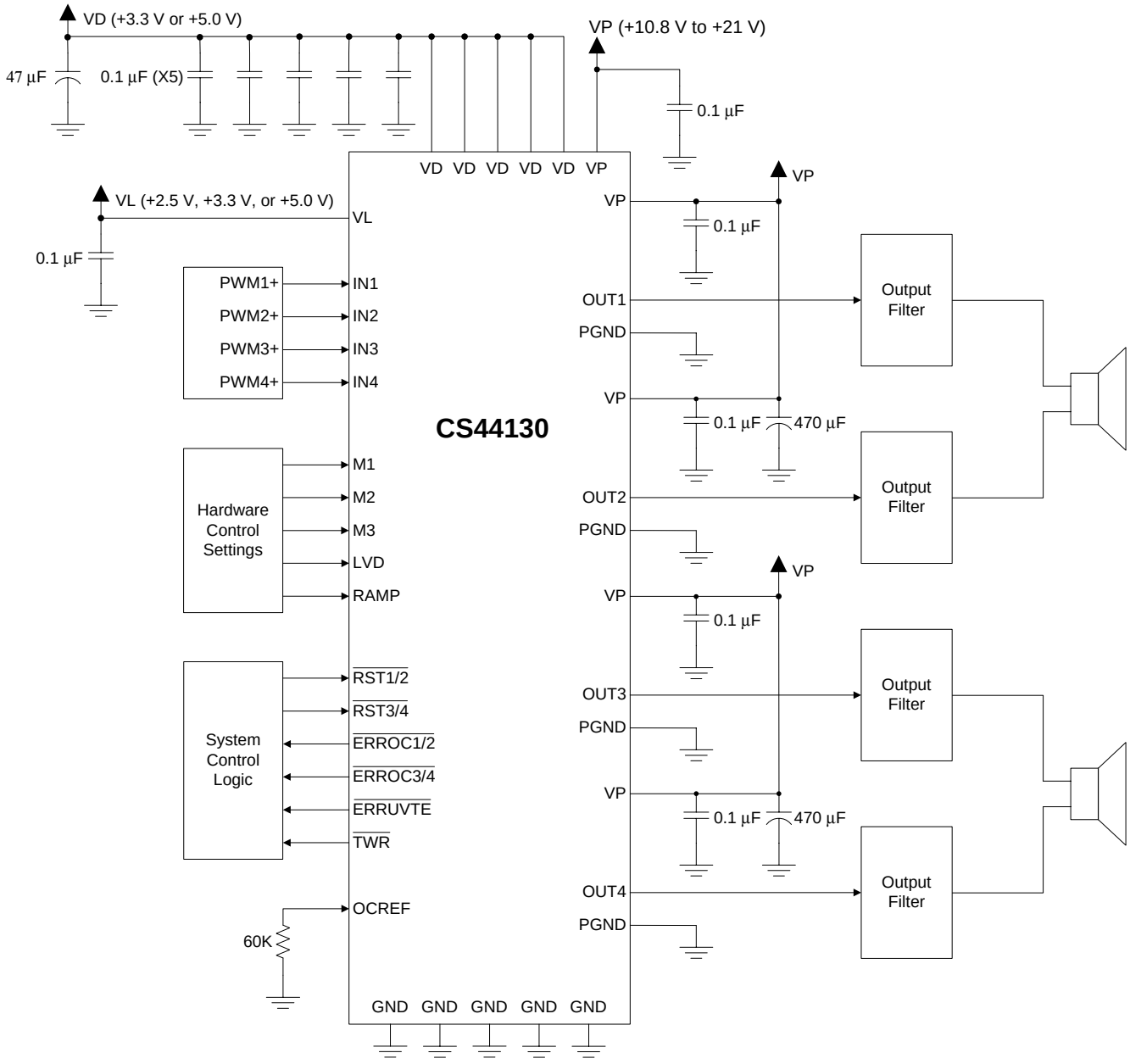


Figure 1. Typical Connection Diagram - Stereo Full-Bridge

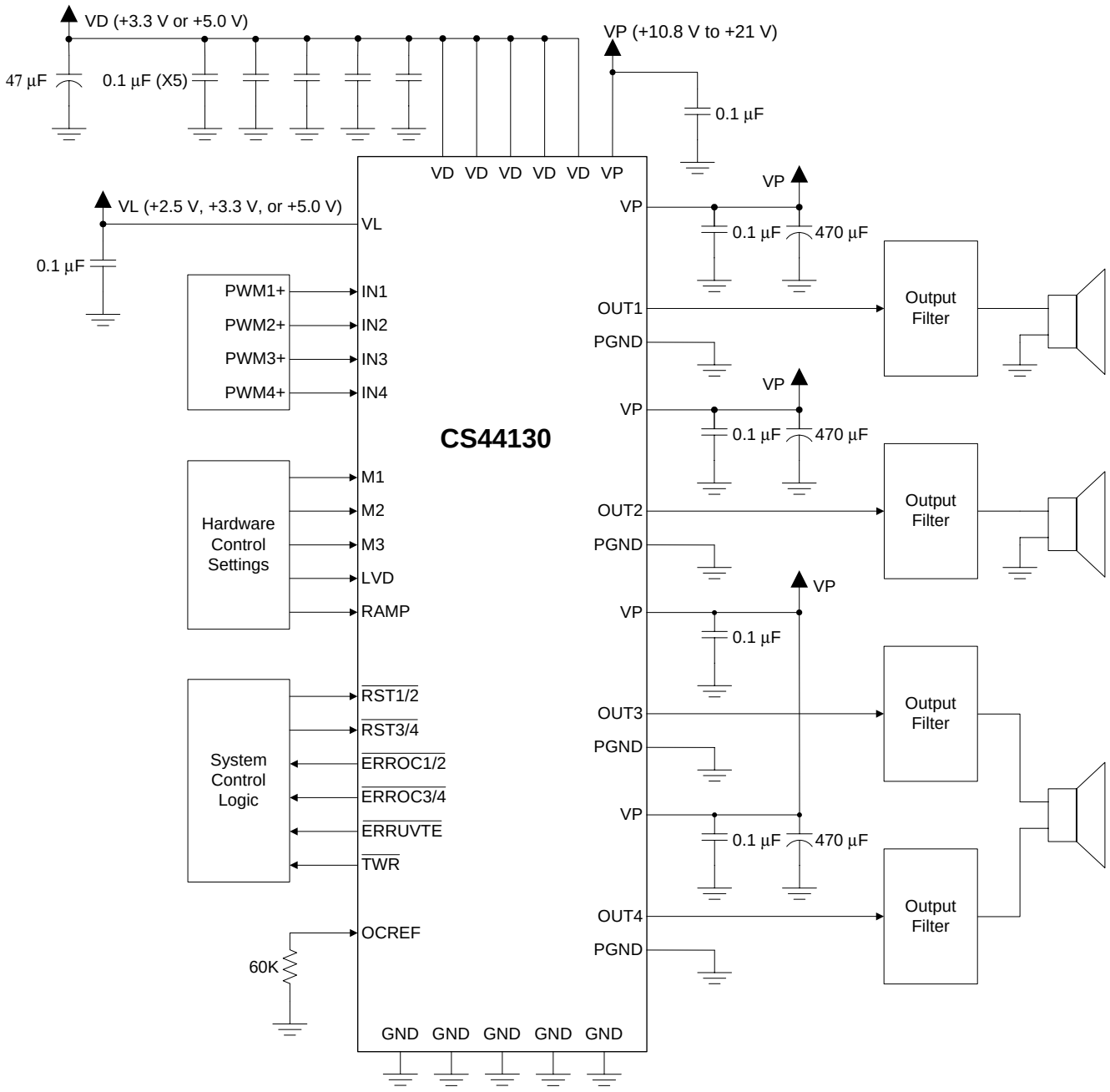


Figure 2. Typical Connection Diagram - 2.1 Channels (2 x Half-Bridge + 1 x Full-Bridge)

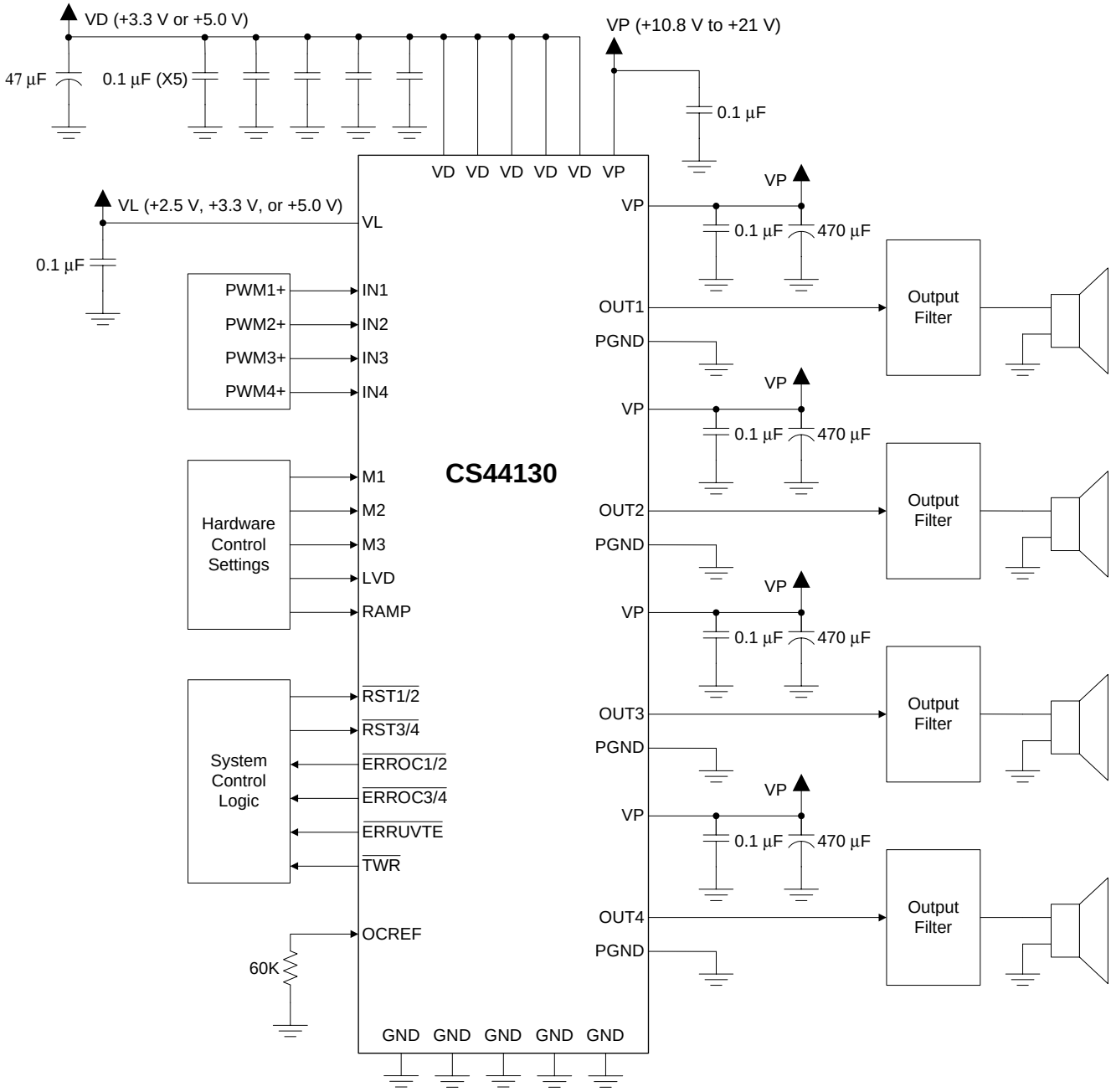


Figure 3. Typical Connection Diagram - 4-Channel Half-Bridge

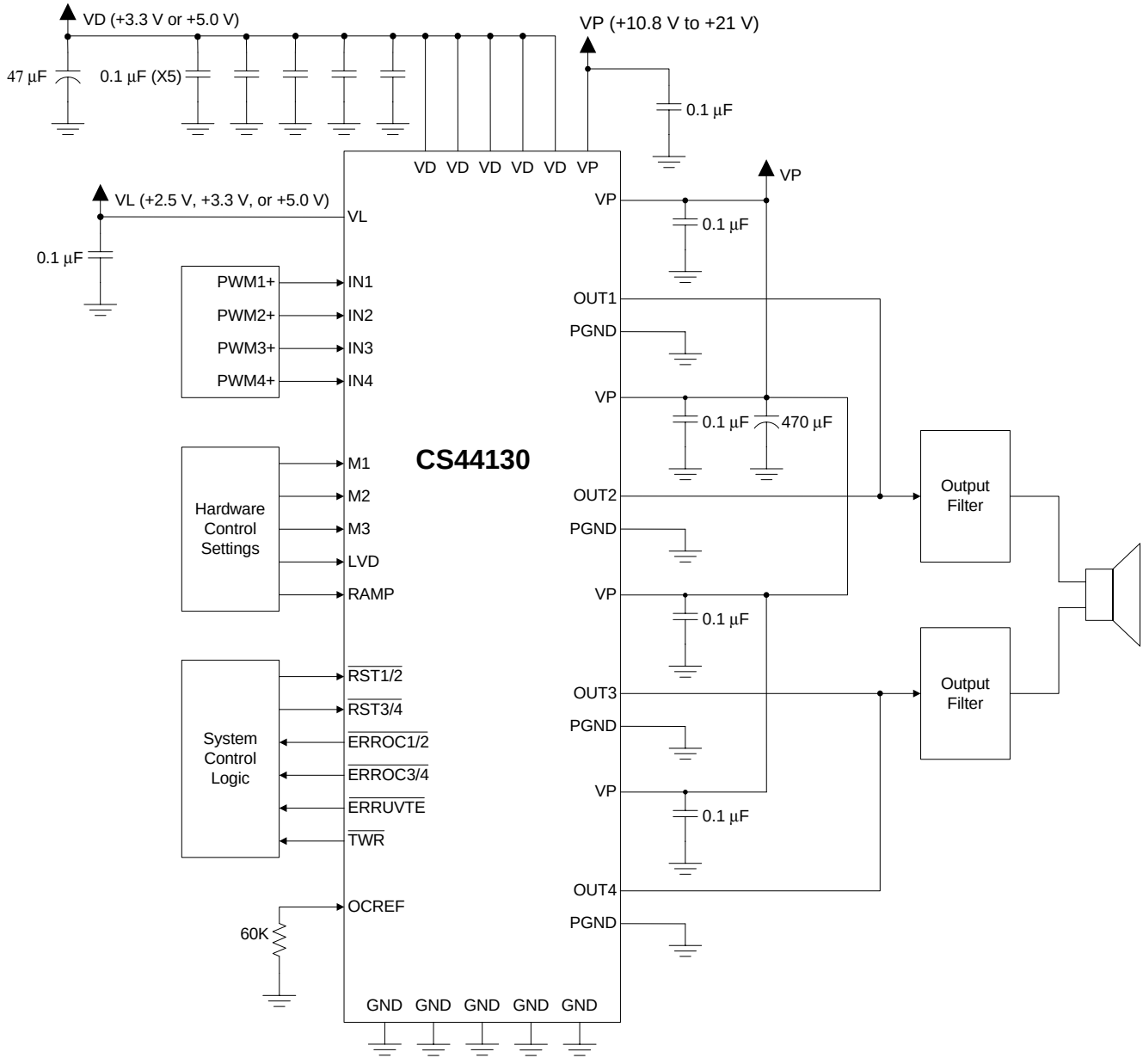


Figure 4. Typical Connection Diagram - Mono Parallel Full-Bridge

4. APPLICATIONS

4.1 Overview

The CS44130 is a high-efficiency power stage for digital Class-D amplifiers. It has been designed to be configured as four half-bridge channels, two half-bridge channels and one full-bridge channel, two full-bridge channels, or one parallel full-bridge channel.

The CS44130 integrates on-chip protection for over-current, under-voltage, and over-temperature events. Addtionally, it integrates error reporting for these events, as well any thermal warning events. The low $R_{DS(ON)}$ of the outputs allows the part to operate at up to 90% efficiency. This efficiency provides for a smaller device package, no heat sink requirements, and smaller power supplies.

The CS44130 is ideal for digital audio systems requiring space-efficient, high quality audio, such as Digital Televisions, MP3 Docking Stations, Mini Shelf Systems, and Desktop Speakers.

4.2 Feature Set Summary

- VD voltage pins for internal core logic levels between 3.3 V and 5.0 V.
- VL voltage pin for PWM input, mode configuration, and error reporting logic levels between 2.5 V and 5.0 V.
- VP voltage pin for PWM output levels between +10.8 V and +21 V.
- Protection and Error Reporting for Over-current, Under-voltage, and Thermal Overload Protection events.
- PWM Popguard for Quiet Startup (valid for Half Bridge configurations only.)

4.3 Output Mode Configuration

The CS44130 can be configured for several modes of operation. Table 1 shows the setting of the M[3:1] inputs and the corresponding mode of operation. These pins should remain static during operation (RSTx/y set high).

M3	M2	M1	Output Mode	Description
0	0	0	Auto-Reset	When an error condition occurs on a channel, that channel is auto-reset until the error condition is removed. IN1 must be inverted from IN2 for full-bridge operation. IN3 must be inverted from IN4 for full-bridge operation.
0	0	1	Latched Shutdown	When an error condition occurs on a channel, that channel is shutdown until the error condition is removed and the channel reset is toggled. IN1 must be inverted from IN2 for full-bridge operation. IN3 must be inverted from IN4 for full-bridge operation.
0	1	0	Auto-Reset with Inversion	This mode should only be used for full-bridge applications. When an error condition occurs on a channel, that channel is auto-reset until the error condition is removed. IN2 is internally inverted for the second half-bridge.[1] IN4 is internally inverted for the second half-bridge.[1]
0	1	1	Latched Shutdown with Inversion	This mode should only be used for full-bridge applications. When an error condition occurs on a channel, that channel is shutdown until the error condition is removed and the channel reset is toggled. IN2 is internally inverted for the second half-bridge.[1] IN4 is internally inverted for the second half-bridge.[1]
1	x	x	Reserved	This setting is reserved and should not be used.

Table 1. Output Mode Configuration Options

1. In modes 010 and 011, IN1 should be connected to IN2 (external to the chip) and driven with a single PWM signal. Likewise, in these same modes, IN3 should be connected to IN4 (external to the chip) and driven with a single PWM signal.

4.4 Output Filter

The RC filter placed after the PWM outputs can greatly affect the output performance. The filter not only reduces radiated EMI (snubber filter) but also filters high-frequency content from the switching output before going to the speaker (low-pass filter).

4.4.1 Half-Bridge Output Filter

Figure 5 shows the output filter for a half-bridge configuration. The transient-voltage suppression circuit, (snubber circuit) is comprised of a resistor (5.6 Ω, 1/8 W) and capacitor (560 pF) and should be placed as close as possible to the corresponding PWM output pin. This will greatly reduce radiated EMI.

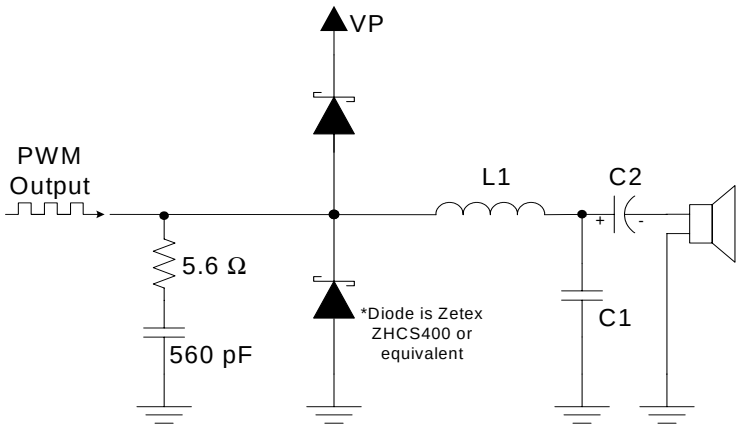


Figure 5. Output Filter - Half-Bridge

The inductor, L1, and capacitor, C1, comprise the low-pass filter. Along with the nominal load impedance of the speaker, these values set the cutoff frequency of the filter. Table 2 shows the component values for L1 and C1 based on nominal speaker (load) impedance for a corner frequency (-3 dB point) of approximately 35 kHz.

Load	L1	C1
4 Ω	22 µH	1.0 µF
6 Ω	33 µH	0.68 µF
8 Ω	47 µH	0.47 µF

Table 2. Low-Pass Filter Components - Half-Bridge

C2 is the DC-blocking capacitor. Table 3 shows the component values for C2 based corner frequency (-3 dB point) and a nominal speaker (load) impedance of 4 Ω. This capacitor should also be chosen to have a ripple current rating above the amount of current that will pass through it.

Corner Frequency	C2
36 Hz	1000 µF
54 Hz	680 µF
110 Hz	330 µF

Table 3. DC-Blocking Capacitors Values - Half-Bridge

4.4.2 Full-Bridge Output Filter (Stereo or Parallel)

Figure 6 shows the output filter for a full-bridge configuration. The snubber resistor (20 Ω, 1/10 W) and capacitor (330 pF), as well as the diodes, should be placed as close as possible to the corresponding PWM output pins. This will greatly reduce radiated EMI. The inductors, L1 and L2, and capacitor, C1, comprise the low-pass filter. Along with the nominal load impedance of the speaker, these values set the cutoff frequency of the filter. Table 4 shows the component values based on nominal speaker (load) impedance for a corner frequency (-3 dB point) of approximately 35 kHz.

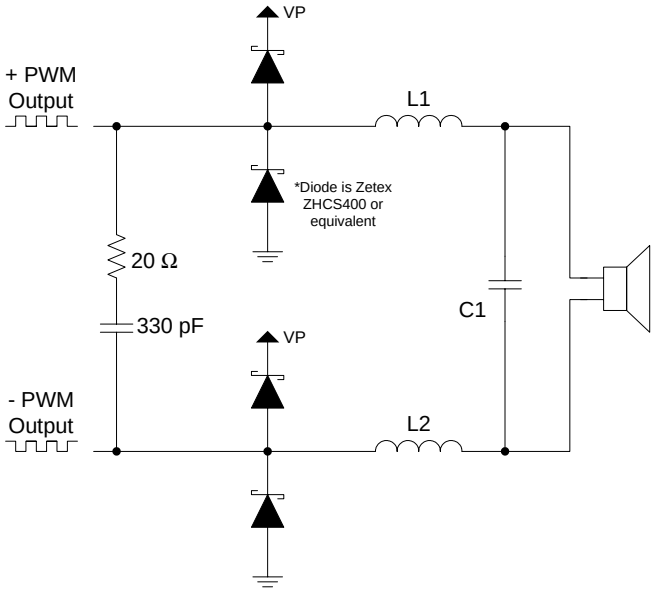


Figure 6. Output Filter - Full-Bridge

Load	L1 & L2	C1
4 Ω	10 µH	1.0 µF
6 Ω	15 µH	0.47 µF
8 Ω	22 µH	0.47 µF

Table 4. Low-Pass Filter Components - Full-Bridge

4.5 Protection and Error Reporting

The CS44130 has built-in protection circuitry for over-current, under-voltage, and thermal warning/overload conditions. All error outputs are open-drain, active low, and can safely be tied together in any combination. These pins also have internal pull-up resistors, alleviating the need for external resistors.

4.5.1 Over-Current Protection

Over-current errors are reported on the $\overline{\text{ERROCx/y}}$ pins (example: over-current error on OUT1 would be reported on $\overline{\text{ERROC1/2}}$). The over-current error is designed to go low for conditions that could potentially damage the part. In order for $\overline{\text{ERROCx/y}}$ to go low only under conditions that could damage the part, it is recommended that a 60 kΩ resistor be connected from the OCREF pin to ground. If the part has been configured for latched shutdown, as specified in Table 1 on page 15, the channel which is reporting the over-current condition will be shut down (OUTx set to HI-Z) until the error condition has been removed and the $\overline{\text{RSTx/y}}$ for that channel has been cycled from low to high.

If the part has been configured for auto-reset, as specified in Table 1 on page 15, the channel which is reporting the over-current condition will be shut down (OUTx set to HI-Z). After approximately 85 milliseconds, the part will try to re-enable the outputs. If the fault has been cleared, the unit will return to normal operation. If the fault is still present, the outputs will remain disabled and the part will try again in approximately 85 milliseconds. After 5 unsuccessful attempts, the outputs will latch in the off (OUTx set to HI-Z) condition and wait for $\overline{\text{RSTx/y}}$ to be reset.

$\overline{\text{ERROCx/y}}$	Error Condition
0	Over-current error on channel x or channel y
1	Normal operation

Table 5. Over-Current Error Conditions

4.5.2 Under-Voltage and Thermal Protection

Table 6 shows the behavior of the $\overline{\text{TWR}}$ and $\overline{\text{ERRUVTE}}$ pins. When the junction temperature exceeds the Junction Thermal Warning Trip Point (T_{TW}, as specified in the "PWM Output Characteristics" on page 9), the $\overline{\text{TWR}}$ pin will be set low. If the junction temperature continues to increase beyond the Junction Over-temperature Trip Point (T_{OT}, as specified in the "PWM Output Characteristics" on page 9), the $\overline{\text{ERRUVTE}}$ pin will be set low. If the voltage on VP falls below the VP Under-voltage Trip Point (V_{UV}, as specified in the "PWM Output Characteristics" on page 9), $\overline{\text{ERRUVTE}}$ will be set low.

If the part has been configured for auto-reset, as specified in Table 1 on page 15, the channel which is reporting the over-current condition will be shut down (OUTx set to HI-Z). After approximately 85 milliseconds, the part will try to re-enable the outputs. If the fault has been cleared, the unit will return to normal operation. If the fault is still present, the outputs will remain disabled and the part will try again in approximately 85 milliseconds. After 5 unsuccessful attempts, the outputs will latch in the off (OUTx set to HI-Z) condition and wait for $\overline{\text{RSTx/y}}$ to be reset.

$\overline{\text{TWR}}$	$\overline{\text{ERRUVTE}}$	Error Condition
0	0	Thermal warning and thermal error and/or under-voltage error.
0	1	Thermal warning only.
1	0	Under-voltage error.
1	1	Normal operation.

Table 6. Thermal and Under-Voltage Error Conditions

5. RESET AND POWER-UP

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks, and configuration pins are stable. It is also recommended that the $\overline{\text{RSTx/y}}$ pin be activated if the voltage supplies drop below the recommended operating condition to prevent power-glitch- related issues.

When $\overline{\text{RSTx/y}}$ is low, the corresponding channels of the CS44130 enter a low-power mode and all internal states are reset and the outputs are set to HI-Z. When $\overline{\text{RSTx/y}}$ is high, the desired mode settings will be loaded and the outputs will begin normal operation.

5.1 PWM Popguard Transient Control

The CS44130 uses Popguard® technology to minimize the effects of output transients during power-up and power-down for half-bridge configurations. This technique reduces the audio transients commonly produced by half-bridge, single-supply amplifiers when implemented with external DC-blocking capacitors connected in series with the audio outputs.

When the device is configured for ramping (RAMP set high) and $\overline{\text{RSTx/y}}$ is set high and the inputs are pulsed, the OUTx output will ramp-up to the bias point (VP/2). This gradual voltage ramping allows time for the external DC-blocking capacitor to charge to the quiescent voltage, minimizing the power-up transient. The OUTx output will not begin normal operation until the ramp has reached the bias point. The INx input must begin switching before the ramp cycle begins.

When the device is configured for ramping (RAMP set high) and $\overline{\text{RSTx/y}}$ is set low, the OUTx output will begin to slowly ramp down from the bias point to PGND, allowing the DC-blocking capacitor to discharge.

It is not necessary to complete a ramp up/down sequence before ramping up/down again. PWM Popguard should only be used in Half Bridge configurations.

5.2 Recommended Power-Up Sequence

1. Turn on the system power.
2. Hold $\overline{\text{RSTx/y}}$ low until the power supply and system clocks are stable. In this state, all associated outputs are HI-Z.
3. Start the PWM modulator output.
4. Once the PWM modulator output is valid, release $\overline{\text{RSTx/y}}$ high. If the CS44130 is configured for ramping, the outputs will ramp to the bias point and then begin switching normally. If the CS44130 is not configured for ramping, the outputs will begin switching after approximately 35 cycles of the PWM input signal.

5.3 Recommended Power-Down Sequence

1. Set $\overline{\text{RSTx/y}}$ low. If the CS44130 is configured for ramping, the outputs will ramp down to PGND and then become HI-Z. If the CS44130 is not configured for ramping, the outputs will immediately become HI-Z.
2. Power-down the remainder of the system.
3. Turn off the system power.

6. POWER SUPPLY, GROUNDING, AND PCB LAYOUT

The CS44130 requires a 3.3 V or 5.0 V digital power supply for the core logic. In order to support a number of PWM frontend solutions, a separate VL power pin is provided to condition the interface signals to support up to 5.0 V levels. The VL power pins control the voltage levels for all PWM input, mode, and error reporting signals.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. It is necessary to decouple the power supply by placing capacitors directly between the power and ground of the CS44130. The recommended procedure is to place a 0.1 µF capacitor as close as physically possible to each power pin. Decoupling capacitors should be as near to the pins of the CS44130 as possible, with the low value ceramic capacitor being the nearest and should be mounted on the same side of the board as the CS44130 to minimize inductance effects

7. PARAMETER DEFINITIONS

Dynamic Range (DR)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth, typically 20 Hz to 20 kHz. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full-scale, with units in dBFS. This measurement can be made “weighted” or “unweighted”. The weighting that was used during for the test is usually indicated by a letter following the units. For instance, “dBFS A” would indicate that an A-weighted filter was used during testing.

This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Frequency Response (FR)

FR is the deviation in signal level versus frequency. The 0 dB reference point is 1 kHz. The amplitude corner, Ac, lists the maximum deviation in amplitude above and below the 1 kHz reference point. The listed minimum and maximum frequencies are guaranteed to be within the AC from minimum frequency to maximum frequency inclusive.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

FFT

Fast Fourier Transform.

Fs

Sampling Frequency.

Signal to Noise Ratio (SNR)

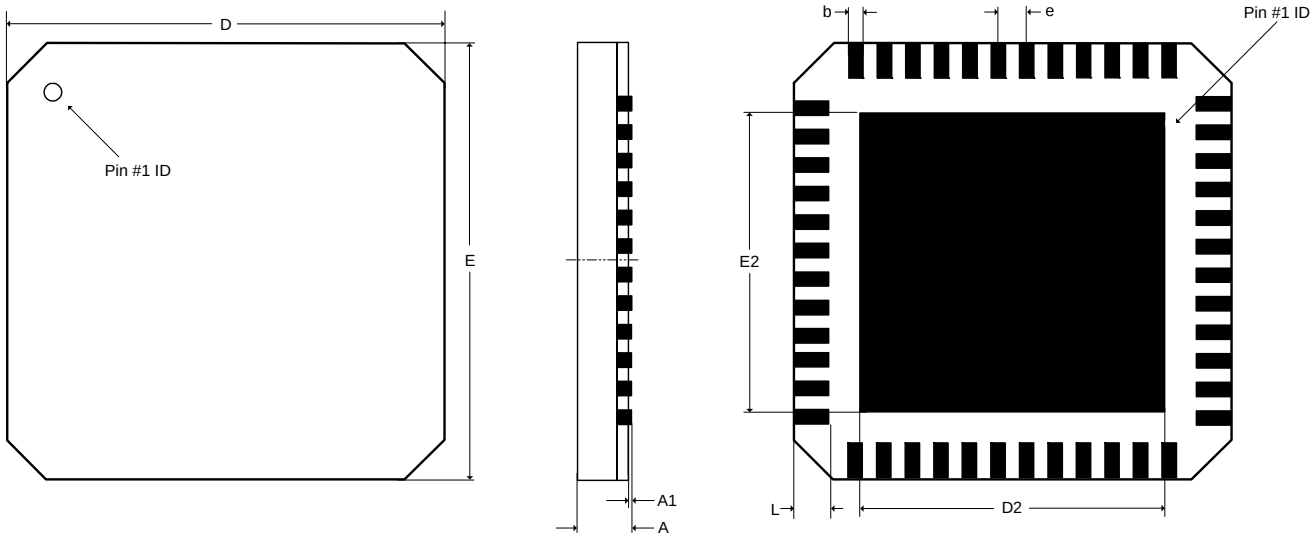
SNR, similar to DR, is the ratio of an arbitrary sinusoidal input signal to the RMS sum of the noise floor, in the presence of a signal. It is measured over a 20 Hz to 20 kHz bandwidth with units in dB.

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in %.

8. PACKAGE DIMENSIONS

48L QFN (9 × 9 MM BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.0354	--	--	0.90	1
A1	0.0000	--	0.0020	0.00	--	0.05	1
b	0.0118	0.0138	0.0157	0.30	0.35	0.40	1,2
D		0.3543 BSC			9.00 BSC		1
D2	0.2618	0.2677	0.2736	6.65	6.80	6.95	1
E		0.3543 BSC			9.00 BSC		1
E2	0.2618	0.2677	0.2736	6.65	6.80	6.95	1
e		0.0256 BSC			0.65 BSC		1
L	0.0177	0.0217	0.0276	0.45	0.55	0.70	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

Notes:

1. Dimensioning and tolerance per ASME Y4.5M - 1994.
2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

9. THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Junction to Case Thermal Impedance		θ_{JC}	-	1	-	°C/Watt
Junction to Ambient Thermal Impedance (Note 1)	2-Layer PCB	θ_{JA}	-	20	-	°C/Watt
	4-Layer PCB		-	18.5	-	

1. θ_{JA} is stated for a system with a thermal flag as described in Section 9.1 below.

9.1 Thermal Flag

This device is designed to have the metal flag on the bottom of the device soldered directly to a metal plane on the PCB. To enhance the thermal dissipation capabilities of the system, this metal plane should be coupled with vias to a large metal plane on the backside (and inner ground layer, if applicable) of the PCB.

In either case, it is beneficial to use copper fill in any unused regions inside the PCB layout, especially those immediately surrounding the CS44130. In addition to improving in electrical performance, this practice also aids in heat dissipation.

The heat dissipation capability required of the metal plane for a given output power can be calculated as follows:

$$T_{CA} = [(T_{J(MAX)} - T_A) / P_D] - \theta_{JC}$$

where,
T_{CA} = Thermal resistance of the metal plane in °C/Watt
$T_{J(MAX)}$ = Maximum rated operating junction temperature in °C, equal to 150 °C
T_A = Ambient temperature in °C
P_D = RMS power dissipation of the device, equal to $0.10*P_{RMS}$ (assuming 90% efficiency)
θ_{JC} = Junction-to-case thermal resistance of the device in °C/Watt

10.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS44130	Quad Half-Bridge Digital Amplifier Power Stage	48-QFN	Yes	Commercial	-10° to +70°C	Rail	CS44130-CNZ
						Tape and Reel	CS44130-CNZR
CRD44130-FB	20 W x 2 + 40 W x 1 Reference Design	-	-	-	-	-	CRD44130-FB

11.REFERENCES

1. Cirrus Logic, AN018: Layout and Design Rules for Data Converters and Other Mixed Signal Devices, Version 6.0, February 1998.

12.REVISION HISTORY

Release	Date	Changes
A1	September 2005	Initial Advance Release
A2	April 2006	2nd Advance Release -Updated "Features" on page 1 -Updated "Specified Operating Conditions" on page 7 -Updated "Absolute Maximum Ratings" on page 7 -Updated "PWM Output Characteristics" on page 9 -Updated "Protection and Error Reporting" on page 18 -Updated "Thermal Characteristics" on page 22
P1	July 2006	Preliminary Datasheet Release -Updated "DC Electrical Characteristics" on page 8 -Updated "PWM Output Characteristics" on page 9 -Updated "Thermal Characteristics" on page 22

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.