CS44210

Digital PWM Controller with Headphone Monitor

Features

- Up to 100 dB Dynamic Range
- 2.4 V to 5.0 V supply
- Sample rates up to 96 kHz
- Digital Tone Control
  - —3 selectable HPF and LPF corner frequencies
  - —12 dB boost for bass and treble - 1 dB step size
- Programmable Digital volume control
  - —+18 to -96 dB in 1 dB steps
- Peak signal soft limiting
- De-emphasis for 32 kHz, 44.1 kHz, and 48 kHz
- Selectable outputs for each channel including
  - —Channel A: R, L, mono (L + R) / 2, mute
  - —Channel B: R, L, mono (L + R) / 2, mute
- PWM PopGuard®

Description

The CS44210 is a complete stereo digital-to-PWM Class D audio amplifier system controller including interpolation, volume control, half bridge PWM driver outputs, and an integrated CS44L10 headphone amplifier in a 24-pin TSSOP package.

The CS44210 architecture uses a direct-to-digital approach that maintains digital signal integrity to the final output filter. This minimizes analog interference effects that can negatively affect system performance.

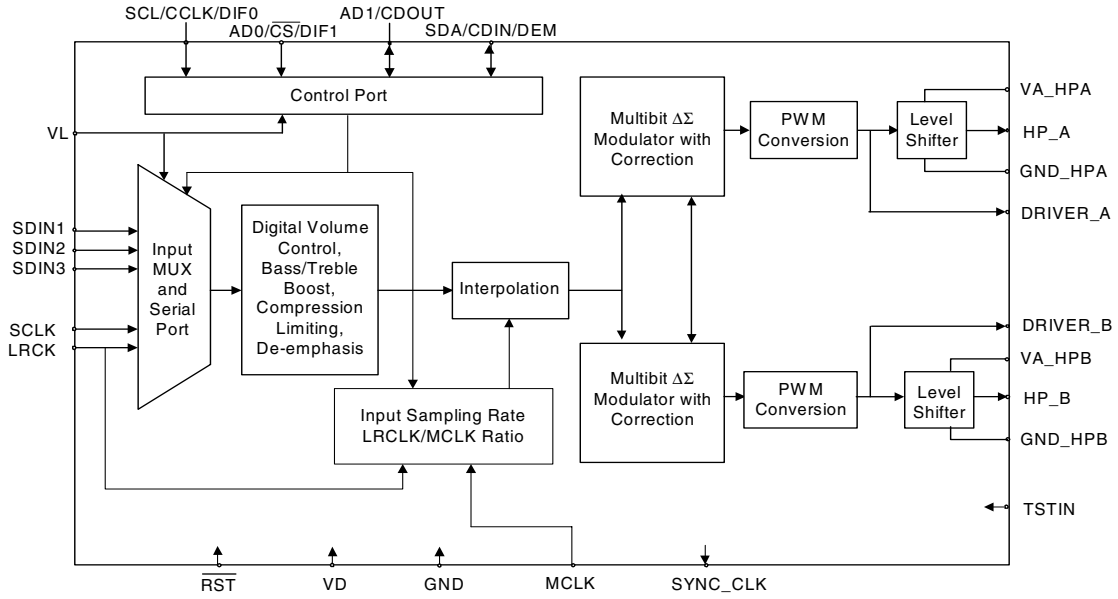
The CS44210 contains on-chip digital bass and treble boost, peak signal limiting, and de-emphasis. The PWM amplifier can achieve greater than 90% efficiency. This efficiency leads to longer battery life for portable systems, smaller device package, less heat sink requirements, and smaller power supplies.

The CS44210 provides all the controls necessary to drive higher voltage output stages for increased power levels.

The CS44210 is ideal for integrated, mult-function systems such as shelf-top audio systems, audio mini systems, audio video receivers (AVR), boom boxes and powered speakers.

ORDERING INFORMATION

CS44210-KZ -10 to 70 °C 24-pin TSSOP



Advance Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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1. CHARACTERISTICS AND SPECIFICATIONS

(T_A = 25 °C; GND = 0 V; Logic "1" = VL = 2.4 V; Logic "0" = GND = 0 V; Full-Scale Output Sine Wave, 997 Hz, MCLK = 12.288 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Fs for Single Speed Mode = 48 kHz, SCLK = 3.072 MHz; Fs for Double Speed Mode = 96 kHz, SCLK = 6.144 MHz. Test load R_L = 16 Ω, C_L = 10pF.) (See Typical CS44210 Connection Diagram.)

Parameter			Symbol	Min	Typ	Max	Unit
Headphone Output Dynamic Performance for VD = VL = VA_HPx = 2.4 V							
Dynamic Range	18 to 24-Bit	A-Weighted		TBD	93	-	dB
		UnWeighted		TBD	91	-	dB
	16-Bit	A-Weighted		-	91	-	dB
		Unweighted		-	89	-	dB
Total Harmonic Distortion + Noise		0 dBFS	THD+N	-	-62	TBD	dB
		-20 dBFS		-	-71	-	dB
		-60 dBFS		-	-31	-	dB
Interchannel Isolation		(1 kHz)		-	TBD	-	dB
Headphone Output Dynamic Performance for VD = VL = VA_HPx = 3.0 V							
Dynamic Range	18 to 24-Bit	A-Weighted		TBD	95	-	dB
		UnWeighted		TBD	92	-	dB
	16-Bit	A-Weighted		-	92	-	dB
		Unweighted		-	90	-	dB
Total Harmonic Distortion + Noise		0 dB	THD+N	-	-64	TBD	dB
		-20 dB		-	-72	-	dB
		-60 dB		-	-32	-	dB
Interchannel Isolation		(1 kHz)		-	TBD	-	dB
Headphone Output Dynamic Performance for VD = VL = VA_HPx = 5.0 V							
Dynamic Range	18 to 24-Bit	A-Weighted		TBD	99	-	dB
		UnWeighted		TBD	96	-	dB
	16-Bit	A-Weighted		-	91	-	dB
		Unweighted		-	93	-	dB
Total Harmonic Distortion + Noise		0 dB	THD+N	-	-67	TBD	dB
		-20 dB		-	-76	-	dB
		-60 dB		-	-36	-	dB
Interchannel Isolation		(1 kHz)		-	TBD	-	dB

CHARACTERISTICS AND SPECIFICATIONS (Continued)

Parameters		Symbol	Min	Typ	Max	Units
PWM Headphone Output						
Full Scale Headphone Output Voltage			TBD	0.85 x VA_HP	TBD	Vp
Headphone Output Quiescent Voltage			-	0.5 x VA_HP	-	VDC
Interchannel Gain Mismatch			-	0.1	-	dB
Modulation Index			-	-	85	%
Maximum Headphone Output	VA_HPx=2.4V	I_{HP}	-	45	-	mA
AC-Current	VA_HPx=5.0V		-	80	-	mA

Parameter		Symbol	Single Speed Mode Min	Typ	Max	Double Speed Mode Min	Typ	Max	Unit
Digital Filter Response (Note 1)									
Passband	to -0.05 dB corner		0	-	.4535	-	-	-	Fs
(Note 2)	to -0.1 dB corner		-	-	-	0	-	.4426	Fs
	to -3 dB corner		0	-	.4998	0	-	.4984	Fs
Frequency Response 10 Hz to 20 kHz	(Note 3)		-.02	-	+.08	0	-	+0.11	dB
StopBand			.5465	-	-	.577	-	-	Fs
StopBand Attenuation	(Note 4)		50	-	-	55	-	-	dB
Group Delay		tgd	-	9/Fs	-	-	4/Fs	-	s
Passband Group Delay Deviation	0 - 40 kHz		-	-	-	-	±1.39/Fs	-	s
	0 - 20 kHz		-	±0.36/Fs	-	-	±0.23/Fs	-	s
De-emphasis Error	Fs = 32 kHz		-	-	+.2/-.1				dB
(Relative to 1 kHz)	Fs = 44.1 kHz		-	-	+.05/-.14		(Note 5)		dB
	Fs = 48 kHz		-	-	+0/-.22				dB

Note:

1. Filter response is not tested but is guaranteed by design.
2. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 11-18) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
3. Referenced to a 1 kHz, full-scale sine wave.
4. For Single Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
   For Double Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.
5. De-emphasis is not available in double speed mode.

ABSOLUTE MAXIMUM RATINGS (GND = 0V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supplies:	Headphone	VA_HPx	2.4	5.5	V
	Interface	VL	2.4	5.5	V
	Digital	VD	2.4	5.5	V
Input Current, Any Pin Except Supplies		I_{in}		±10	mA
Digital Input Voltage		V_{IND}	-0.3	VL + 0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

CAUTION: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (GND = 0V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
Ambient Temperature		T_A	-10	-	70	°C
DC Power Supplies:	Headphone	VA_HPx	2.4	-	5.0	V
	Interface	VL	2.4	-	5.0	V
	Digital	VD	2.4	-	5.0	V

SWITCHING CHARACTERISTICS (T_A = -10 to 70°C; VL = 2.4V - 5.0V; Inputs: Logic 0 = GND, Logic 1 = VL, CL = 20pF)

Parameters		Symbol	Min	Typ	Max	Units
Input Sample Rate	Single Speed Mode	Fs	8	-	50	kHz
	Double Speed Mode	Fs	50	-	100	kHz
MCLK Duty Cycle			40	50	60	%
LRCK Duty Cycle			40	50	60	%
SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
SCLK Period	Single Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
	Double Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	ns
SCLK rising to LRCK edge delay		t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	-	ns
SDIN valid to SCLK rising setup time		t_{sdlrs}	20	-	-	ns
SCLK rising to SDIN hold time		t_{sdh}	20	-	-	ns

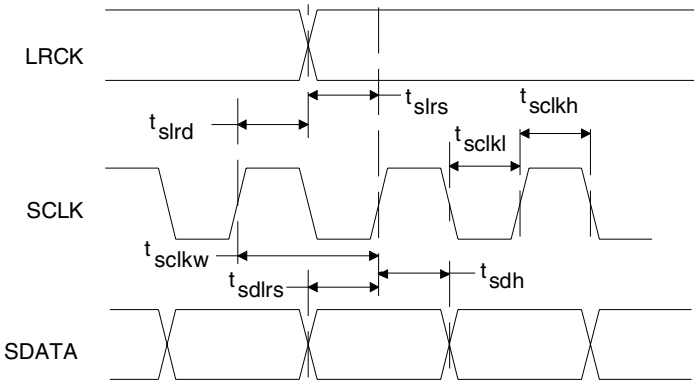


Figure 1. Serial Audio Data Interface Timing

POWER AND THERMAL CHARACTERISTICS

(GND = 0 V; All voltages with respect to ground. All measurements taken with all zeros input and open outputs, unless otherwise specified.)

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current-	VA_HPx= 2.4 V	I_{VA_HP}	-	1	-	mA
Normal Operation	VD = 2.4 V	I_D	-	10	-	mA
	VL= 2.4 V	I_L	-	1	-	mA
Power Supply Current-	VA_HPx = 2.4V	I_{VA_HP}	-	TBD	-	µA
Power Down Mode (Note 6)	VD = 2.4V	I_D	-	TBD	-	µA
	VL = 2.4V	I_L	-	TBD	-	µA
Power Supply Current-	VA_HPx = 5.0 V	I_{VA_HP}	-	2	-	mA
Normal Operation	VD = 5.0 V	I_D	-	20	-	mA
	VL = 5.0 V	I_L	-	2	-	mA
Power Supply Current-	VA_HPx = 5.0V	I_{VA_HP}	-	TBD	-	µA
Power Down Mode (Note 6)	VD = 5.0V	I_D	-	TBD	-	µA
	VL = 5.0 V	I_L	-	TBD	-	µA
Total Power Dissipation-	All Supplies = 2.4 V		-	29	-	mW
Normal Operation	All Supplies = 5.0 V		-	120	-	mW
Power Supply Rejection Ratio		PSRR	-	0	-	dB
Maximum Headphone Power Dissipation	VA=2.4 V		-	23	-	mW
(1 kHz full-scale sine wave into 16 ohm load)	VA=5.0 V		-	100	-	mW
Package Thermal Resistance		θ_{JA}	-	75	-	°C/Watt

Note:

6. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

DIGITAL CHARACTERISTICS (T_A = 25° C; VL = 2.4 V - 3.6 V; GND = 0 V)

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	0.7 x VL	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.3 x VL	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
High-Level Output Voltage (Pin 15)	(Note 7)	V_{OH}	0.7 x VL	-	-	V
Low-Level Output Voltage (Pin 15)	(Note 7)	V_{OL}	-	-	0.3 x VL	V
High-Level Output Voltage (Pins 11, 13, 14)	(Note 7)	V_{OH}	0.7 x VD	-	-	V
Low-Level Output Voltage (Pins 11, 13, 14)	(Note 7)	V_{OL}	-	-	0.3 x VD	V

SWITCHING CHARACTERISTICS- CONTROL PORT- TWO-WIRE FORMAT

(Note 8) (T_A = 25° C; VL = 2.4 V - 5.0 V; Inputs: Logic 0 = GND, Logic 1 = VL, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SCL Clock Frequency		f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start		t_{irs}	500	-	ns
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling	(Note 9)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising		t_{sud}	250	-	ns
Rise Time of SCL and SDA		t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA		t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	(Note 10)	t_{ack}	-	(Note 11)	ns

Note:

7. V_{OH} and V_{OL} are tested at an output current of TBD mA.
8. The Two-Wire Format is compatible with the I^2C protocol.
9. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.
10. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.
11. $\frac{5}{256 \times Fs}$ for Single-Speed Mode and $\frac{5}{128 \times Fs}$ for Double-Speed Mode.

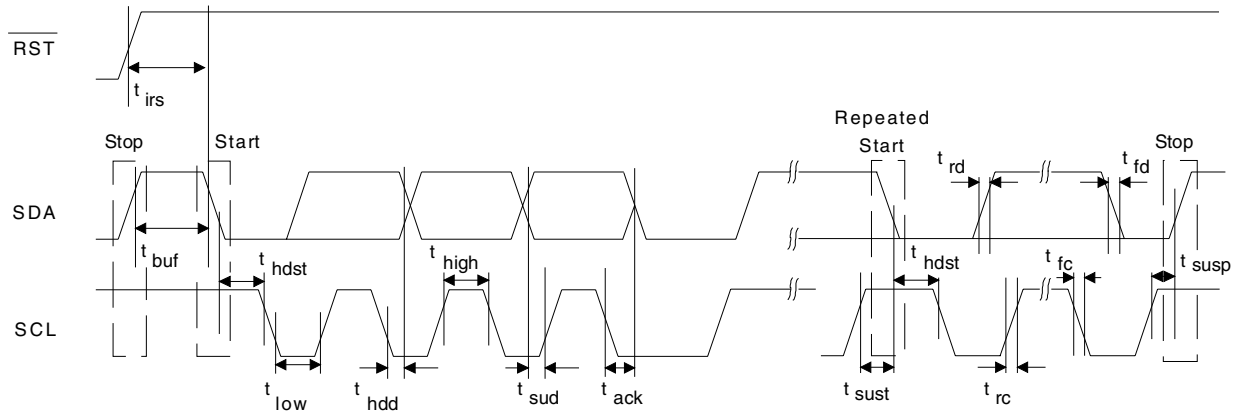


Figure 2. Control Port Timing - Two-Wire Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

(T_A = 25° C; VL = 2.4 V - 5.0 V; Inputs: Logic 0 = GND, Logic 1 = VL, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 12)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 13)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 14)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 15)	t_{f2}	-	100	ns
Transition time from CCLK to CDOUT valid	(Note 15)	t_{scdov}	-	40	ns
Time from $\overline{CS}$ rising to CDOUT high-Z	(Note 16)	t_{cscdo}	-	20	ns

Note:

12. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.
13. Data must be held for sufficient time to bridge the transition time of CCLK.
14. For F_{SCK} < 1 MHz.
15. CDOUT should *not* be sampled during this time period.
16. This time is not tested but is guaranteed by design.

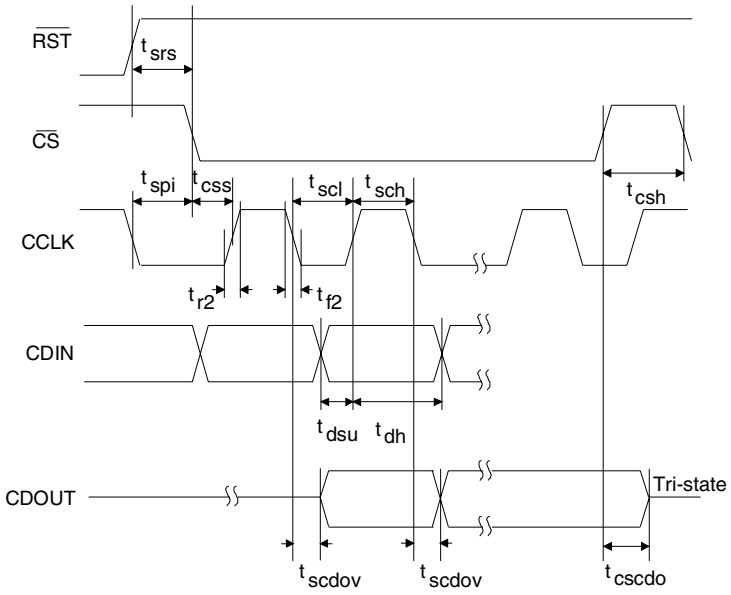
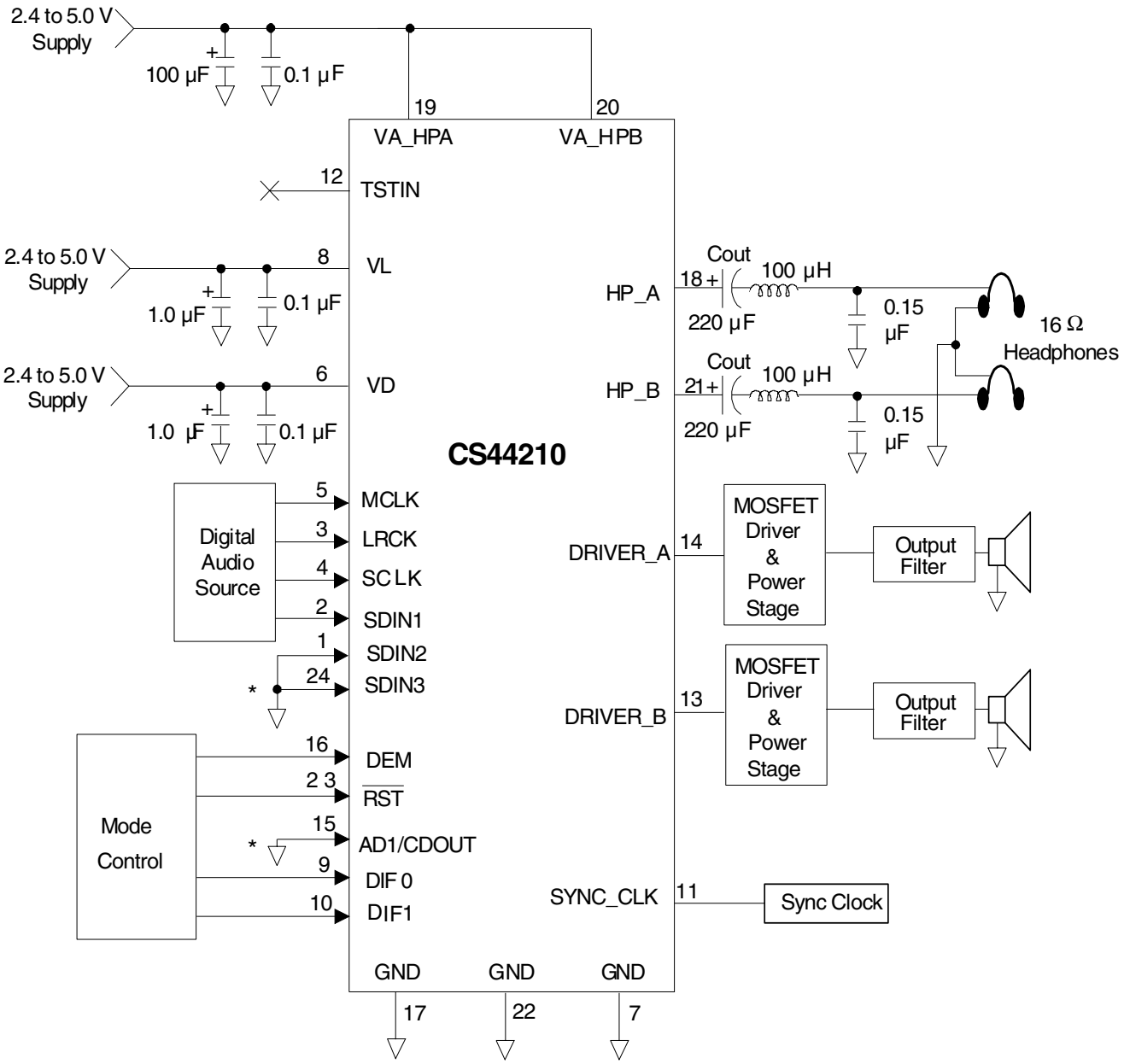


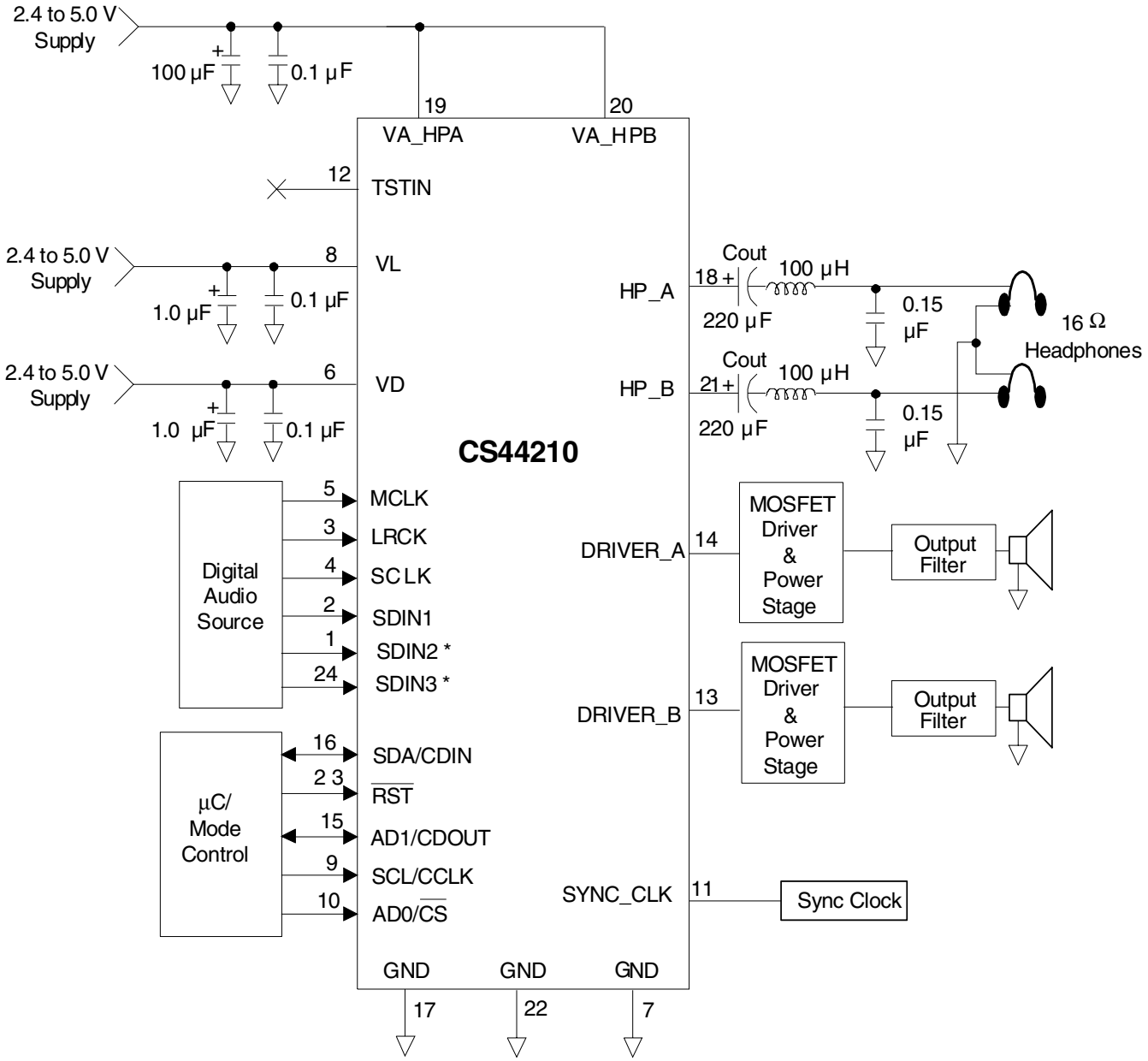
Figure 3. Control Port Timing - SPI Format

2. TYPICAL CONNECTION DIAGRAMS



* This feature is unavailable in this mode.
This pin should be grounded.

Figure 4. Typical CS44210 Connection Diagram Stand-Alone Mode



* Unused SDIN pins should be connected to GND

Figure 5. Typical CS44210 Connection Diagram Control Port Mode

3. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
2h	Power and Muting Control	SZC1	SZC0	PDN	FLT	RUPBYP	RDNBYP	Reserved	Reserved
	default	1	0	1	0	0	0	0	0
3h	Channel A Volume Control	VOLA7	VOLA6	VOLA5	VOLA4	VOLA3	VOLA2	VOLA1	VOLA0
	default	0	0	0	0	0	0	0	0
4h	Channel B Volume Control	VOLB7	VOLB6	VOLB5	VOLB4	VOLB3	VOLB2	VOLB1	VOLB0
	default	0	0	0	0	0	0	0	0
5h	Tone Control	BB3	BB2	BB1	BB0	TB3	TB2	TB1	TB0
	default	0	0	0	0	0	0	0	0
6h	Mode Control 1	BBCF1	BBCF0	TBCF1	TBCF0	TC1	TC0	TC_EN	LIM_EN
	default	0	0	0	0	0	0	0	0
7h	Limiter Attack Rate	ARATE7	ARATE6	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0
	default	0	0	0	1	0	0	0	0
8h	Limiter Release Rate	RRATE7	RRATE6	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0
	default	0	0	1	0	0	0	0	0
9h	Volume and Mixing Control	IS1	IS0	RMP_SP1	RMP_SP0	ATAPI3	ATAPI2	ATAPI1	ATAPI0
	default	0	0	0	1	1	0	0	1
Ah	Mode Control2	MCLKDIV	CLKDV1	CLKDV0	DBS	FRQSFT1	FRQSFT0	DEM1	DEM0
	default	0	0	0	0	0	0	0	0
Bh	Mode Control 3	DIF1	DIF0	A=B	VCBYP	CP_EN	FREEZE	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
Ch	Revision Indicator	Reserved	Reserved	Reserved	Reserved	REV3	REV2	REV1	REV0
	default	0	0	0	0	Read Only	Read Only	Read Only	Read Only

Table 1. Register Quick Reference

4. REGISTER DESCRIPTIONS

4.1 Power and Muting Control (address 02h)

7	6	5	4	3	2	1	0
SZC1	SZC0	PDN	FLT	RUPBYP	RDNBYP	Reserved	Reserved
1	0	1	0	0	0	0	0

4.1.1 SOFT RAMP AND ZERO CROSS CONTROL (SZC)

Default = 10
00 - Immediate Change
01 - Zero Cross Control
10 - Ramped Control
11 - Reserved

Function:

Immediate Change

When Immediate Change is selected, all level changes will take effect immediately in one step.

Zero Cross Control

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period of 512 sample periods (10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Ramped Control

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Note: Ramped Control is not available in Double Speed Mode.

4.1.2 POWER DOWN (PDN)

Default = 1
0 - Disabled
1 - Enabled

Function:

The entire device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power-down bit defaults to ‘enabled’ on power-up and must be disabled before normal operation in Control Port mode can occur.

4.1.3 FLOAT OUTPUT (FLT)

Default = 0
0 - Disabled
1 - Enabled

Function:

When enabled, this bit will cause the headphone output of the CS44210 to float when in the power down state (PDN=1). The float function can be used in single-ended applications to maintain the charge on the DC-blocking capacitor during power transients. On power transitions, the output will quickly change to the bias point, however, if the DC-blocking capacitor still has a full charge, as in short power cycles, the transition will be very small, often inaudible. Refer to Section 6.4.

4.1.4 RAMP UP BYPASS (RUPBYP)

Default = 0
0 - Normal
1 - Bypass

Function:

When in normal mode, the duty cycle of the output PWM signal is increased at a rate determined by the Ramp Speed variable (RMP_SPx). Normal mode is used in Single Ended applications to reduce pops in the output caused by the DC-blocking capacitor. When the ramp up function is bypassed in Single Ended applications, there will be an abrupt change in the output signal. Refer to Section 6.4.

4.1.5 RAMP DOWN BYPASS (RDNBYP)

Default = 0
0 - Disabled
1 - Enabled

Function:

When in normal mode, the duty cycle of the output PWM signal is decreased at a rate determined by the Ramp Speed variable (RMP_SPx). Normal mode is used in Single Ended applications to reduce pops in the output caused by the DC-blocking capacitor and changes in bias conditions. When the ramp down function is bypassed in Single Ended applications, there will be an abrupt change in the output signal. Refer to Section 6.4.

4.2 Channel A Volume Control (address 03h) (VOLA)

4.3 Channel B Volume Control (address 04h) (VOLB)

7	6	5	4	3	2	1	0
VOLx7	VOLx6	VOLx5	VOLx4	VOLx3	VOLx2	VOLx1	VOLx0
0	0	0	0	0	0	0	0

Default = 0 dB (No attenuation)

Function:

The Volume Control registers allow independent control of the signal levels in 1 dB increments from +18 to -96 dB. Volume settings are decoded using a 2's complement code, as shown in Table 2. The volume changes are implemented as dictated by the Soft and Zero Cross bits. All volume settings less than -96 dB are equivalent to muting the channel via the ATAPI bits (see Section 4.8.3).

Note: All volume settings greater than +18 dB are interpreted as +18 dB.

Binary Code	Decimal Value	Volume Setting
00001010	12	+12 dB
00000111	7	+7 dB
00000000	0	0 dB
11000100	-60	-60 dB
10100110	-90	-90 dB

Table 2. Example Volume Settings

4.4 Tone Control (address 05h)

7	6	5	4	3	2	1	0
BB3	BB2	BB1	BB0	TB3	TB2	TB1	TB0
0	0	0	0	0	0	0	0

4.4.1 BASS BOOST LEVEL (BB)

Default = 0 dB (No Bass Boost)

Function:

The level of the shelving bass boost filter is set by Bass Boost Level. The level can be adjusted in 1 dB increments from 0 to +12 dB of boost. Boost levels are decoded as shown in Table 3. Levels above +12 dB are interpreted as +12 dB.

Binary Code	Decimal Value	Boost Setting
0000	0	0 dB
0010	2	+2 dB
1010	6	+6 dB
1001	9	+9 dB
1100	12	+12 dB

Table 3. Example Bass Boost Settings

4.4.2 TREBLE BOOST LEVEL (TB)

Default = 0 dB (No Treble Boost)

Function:

The level of the shelving treble boost filter is set by Treble Boost Level. The level can be adjusted in 1 dB increments from 0 to +12 dB of boost. Boost levels are decoded as shown in Table 4. Levels above +12 dB are interpreted as +12 dB.

Note: Treble Boost is not available in Double Speed Mode.

Binary Code	Decimal Value	Boost Setting
0000	0	0 dB
0010	2	+2 dB
1010	6	+6 dB
1001	9	+9 dB
1100	12	+12 dB

Table 4. Example Treble Boost Settings

4.5 Mode Control 1 (address 06h)

7	6	5	4	3	2	1	0
BBCF1	BBCF0	TBCF1	TBCF0	TC1	TC0	TC_EN	LIM_EN
0	0	0	0	0	0	0	0

4.5.1 BASS BOOST CORNER FREQUENCY (BBCF)

Default = 00
00 - 50 Hz
01 - 100 Hz
10 - 200 Hz
11 - Reserved

Function:

The bass boost corner frequency is user-selectable. The corner frequency is a function of LRCK (sampling frequency), the DBS bit and the BBCF bits as shown in Table 5 and Table 6.

BBCF	LRCK in Single Speed Mode (DBS=0)			
Fs	48 kHz	24 kHz	12 kHz	8 kHz
00	50 Hz	25 Hz	12.5 Hz	8.33 Hz
01	100 Hz	50 Hz	25 Hz	16.7 Hz
10	200 Hz	100 Hz	50 Hz	33.3 Hz
11	Reserved	Reserved	Reserved	Reserved

Table 5. Base Boost Corner Frequencies in Single Speed Mode

BBCF	LRCK in Double Speed Mode (DBS=1)			
Fs	96 kHz	48 kHz	24 kHz	16 kHz
00	50 Hz	25 Hz	12.5 Hz	8.33 Hz
01	100 Hz	50 Hz	25 Hz	16.7 Hz
10	200 Hz	100 Hz	50 Hz	33.3 Hz
11	Reserved	Reserved	Reserved	Reserved

Table 6. Base Boost Corner Frequencies in Double Speed Mode

4.5.2 TREBLE BOOST CORNER FREQUENCY (TBCF)

Default = 00
00 - 2 kHz
01 - 4 kHz
10 - 7 kHz
11 - Reserved

Function:

The treble boost corner frequency is user selectable. The corner frequency is a function of LRCK (sampling frequency) and the TBCF bits as shown in Table 7.

Note: Treble Boost is not available in Double Speed Mode.

TBCF Fs	LRCK in Single Speed Mode (DBS=0)			
	48 kHz	24 kHz	12 kHz	8 kHz
00	2 kHz	1 kHz	0.5 kHz	0.33 kHz
01	4 kHz	2 kHz	1 kHz	0.67 kHz
10	7 kHz	3.5 kHz	1.75 kHz	1.17 kHz
11	Reserved	Reserved	Reserved	Reserved

Table 7. Treble Boost Corner Frequencies in Single Speed Mode

4.5.3 TONE CONTROL MODE (TC)

Default = 00
00 - All settings are taken from user registers
01 - 12 dB of Bass Boost at 100 Hz and 6 dB of Treble Boost at 7 kHz (at LRCK = 48 kHz)
10 - 8 dB of Bass Boost at 100 Hz and 4 dB of Treble Boost at 7 kHz (at LRCK = 48 kHz)
11 - 4 dB of Bass Boost at 100 Hz and 2 dB of Treble Boost at 7 kHz (at LRCK = 48 kHz)

Function:

The Tone Control Mode bits determine how the Bass Boost and Treble Boost features are configured. The user-defined settings from the Bass and Treble Boost Level and Corner Frequency registers are used when these bits are set to '00'. Alternately, one of three pre-defined settings may be used (these settings are a function of LRCK - refer to tables 5, 6, and 7).

Note: Treble boost is not available in Double Speed Mode.

4.5.4 TONE CONTROL ENABLE (TC_EN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The Bass Boost and Treble Boost features are active when this function is enabled.

4.5.5 PEAK SIGNAL LIMITER ENABLE (LIM_EN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The CS44210 will limit the maximum signal amplitude to prevent clipping when this function is enabled. Peak Signal Limiting is performed by first decreasing the Bass and Treble Boost Levels. If the signal is still clipping, the digital attenuation is increased. The attack rate is determined by the Limiter Attack Rate register.

Once the signal has dropped below the clipping level, the attenuation is decreased back to the user selected level followed by the Bass Boost being increased back to the user selected level. The release rate is determined by the Limiter Release Rate register.

Note: The A=B bit should be set to '1' for optimal limiter performance.

4.6 Limiter Attack Rate (address 07h) (ARATE)

7	6	5	4	3	2	1	0
ARATE7	ARATE6	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0
0	0	0	1	0	0	0	0

Default = 10h - 2 LRCK's per 1/8 dB

Function:

The limiter attack rate is user-selectable. The rate is a function of sampling frequency, As, and the value in the Limiter Attack Rate register. Rates are calculated using the function RATE = 32/{value}, where {value} is the decimal value in the Limiter Attack Rate register and RATE is in LRCK's per 1/8 dB of change.

Note: A value of zero in this register is not recommended, as it will induce erratic behavior of the limiter. Use the LIM_EN bit to disable the limiter function (see *"Peak Signal Limiter Enable (LIM_EN)"*).

Binary Code	Decimal Value	LRCK's per 1/8 dB
00000001	1	32
00010100	20	1.6
00101000	40	0.8
00111100	60	0.53
01011010	90	0.356

Table 8. Example Limiter Attack Rate Settings

4.7 Limiter Release Rate (address 08h) (RRATE)

7	6	5	4	3	2	1	0
RRATE7	RRATE6	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0
0	0	1	0	0	0	0	0

Default = 20h - 16 LRCK's per 1/8 dB

Function:

The limiter release rate is user-selectable. The rate is a function of sampling frequency, Fs, and the value in the Limiter Release Rate register. Rates are calculated using the function RATE = 512/{value}, where {value} is the decimal value in the Limiter Release Rate register and RATE is in LRCK's per 1/8 dB of change.

Note: A value of zero in this register is not recommended, as it will induce erratic behavior of the limiter. Use the LIM_EN bit to disable the limiter function (see *"Peak Signal Limiter Enable (LIM_EN)"*).

Binary Code	Decimal Value	LRCK's per 1/8 dB
00000001	1	512
00010100	20	25
00101000	40	12
00111100	60	8
01011010	90	5

Table 9. Example Limiter Release Rate Settings

4.8 Volume and Mixing Control (address 09h)

7	6	5	4	3	2	1	0
IS1	IS0	RMP_SP1	RMP_SP0	ATAPI3	ATAPI2	ATAPI1	ATAPI0
0	0	0	0	1	0	0	1

4.8.1 INPUT MUX SELECTION (IS)

Default = 00

00 - Selects SDIN1 as input
01 - Selects SDIN2 as input
10 - Selects SDIN3 as input
11 - Reserved

Function:

The Input Mux Selector determines which SDIN input is selected.

4.8.2 RAMP SPEED (RMP_SP)

Default = 01

00 - Ramp speed = approximately 0.1 seconds
01 - Ramp speed = approximately 0.2 seconds
10 - Ramp speed = approximately 0.3 seconds
11 - Ramp speed = approximately 0.65 seconds

Function:

This feature is used in Single Ended applications to reduce pops in the output caused by the DC-blocking capacitor. When in control port mode, the Ramp Speed sets the time for the PWM signal to linearly ramp up and down from the bias point (50% PWM duty cycle). Refer to Section 6.4.

4.8.3 ATAPI CHANNEL MIXING AND MUTING (ATAPI)

Default = 1001 - HP_A = L, HP_B = R (Stereo)

Function:

The CS44210 implements the channel mixing functions of the ATAPI CD-ROM specification. Refer to Table 10 and Figure 6 for additional information.

Note: All mixing functions occur prior to the digital volume control.

ATAPI3	ATAPI2	ATAPI1	ATAPI0	HP_A	HP_B
0	0	0	0	MUTE	MUTE
0	0	0	1	MUTE	R
0	0	1	0	MUTE	L
0	0	1	1	MUTE	[(L+R)/2]
0	1	0	0	R	MUTE
0	1	0	1	R	R
0	1	1	0	R	L
0	1	1	1	R	[(L+R)/2]
1	0	0	0	L	MUTE
1	0	0	1	L	R
1	0	1	0	L	L
1	0	1	1	L	[(L+R)/2]
1	1	0	0	[(L+R)/2]	MUTE
1	1	0	1	[(L+R)/2]	R
1	1	1	0	[(L+R)/2]	L
1	1	1	1	[(L+R)/2]	[(L+R)/2]

Table 10. ATAPI Decode

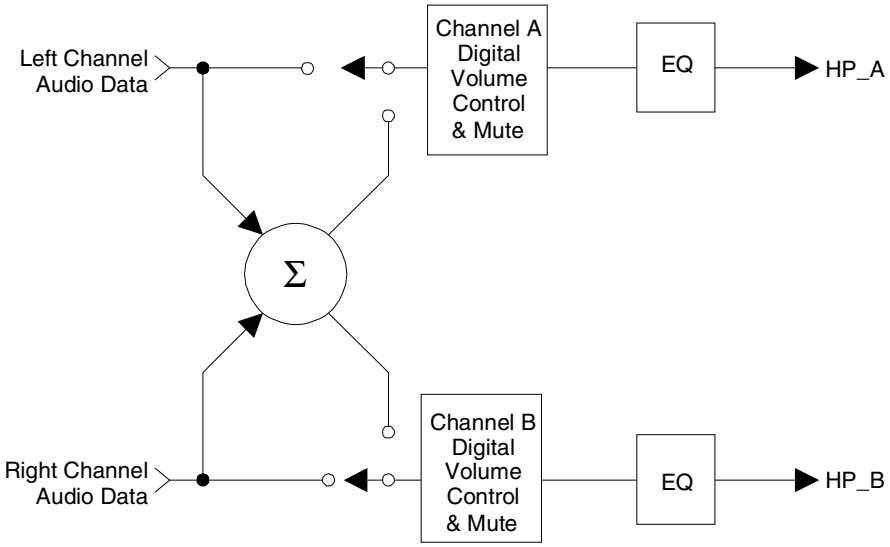


Figure 6. Dynamics Control Block Diagram

4.9 Mode Control 2 (address 0Ah)

7	6	5	4	3	2	1	0
MCLKDIV	CLKDV1	CLKDV0	DBS	FRQSFT1	FRQSFT0	DEM1	DEM0
0	0	0	0	0	0	0	0

4.9.1 MASTER CLOCK DIVIDE ENABLE (MCLKDIV)

Default = 0

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2 prior to all other internal circuitry. MCLKDIV, DBS, CLKDIV and FRQSFT are set per the user's MCLK and LRCK requirements. Refer to Tables 11, 12, 13, 14, and Section 6.2.

4.9.2 CLOCK DIVIDE (CLKDIV)

Default = 00

Function:

MCLKDIV, DBS, CLKDIV and FRQSFT are set per the user's MCLK and LRCK requirements. Refer to Tables 11, 12, 13, 14, and Section 6.2.

4.9.3 DOUBLE SPEED MODE (DBS)

Default = 0
0 - Single Speed
1 - Double Speed (DBS)

Function:

Single Speed supports 8kHz to 50 kHz sample rates and Double Speed supports 50 kHz to 96kHz sample rates. MCLKDIV, DBS, CLKDIV and FRQSFT are set per the user's MCLK and LRCK requirements. Refer to Tables 11, 12, 13, 14, and Section 6.2.

Note: De-emphasis, ramp control, and treble control are not available in Double Speed Mode.

4.9.4 FREQUENCY SHIFT (FRQSFT)

Default = 00

Function:

MCLKDIV, DBS, CLKDIV and FRQSFT are set per the user's MCLK and LRCK requirements. Refer to Tables 11, 12, 13, 14, and Section 6.2.

	DBS = 0 MCLKDIV = 0		DBS = 0 MCLKDIV = 1						
LRCK (kHz)	MCLK/ LRCK	MCLK (MHz)	MCLK/ LRCK	MCLK (MHz)	FRQSFT1	FRQSFT0	CLKDIV1	CLKDIV0	PWM Switching Freq. (kHz)
48	256	12.288	512	24.576	0	0	0	0	384
48	384	18.432	768	36.864	0	0	0	1	
48	512	24.576	1024	49.152	0	0	1	0	
44.1	256	11.2896	512	22.5792	0	0	0	0	352.8
44.1	384	16.9344	768	33.8688	0	0	0	1	
44.1	512	22.5792	1024	45.1584	0	0	1	0	
32	512	16.384	1024	32.768	0	1	0	0	512
32	768	24.576	1536	49.152	0	1	0	1	
32	1024	32.768	2048	65.536	0	1	1	0	
24	512	12.288	1024	24.576	0	1	0	0	384
24	768	18.432	1536	36.864	0	1	0	1	
24	1024	24.576	2048	49.152	0	1	1	0	
12	1024	12.288	2048	24.576	1	0	0	0	384
12	1536	18.432	3072	36.864	1	0	0	1	
12	2048	24.576	4096	49.152	1	0	1	0	
8	1536	12.288	3072	24.576	1	1	0	0	384
8	2304	18.432	4608	36.864	1	1	0	1	
8	3072	24.576	6144	49.152	1	1	1	0	

Table 11. Single Speed Clock Modes - Control Port Mode

LRCK (kHz)	MCLK/ LRCK	MCLK (MHz)	PWM Switching Freq. (kHz)
48	256	12.288	384
48	384	18.432	
48	512	24.576	
44.1	256	11.2896	352.8
44.1	384	16.9344	
44.1	512	22.5792	
32	1024	32.768	512
24	1024	24.576	384
12	2048	24.576	
8	1536	12.288	
8	2304	18.432	
8	3072	24.576	

Table 12. Single Speed Clock Modes - Stand-Alone Mode

	DBS = 1 MCLKDIV = 0		DBS = 1 MCLKDIV = 1						
LRCK (kHz)	MCLK/ LRCK	MCLK (MHz)	MCLK/ LRCK	MCLK (MHz)	FRQSFT1	FRQSFT0	CLKDIV1	CLKDIV0	PWM Switching Freq. (kHz)
96	128	12.288	256	24.576	0	0	0	0	384
96	192	18.432	384	36.864	0	0	0	1	
96	256	24.576	512	49.152	0	0	1	0	

Table 13. Double Speed Clock Modes - Control Port Mode

LRCK (kHz)	MCLK/ LRCK	MCLK (MHz)	PWM Switching Freq. (kHz)
96	128	**12.288**	**384**
96	192	**18.432**	

Table 14. Double Speed Clock Modes - Stand-Alone Mode

4.9.5 DE-EMPHASIS CONTROL (DEM)

Default = 00
00 - Disabled
01 - 44.1 kHz
10 - 48 kHz
11 - 32 kHz

Function:

Selects the appropriate digital filter to maintain the standard 15 µs/50 µs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates (see Figure 7).

Note: De-emphasis is not available in double speed mode.

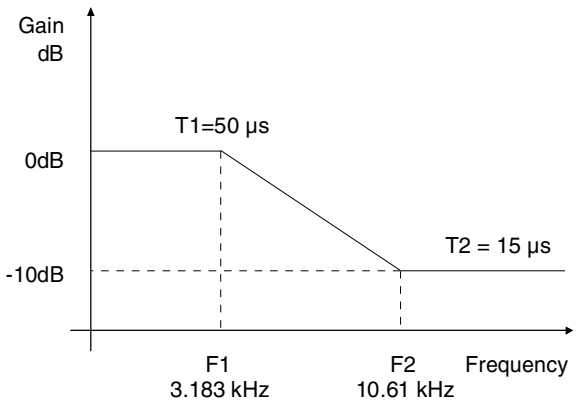


Figure 7. De-Emphasis Curve

4.10 Mode Control 3 (address 0Bh)

7	6	5	4	3	2	1	0
DIF1	DIF0	A=B	VCBYP	CP_EN	FREEZE	HPSEN	Reserved
0	0	0	0	0	0	0	0

4.10.1 DIGITAL INTERFACE FORMATS (DIF)

Default = 00
00 - I^2S
01 - Right Justified, 16 bit
10 - Left Justified
11 - Right Justified, 24 bit

Function:

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in figures 19 through 22.

4.10.2 CHANNEL A VOLUME = CHANNEL B VOLUME (A=B)

Default = 0
0 - Disabled
1 - Enabled

Function:

The HP_A and HP_B volume levels and the DRIVER_x outputs are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both HP_A, HP_B, DRIVER_A and DRIVER_B are determined by the A Channel Volume Control Byte and the B Channel Byte is ignored when this function is enabled.

4.10.3 VOLUME CONTROL BYPASS (VCBYP)

Default = 0
0 - Disabled
1 - Enabled

Function:

The digital volume control section is bypassed when this function is enabled. This disables the digital volume control, muting, bass boost, treble boost, limiting, and ATAPI functions.

4.10.4 CONTROL PORT ENABLE (CP_EN)

Default = 0
0 - Disabled
1 - Enabled

Function:

This bit defaults to 0, allowing the device to power-up in Stand-Alone mode. The Control port mode can be accessed by setting this bit to 1. This will allow the operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode. Refer to Section 7.1.

4.10.5 FREEZE (FREEZE)

Default = 0
0 - Disabled
1 - Enabled

Function:

This function allows modifications to be made to the registers without the changes being taking effect until the FREEZE is disabled. To make multiple changes in the Control port registers take effect simultaneously, you will first enable the FREEZE Bit, then make all register changes, then Disable the FREEZE bit.

4.11 Revision Indicator (address 0Ch)[Read Only]

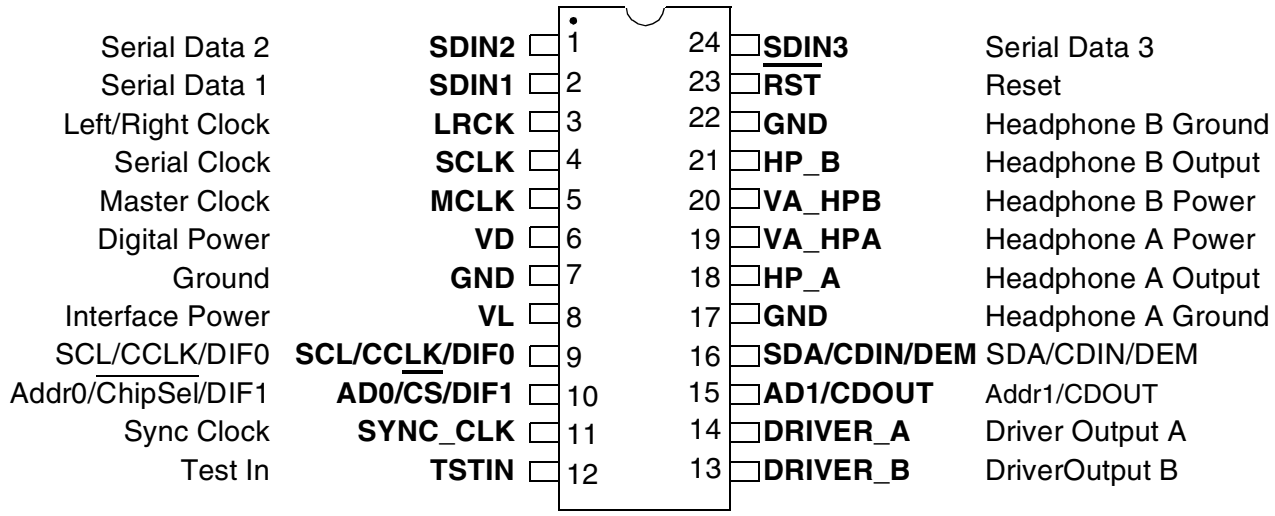
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	REV3	REV2	REV1	REV0
0	0	0	0	0	0	0	0

Default = none
0000 - Revision A
0001 - Revision B
0010 - Revision C
etc.

Function:

This read-only register indicates the revision level of the device.

5. PIN DESCRIPTION



SDIN1 SDIN2 SDIN3	2 1 24	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data. Unused inputs should be grounded.
LRCK	3	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SCLK	4	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
MCLK	5	**Master Clock** (*Input*) - Clock source for the PWM modulator and digital filters. Table 11, 12, 13 and 14 illustrate several standard audio sample rates and the required master clock frequencies.
VD	6	**Digital Power** (*Input*) **-** Positive power supply for the digital section. Refer to "Recommended Operating Conditions" for appropriate voltages.
GND	7, 17 & 22	**Ground** (*Input*) - Ground Reference.
VL	8	**Logic Power** (*Input*) **-** Determines the required signal level for the digital input/output. Refer to "Recommended Operating Conditions" for appropriate voltages.
Sync Clock	11	**SYNC_CLK** (*Output)* - Provides a high frequency clock signal at 32 x PWM switching frequency to synchronize external circuitry, if needed.
TSTIN	12	**Test In** (*Input)* - This pin is not used and must remaing floating.
DRIVER_A DRIVER_B	14 13	**DRIVER OUTPUTS**(*Outputs)* Outputs used to drive external power devices.
HP_A HP_B	18 21	**Headphone Outputs** (*Output*) - PWM Headphone Outputs. An external LC filter should be added to suppress high frequency switching noise. A DC blocking capacitor is also required. Refer to Typical Connection Diagrams.
VA_HPA VA_HPB	19 20	**Headphone Amplifier Power** (*Input*) - Positive power supply for the headphone amplifier. Refer to "Recommended Operating Conditions" for appropriate voltages.
$\overline{\text{RST}}$	23	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low. The control port cannot be accessed when Reset is low. See Section 6.5
Control Port Definitions		
SCL/CCLK	9	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to VL in Two-Wire mode.

ADO/$\overline{CS}$	10	**Address Bit 0 (Two-Wire) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin Two-Wire mode; $\overline{CS}$ is used to enable the control port interface.
AD1/CDOUT	15	**AD1/CDOUT - Address Bit 1 (Two Wire) / Serial Control data out (SPI)** (*Input/Output*) - In Two- Wire mode, AD1 is a chip address pin. In SPI mode, CDOUT is the output data from the control port interface.
SDA/CDIN	16	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in Two-Wire mode and requires an external pull-up resistor to the logic interface voltage. CDIN is the input data line for the control port interface in SPI mode.
Stand Alone Definitions		
DIF0 DIF1	9 10	**Digital Interface Format** (I*nput*) - The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed below .

DIF1	DIF0	DESCRIPTION	FIGURE
0	0	Left Justified, up to 24-bit data	19
0	1	Right Justified, 24 -bit Data	20
1	0	I^2S, up to 24-bit data	21
1	1	Right Justified, 16-bit Data	22

Table 15. Digital Interface Format - DIF1 and DIF0

AD1/CDOUT	15	**Non-applicable** *(input)* - non-functional in this mode should be connected to ground.
DEM	16	**De-emphasis Control** (*Input*) - Selects the standard 15 µs/50 µs digital de-emphasis filter response at 44.1 kHz sample rates. NOTE: De-emphasis is not available in Double or Quad Speed Modes. When DEM is grounded, de-emphasis is disabled.

6. APPLICATIONS

6.1 Grounding and Power Supply Decoupling

As with any switching converter, the CS44210 requires careful attention to power supply and grounding arrangements to optimize performance. Figures 4 and 5 show the recommended power arrangement with VD, VA_HPx, and VL connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be used on each supply pin.

6.2 Clock Modes

One of the characteristics of a PWM amplifier is that the frequency content of out-of-band noise generated by the modulator is dependent on the PWM switching frequency. The systems designer will specify the external filter based on this switching frequency. The obvious implementation in a digital PWM system is to directly lock the PWM switching rate to the incoming data sample rate. However, this would require a tuneable filter to attentuate the switching frequency across the range of possible sample rates. To simplify the external filter design and to accommodate sample rates ranging from 8 kHz to 96 kHz the CS44210 Controller uses several clock modes that keep the PWM switching frequency in a small range.

In control port mode, for operation at a particular sample rate the user selects register settings (refer to Section 4.9 and Tables 11 and 13) based on their MCLK and MCLK/LRCK parameters. When using Stand-Alone mode, refer to Tables 12 and 14 for available clock modes.

6.3 De-Emphasis

The CS44210 includes on-chip digital de-emphasis. Figure 7 shows the de-emphasis curve. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

The de-emphasis feature is included to accommodate older audio recordings that utilize pre-emphasis equalization as a means of noise reduction.

6.4 PWM PopGuard Transient Control

The CS44210 uses PopGuard® technology to minimize the effects of output transients during power-up and power-down. This technique minimizes the audio transients commonly produced by single-ended, single-supply converters when it is implemented with external DC-blocking capacitors connected in series with the audio outputs.

When the device is initially powered-up, the DRIVER_x, and HP_x outputs are clamped to GND. Following a delay each output begins to increase the PWM duty cycle toward the quiescent voltage point. By a speed set by the RMP_SP bit, the DRIVER_x and HP_x outputs will later reach the bias point (50% PWM duty cycle), and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitor to charge to the quiescent voltage, minimizing the power-up transient.

To prevent transients at power-down, the device must first enter its power-down state. When this occurs, audio output ceases and the PWM duty cycle is decreased until the DRIVER_x and HP_x outputs reach GND. The time required to reach GND is determined by the RMP_SP bits. This allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off, and the system is ready for the next power-on.

To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning off the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to GND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance and the output load. For example, with a 220 µF capacitor

and a 16 ohm load on the headphone outputs, the minimum power-down time will be approximately 0.4 seconds.

Note that ramp up and ramp down period can be set to zero with the RUPBYP and RDNBYP bits respectively.

6.5 Recommended Power-up Sequence

6.5.1 Stand Alone Mode

1. Hold $\overline{\text{RST}}$ low until the power supply, master, and left/right clocks are stable. In this state, the control port is reset to its default settings and the HP_x and DRIVER_x lines will remain low.

2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state and will initiate the Stand-Alone power-up sequence. The control port will be accessible at this time.

6.5.2 Control Port Mode

1. Hold $\overline{\text{RST}}$ low until the power supply, master, and left/right clocks are stable. In this state, the control port is reset to its default settings and the HP_x and DRIVER_x lines will remain low.

2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state and will initiate the Stand-Alone power-up sequence. The control port will be accessible at this time.

3. On the CS44210 the control port pins are shared with stand-alone configuration pins. To enable the control port, the user must set the CP_EN bit. This is done by performing a Two-Wire or SPI write. Once the control port is enabled, these pins are dedicated to control port functionality.

To prevent audible artifacts the CP_EN bit (see Section 4.10.4) should be set prior to the completion of the Stand-Alone power-up sequence, approximately 21mS. Writing this bit will halt the Stand-Alone power-up sequence and initialize the control port to its default settings. Note, the CP_EN bit can be set any time after $\overline{\text{RST}}$ goes high; however, setting this bit after the Stand-Alone power-up sequence has completed can cause audible artifacts.

7. CONTROL PORT INTERFACE

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The CS44210 has MAP auto increment capability, enabled by the INCR bit in the MAP register, which is the MSB. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set to 1, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

7.1 Format Selection

The control port has 2 formats: SPI and Two-Wire, with the CS44210 operating as a slave device.

If Two-Wire operation is desired, AD0/$\overline{CS}$ should be tied to VL or GND. If the CS44210 ever detects a high to low transition on AD0/$\overline{CS}$ after power-up and after the control port is activated, SPI format will be selected.

7.2 Two-Wire Format

In Two-Wire Format, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with a clock to data relationship as shown in Figure 8. The receiving device should send an acknowledge (ACK) after each byte received. There is no $\overline{CS}$ pin. Pins AD0 and AD1 forms the partial chip address and should be tied to VL or GND as required. The upper 6 bits of the 7-bit address field must be 001000.

Note: MCLK is required during all two-wire transactions. The Two-Wire format is compatible with the I^2C protocol.

7.2.1 Writing in Two-Wire Format

To communicate with the CS44210, initiate a START condition of the bus. Next, send the chip address. The eighth bit of the address byte is the R/$\overline{W}$ bit (low for a write). The next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. To write multiple registers, continue providing a clock and data, waiting for the CS44210 to acknowledge between each byte. To end the transaction, send a STOP condition.

7.2.2 Reading in Two-Wire Format

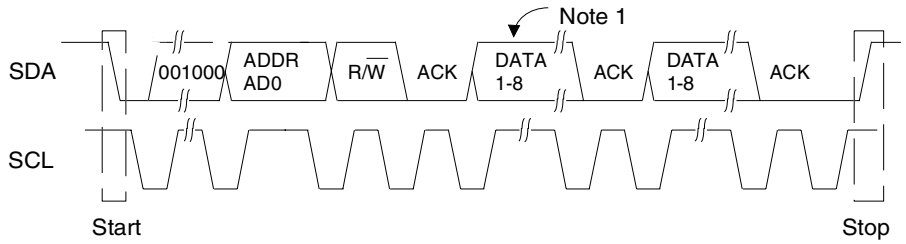
To communicate with the CS44210, initiate a START condition of the bus. Next, send the chip address. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read). The contents of the register pointed to by the MAP will be output after the chip address. To read multiple registers, continue providing a clock and issue an ACK after each byte. To end the transaction, send a STOP condition.

7.3 SPI Format

In SPI format, $\overline{CS}$ is the CS44210 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller, CDOUT is the output data line, and the chip address is 0010000. $\overline{CS}$, CCLK and CDIN are all inputs and data is clocked in on the rising edge of CCLK. CDOUT is an output and is three-stated when not actively outputting data.

7.3.1 Writing in SPI

Figure 9 shows the operation of the control port in SPI format. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into register designated by the MAP. To write multiple registers, keep $\overline{CS}$ low and continue providing clocks on CCLK. End the read transaction by setting $\overline{CS}$ high.



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 8. Control Port Timing, Two-Wire Format

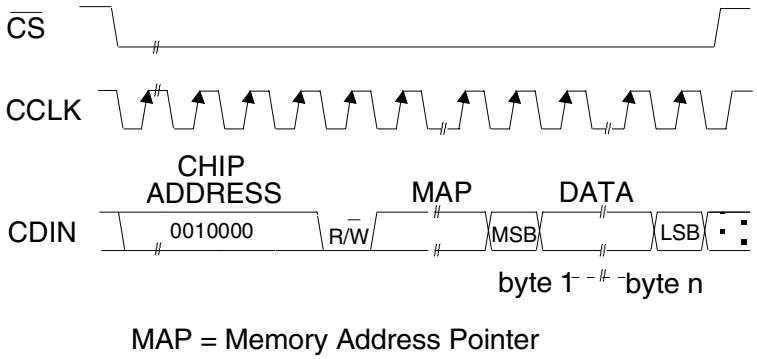


Figure 9. Control Port Timing, SPI Format (Write)

7.3.2 Reading in SPI

Figure 10 shows the operation of the control port in SPI format. To read to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be high to read. The CDOUT line will then output the data from the register designated by the MAP. To read multiple registers, keep $\overline{CS}$ low and continue providing clocks on CCLK. End the read transaction by setting $\overline{CS}$ high. The CDOUT line will tri-state once $\overline{CS}$ goes high.

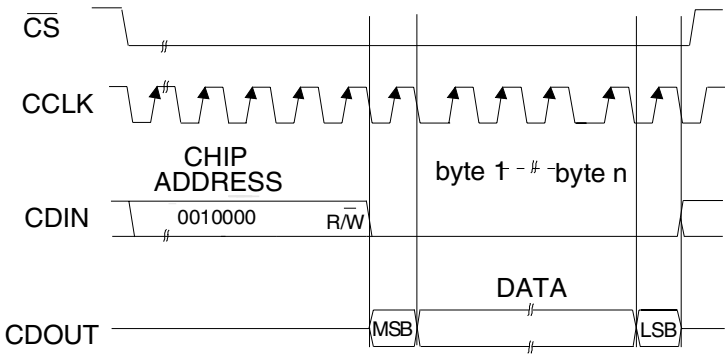


Figure 10. Control Port Timing, SPI Format (Read)

7.4 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

7.4.1 INCR (Auto Map Increment Enable)

Default = '0'
0 - Disabled
1 - Enabled

7.4.2 MAP3-0 (Memory Address Pointer)

Default = '0000'

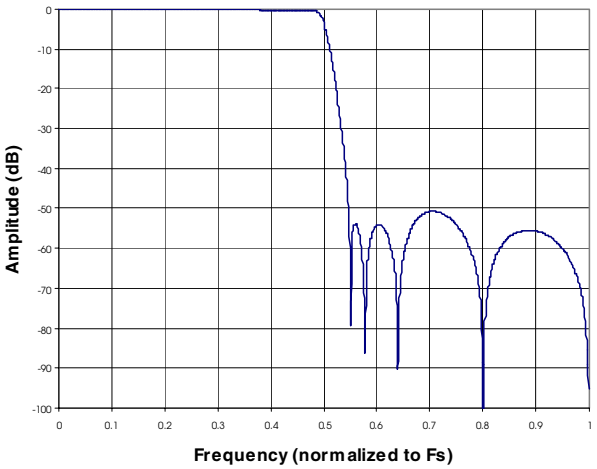


Figure 11. Single Speed Stopband Rejection

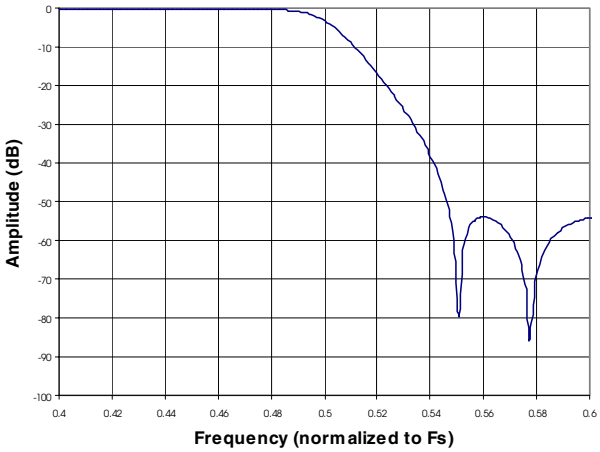


Figure 12. Single Speed Transition Band

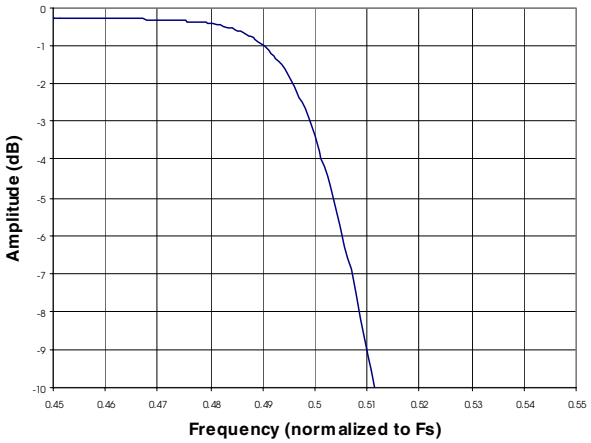


Figure 13. Single Speed Transition Band (Detail)

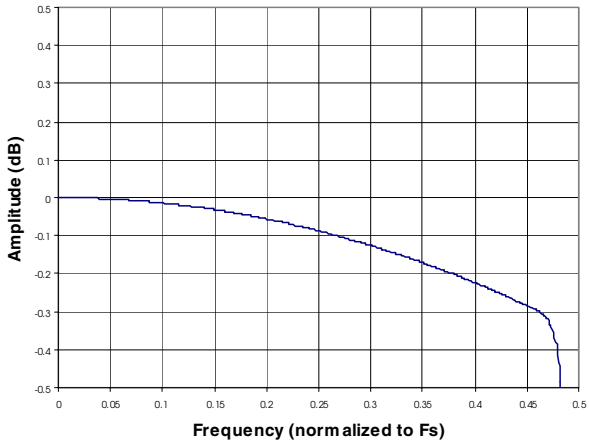


Figure 14. Single Speed Passband Ripple

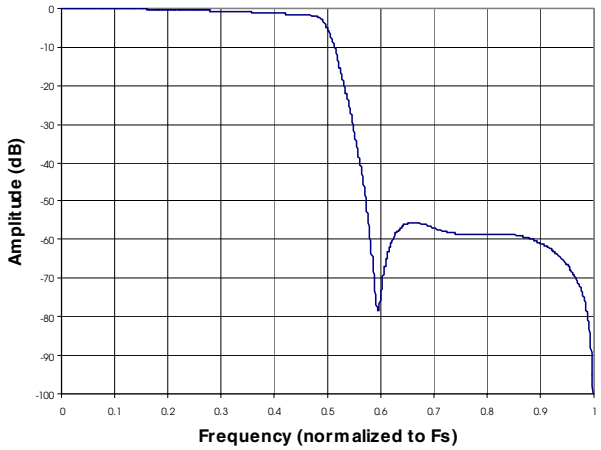


Figure 15. Double Speed Stopband Rejection

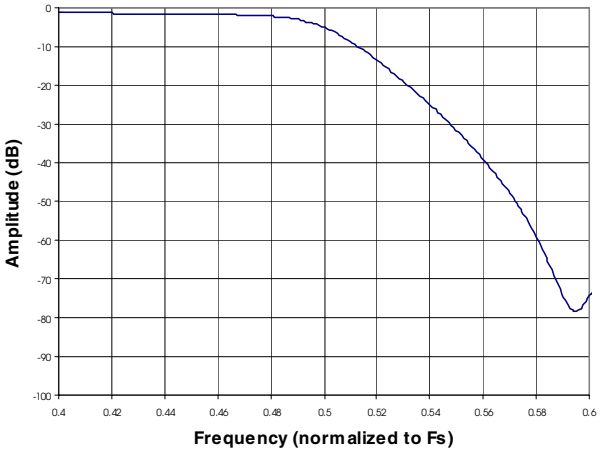


Figure 16. Double Speed Transition Band

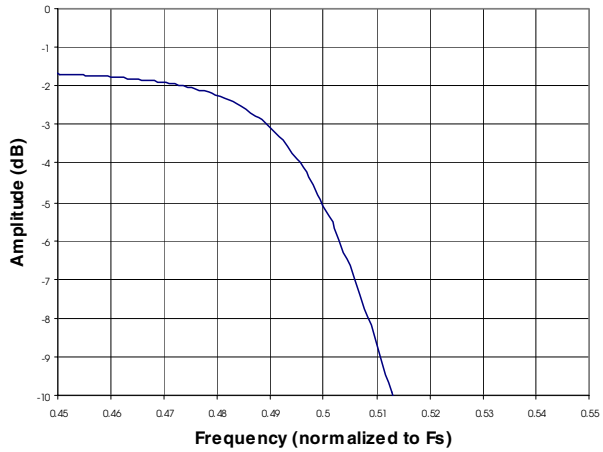


Figure 17. Double Speed Transition Band (Detail)

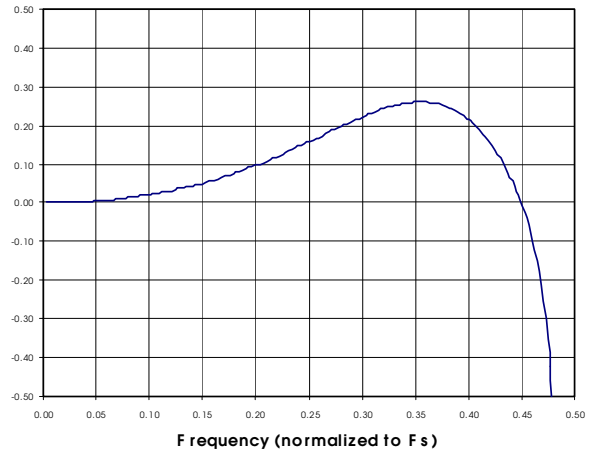


Figure 18. Double Speed Passband Ripple

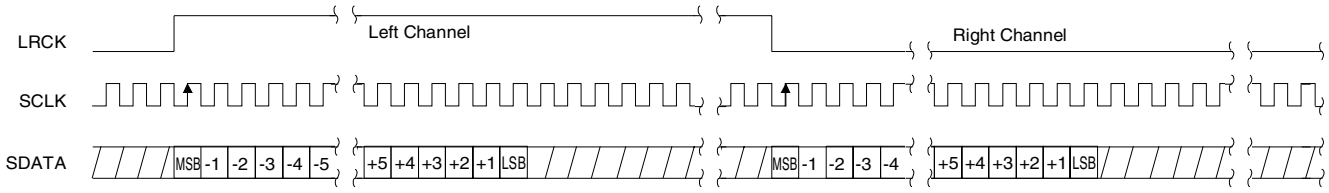


Figure 19. Left Justified, up to 24-Bit Data

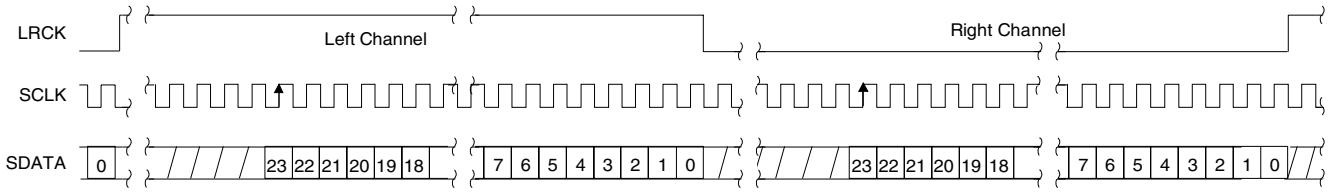


Figure 20. Right Justified, 24-Bit Data

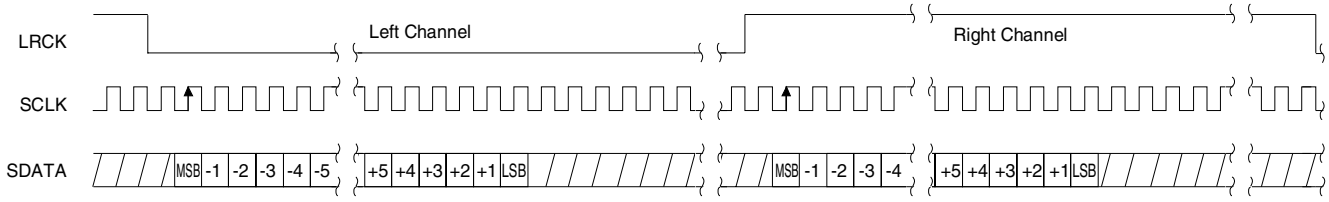


Figure 21. I^2S, Up to 24-Bit Data

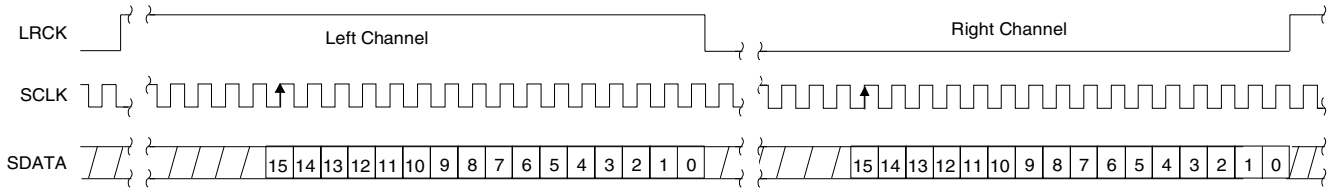


Figure 22. Right Justified, 16-Bit Data

8. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

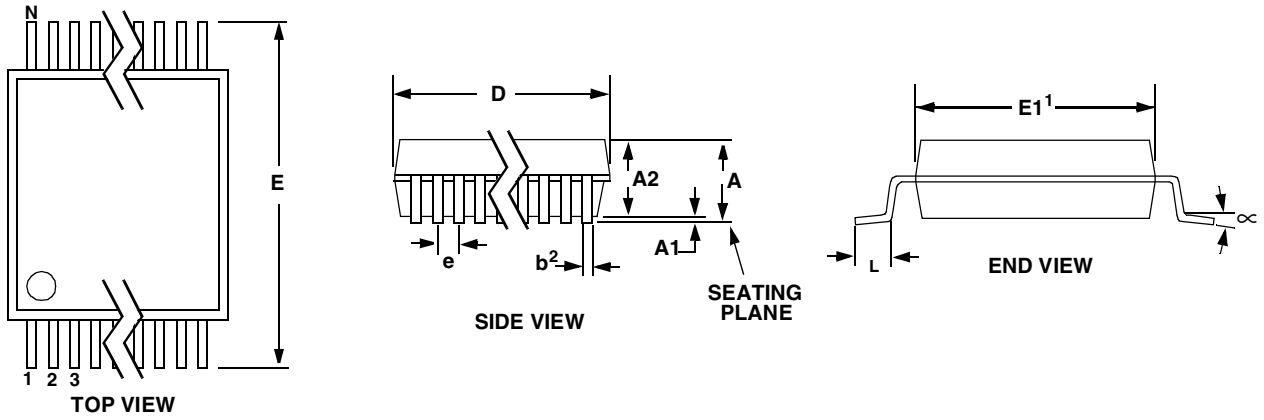
The gain difference between left and right channels. Units in decibels.

9.0 REFERENCES

1) "The I^2C-Bus Specification: Version 2.0" Philips Semiconductors, December 1998. http://www.semiconductors.philips.com

10. PACKAGE DIMENSIONS

24L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.303	0.307	0.311	7.70	7.80	7.90	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Note:

1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.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