



Pb Free Plating Product

CS48N18

70V,158A N-Channel Trench Process Power MOSFET

General Description

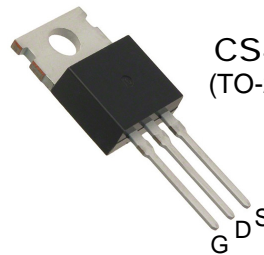
The CS48N18 is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged EAS capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching especially for E-Bike controller applications.

Features

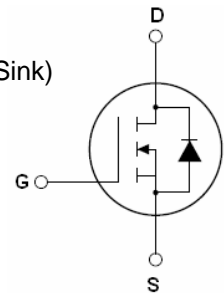
- $V_{DS}=70V$; $I_D=158A@V_{GS}=10V$;
 $R_{DS(ON)}<4.2m\Omega @V_{GS}=10V$
- Special Designed for E-Bike Controller Application
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- 48V E-Bike Controller Applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



CS48N18
(TO-220 HeatSink)



Schematic Diagram

$$V_{DSS} = 70V$$

$$I_{DSS} = 158A$$

$$R_{DS(ON)} = 3.5m\Omega$$

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	70	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 25	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	158	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	110	A
$I_{DM(pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	632	A
dv/dt	Peak Diode Recovery Voltage	30	V/ns
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	231	W
	Derating Factor	1.54	W/°C
E_{AS}	Single Pulse Avalanche Energy (Note 2)	1300	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, V_{DD}=33V, V_G=10V, I_D=72.5A$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.65	$^{\circ}C/W$

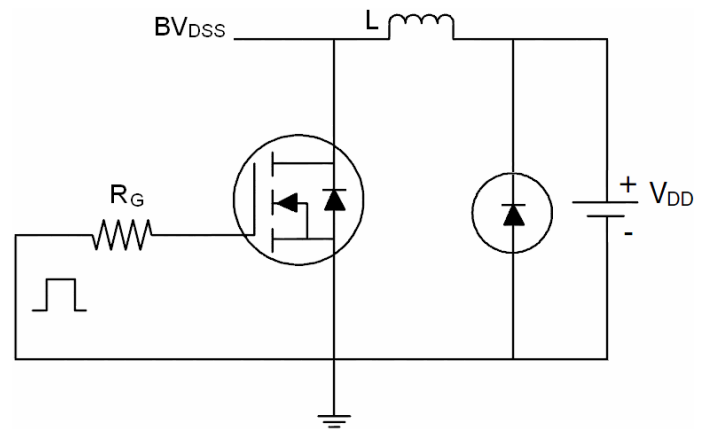
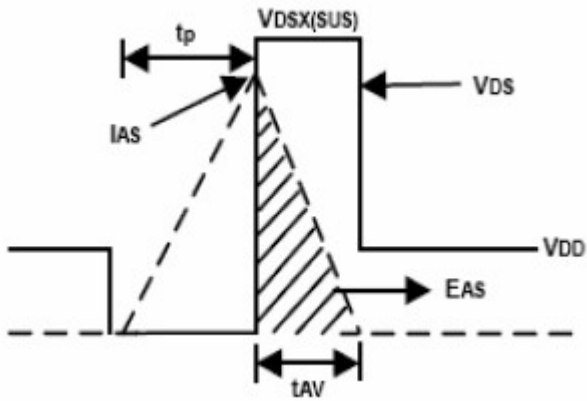
Table 3. Electrical Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	70			V
I_{DSS}	Zero Gate Voltage Drain Current($T_c=25^{\circ}C$)	$V_{DS}=68V, V_{GS}=0V$			1	μA
I_{DSS}	Zero Gate Voltage Drain Current($T_c=125^{\circ}C$)	$V_{DS}=68V, V_{GS}=0V$			1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 25V, V_{DS}=0V$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
$R_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=40A$		3.5	4.2	m Ω
Dynamic Characteristics						
g_{FS}	Forward Transconductance	$V_{DS}=10V, I_D=40A$	22			S
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0MHz$		6448		pF
C_{oss}	Output Capacitance			967		pF
C_{rss}	Reverse Transfer Capacitance			492		pF
Q_g	Total Gate Charge	$V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$		150		nC
Q_{gs}	Gate-Source Charge			28		nC
Q_{gd}	Gate-Drain Charge			40		nC
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$		24		nS
t_r	Turn-on Rise Time			28		nS
$t_{d(off)}$	Turn-Off Delay Time			50		nS
t_f	Turn-Off Fall Time			60		nS
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current(Body Diode)			175		A
I_{SDM}	Pulsed Source-Drain Current(Body Diode)			700		A
V_{SD}	Forward on Voltage (Note 1)	$T_J=25^{\circ}C, I_{SD}=40A, V_{GS}=0V$		0.8	0.95	V
t_{rr}	Reverse Recovery Time (Note 1)	$T_J=25^{\circ}C, I_F=75A$ $di/dt=100A/\mu s$		90		nS
Q_{rr}	Reverse Recovery Charge (Note 1)			180		nC
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

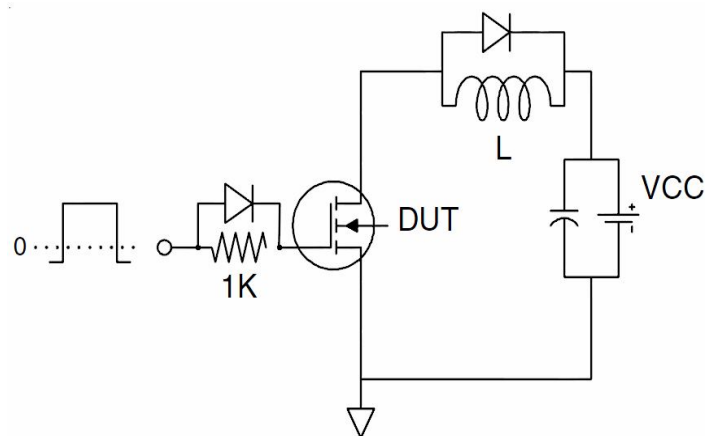
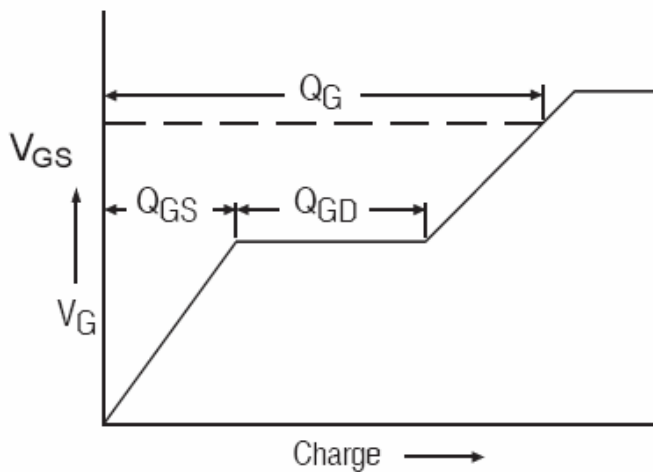
Notes 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1.5\%$, $R_G=25\Omega$, Starting $T_J=25^{\circ}C$

Test Circuit

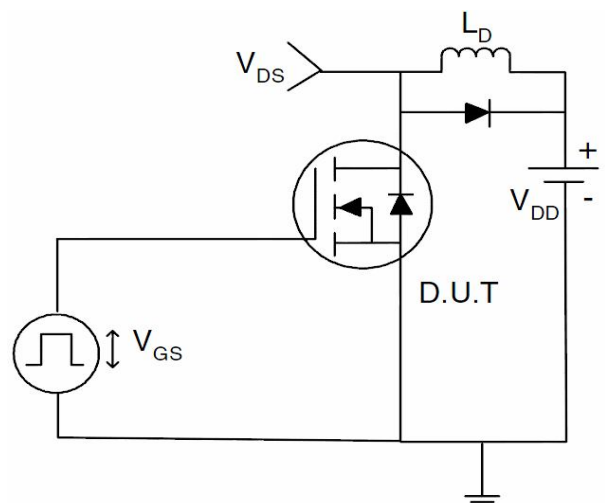
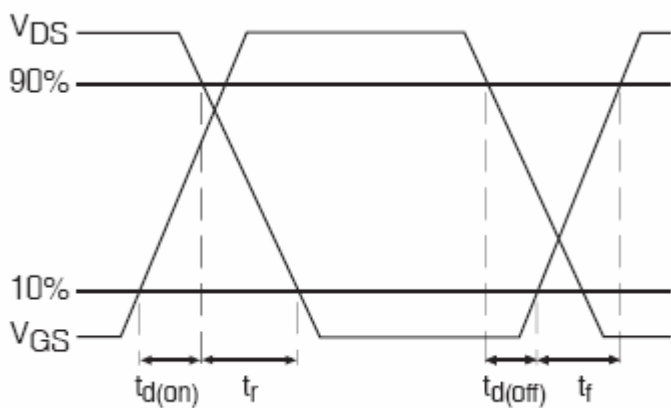
1) E_{AS} Test Circuits



2) Gate charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Safe Operating Area

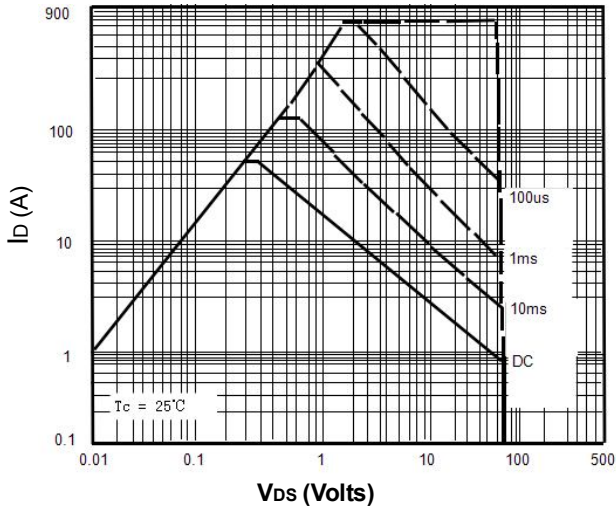


Figure2. Source-Drain Diode Forward Voltage

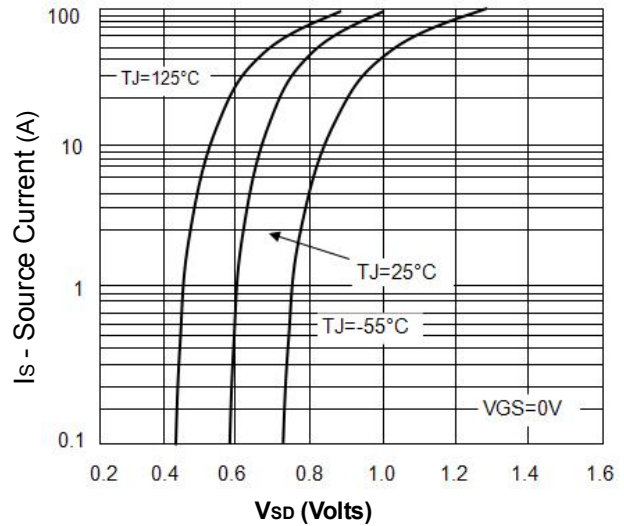


Figure3. Output Characteristics

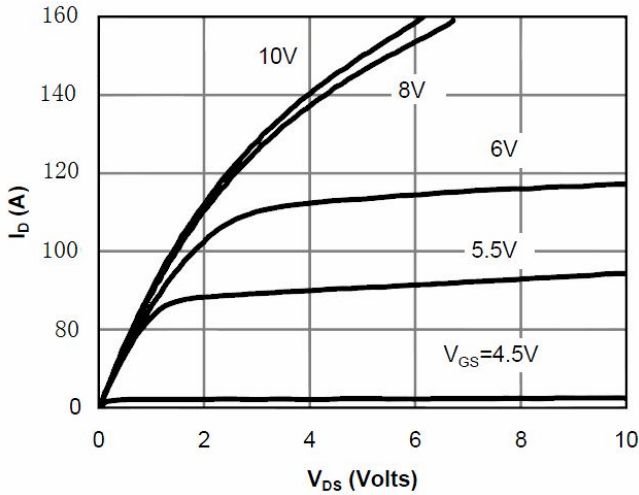


Figure4. Transfer Characteristics

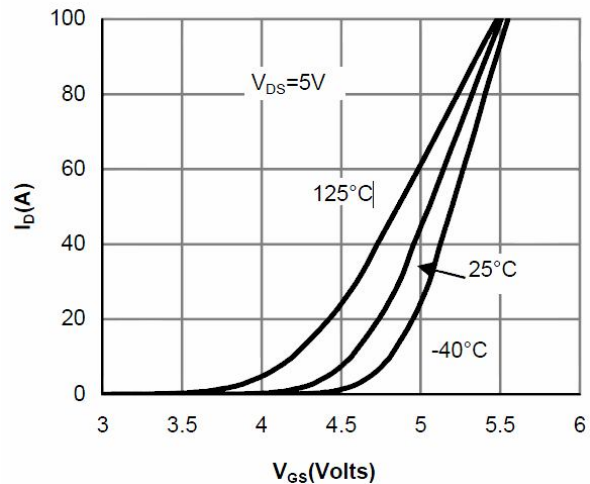


Figure5. Static Drain-Source On Resistance

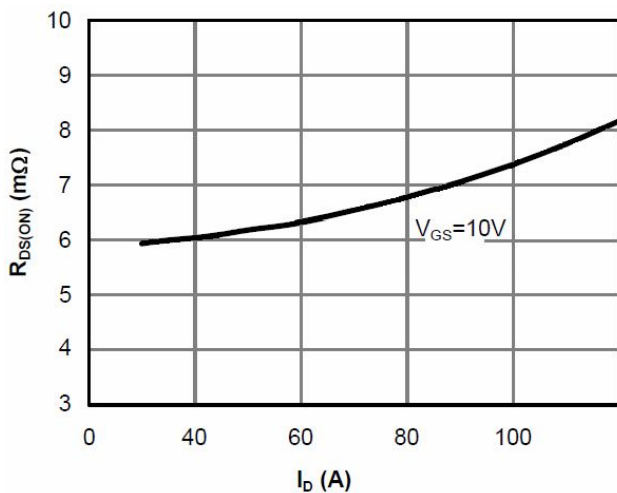


Figure6. RDS(ON) vs Junction Temperature

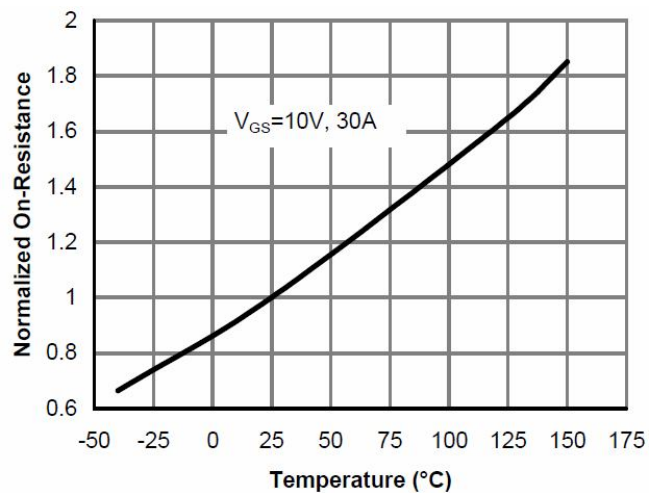


Figure7. BV_{DSS} vs Junction Temperature

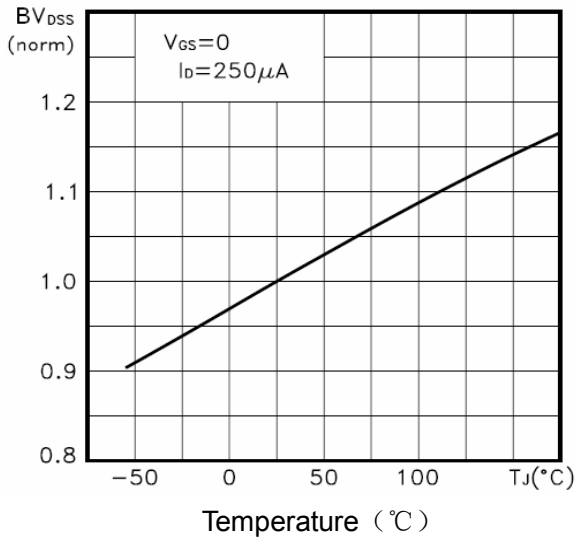


Figure8. $V_{GS(th)}$ vs Junction Temperature

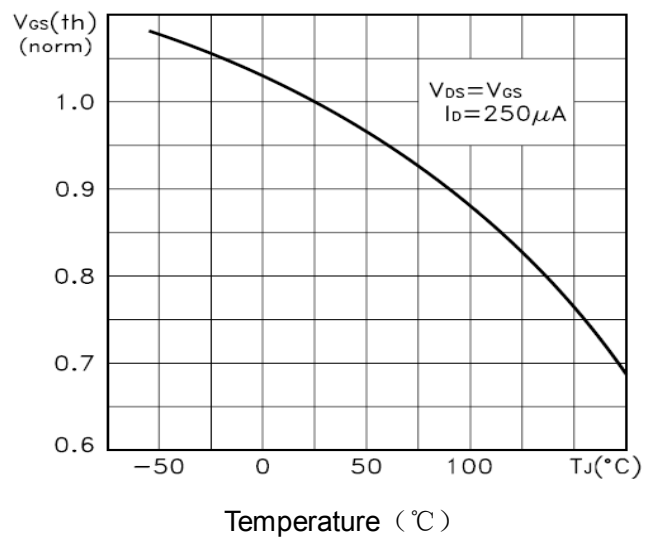


Figure9. Gate Charge Waveforms

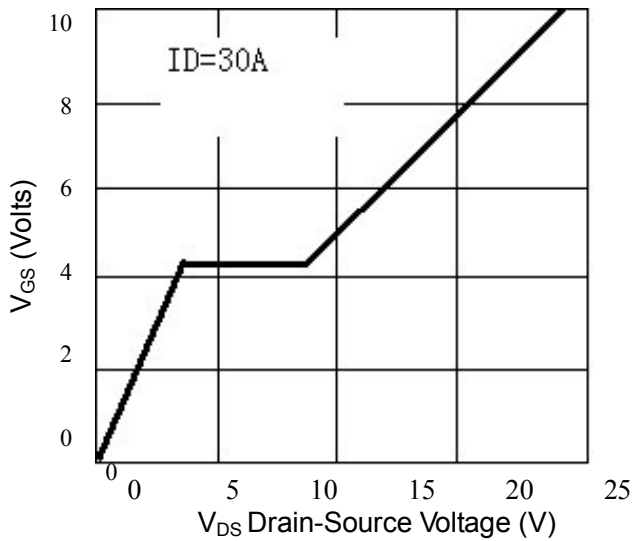


Figure10. Capacitance

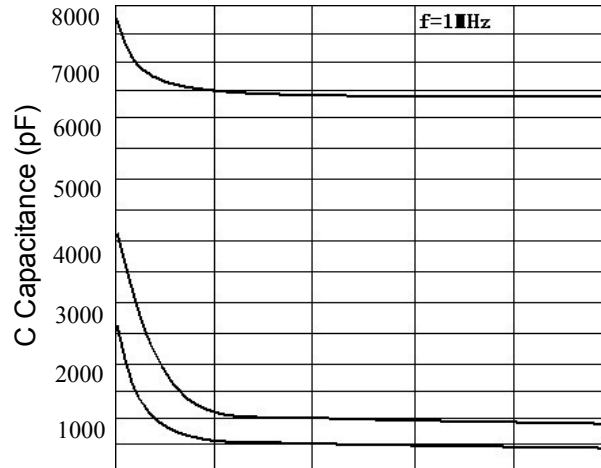
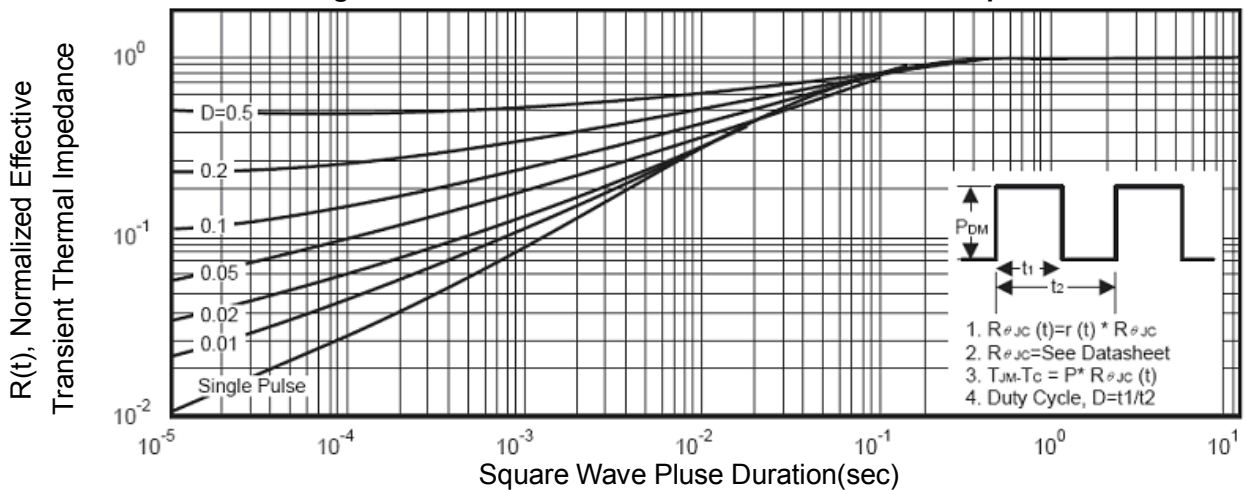


Figure11. Normalized Maximum Transient Thermal Impedance



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