



CS4N60 A4TDY

General Description:

CS4N60 A4TDY, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-252, which accords with the RoHS standard.

Features:

- I Fast Switching
- I ESD Improved Capability
- I Low Gate Charge (Typical Data: 13nC)
- I Low Reverse transfer capacitances(Typical: 2.2pF)
- I 100% Single Pulse avalanche energy Test

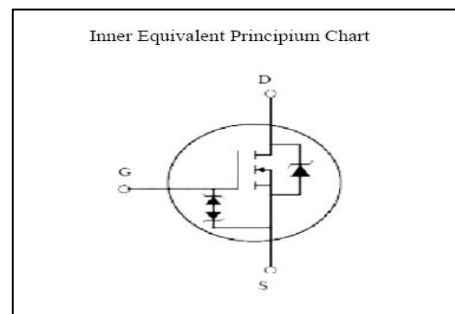
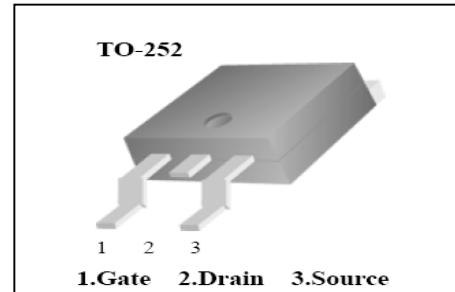
Applications:

Power switch circuit of adaptor and charger.

Absolute (Tc= 25°C unless otherwise specified):

Symbol	Parameter	Rating	Units
V _{DSS}	Drain-to-Source Voltage	600	V
I _D	Continuous Drain Current	4	A
	Continuous Drain Current T _C = 100 °C	3.2	A
I _{DM} ^{a1}	Pulsed Drain Current	16	A
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS} ^{a2}	Single Pulse Avalanche Energy	200	mJ
E _{AR} ^{a1}	Avalanche Energy ,Repetitive	30	mJ
I _{AR} ^{a1}	Avalanche Current	2.5	A
dv/dt ^{a3}	Peak Diode Recovery dv/dt	5.0	V/ns
P _D	Power Dissipation	75	W
	Derating Factor above 25°C	0.60	W/°C
V _{ESD(G-S)}	Gate source ESD (HBM-C= 100pF, R=1.5kΩ)	3000	V
T _J , T _{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	°C
T _L	Maximum Temperature for Soldering	300	°C

V _{DSS}	600	V
I _D	4	A
P _D (T _C =25°C)	75	W
R _{DS(ON)Typ}	2.0	Ω





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Electrical Characteristics (Tc= 25°C unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	600	--	--	V
$\Delta BV_{DSS}/\Delta T_j$	Bvdss Temperature Coefficient	$ID=250\mu A, \text{Reference } 25^\circ C$	--	0.6	--	V/°C
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=600V, V_{GS}=0V, T_a=25^\circ C$	--	--	1	μA
		$V_{DS}=480V, V_{GS}=0V, T_a=125^\circ C$	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20V$	--	--	10	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20V$	--	--	-10	μA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=2A$	--	2.0	2.5	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Trans conductance	$V_{DS}=15V, I_D=2A$		3.5	--	S
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$	--	554		pF
C_{oss}	Output Capacitance		--	50		
C_{rss}	Reverse Transfer Capacitance		--	2.2		

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=4A, V_{DD}=300V, R_G=10\Omega$	--	14	--	ns
t_r	Rise Time		--	13	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	32	--	
t_f	Fall Time		--	8	--	
Q_g	Total Gate Charge	$I_D=4A, V_{DD}=480V, V_{GS}=10V$	--	13		nC
Q_{gs}	Gate to Source Charge		--	2.7		
Q_{gd}	Gate to Drain ("Miller") Charge		--	5.5		



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Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	4	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	16	A
V_{SD}	Diode Forward Voltage	$I_S=4.0A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=4.0A, T_J = 25^\circ C$	--	250	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt=100A/us, V_{GS}=0V$	--	1180	--	nC
Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	1.67	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	62.5	$^\circ C/W$

Gate-source Zener diode						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{GSO}	Gate-source breakdown voltage	$I_{GS} = \pm 1mA (Open Drain)$	30			V
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.						

^{a1}: Repetitive rating; pulse width limited by maximum junction temperature

^{a2}: $L=10mH, I_D=6.3A, Start T_J=25^\circ C$

^{a3}: $I_{SD}=4A, di/dt \leq 100A/us, V_{DD} \leq BV_{DS}, Start T_J=25^\circ C$

Characteristics Curve:

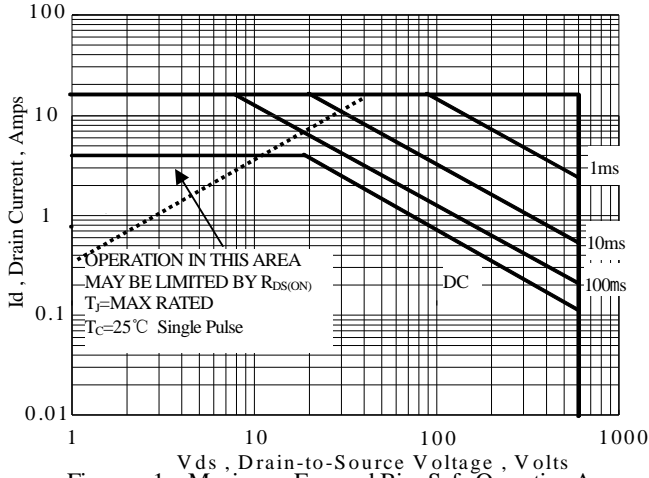


Figure 1 Maximum Forward Bias Safe Operating Area

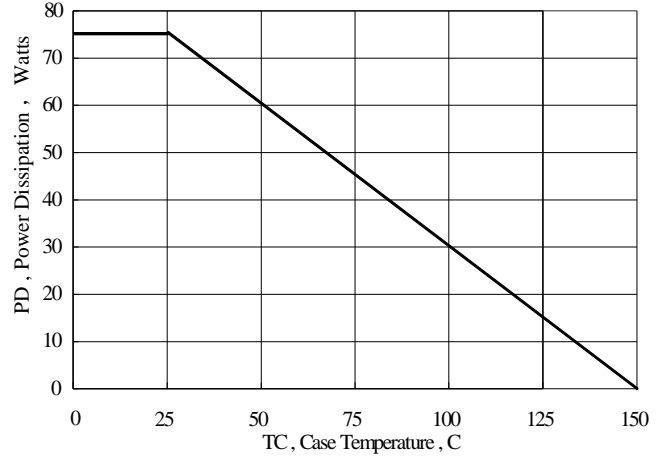


Figure 2 Maximum Power Dissipation vs Case Temperature

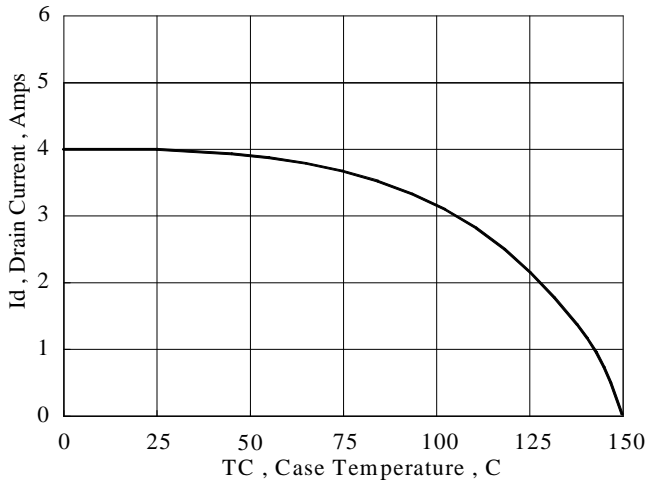


Figure 3 Maximum Continuous Drain Current vs Case Temperature

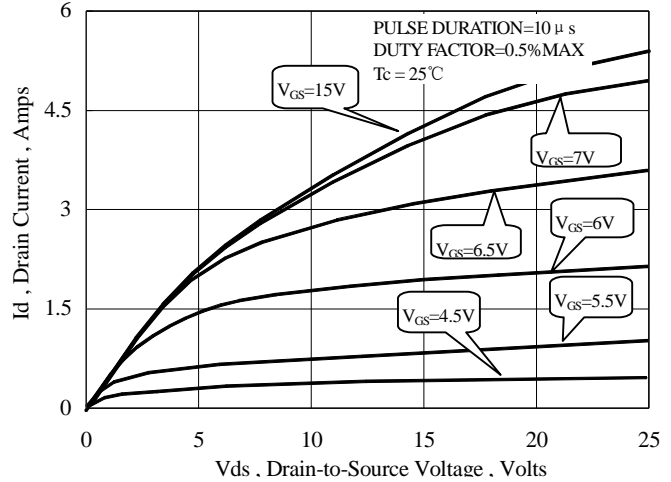


Figure 4 Typical Output Characteristics

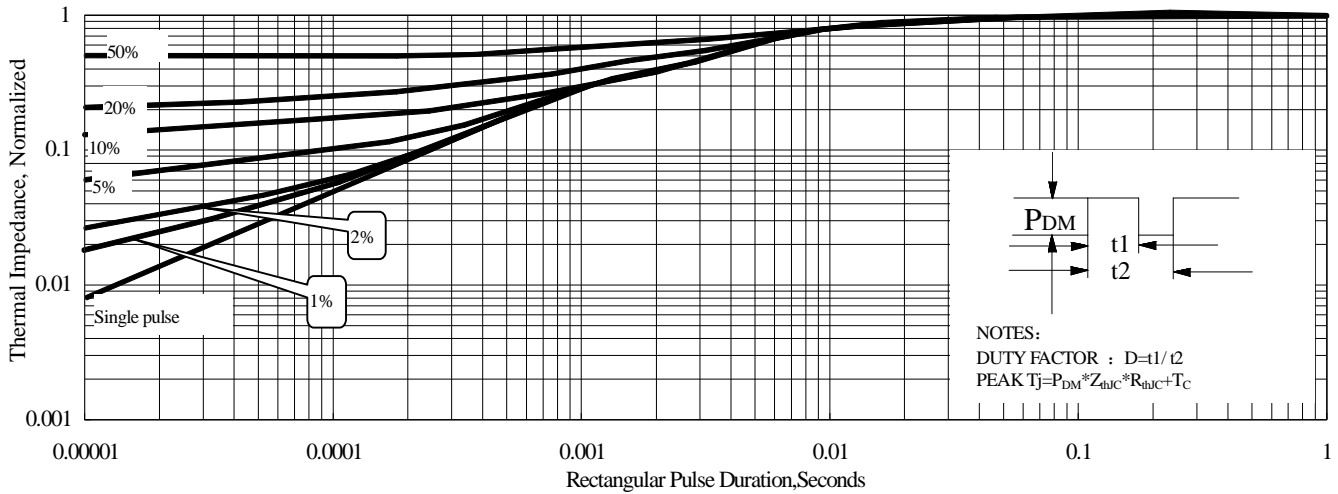


Figure 5 Maximum Effective Thermal Impedance, Junction to Case



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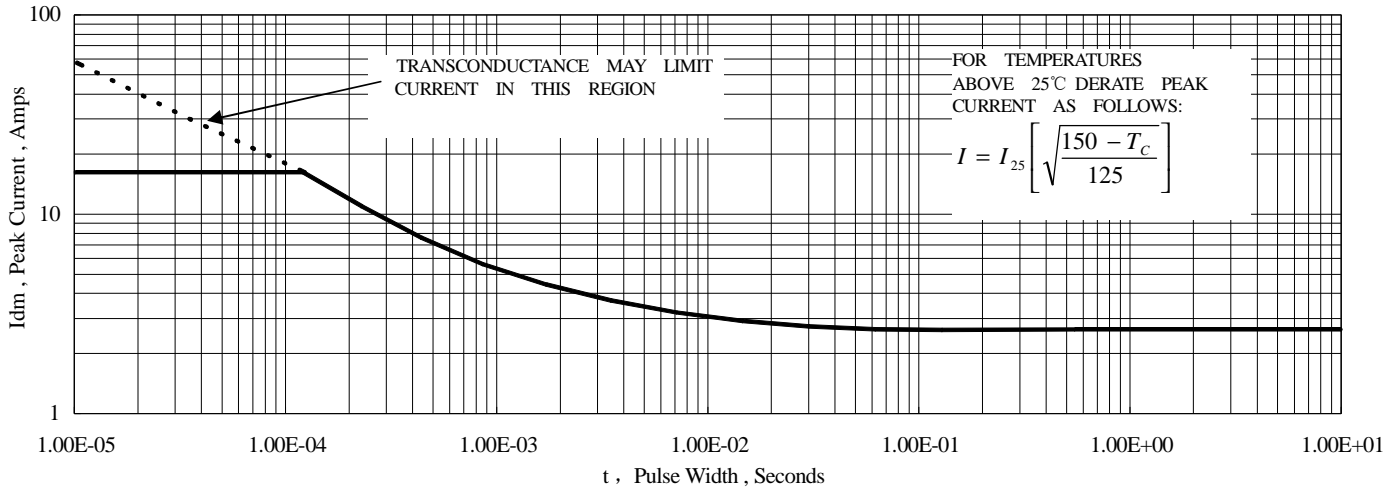


Figure 6 Maximum Peak Current Capability

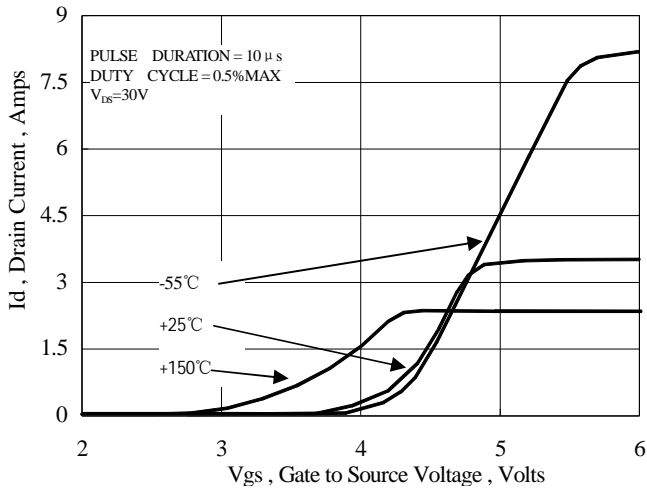


Figure 7 Typical Transfer Characteristics

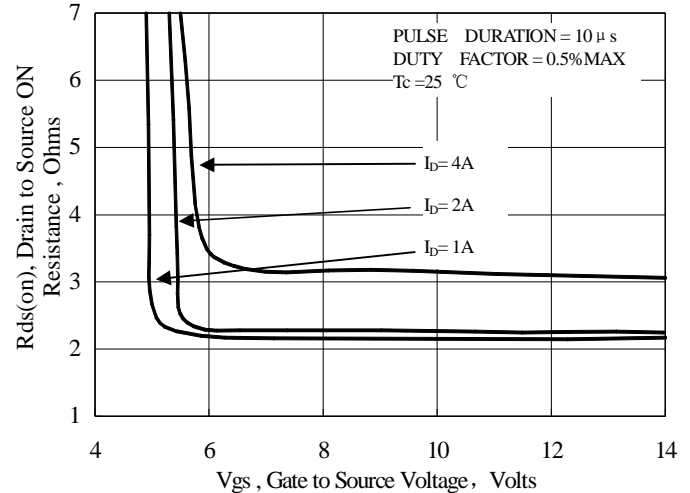


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

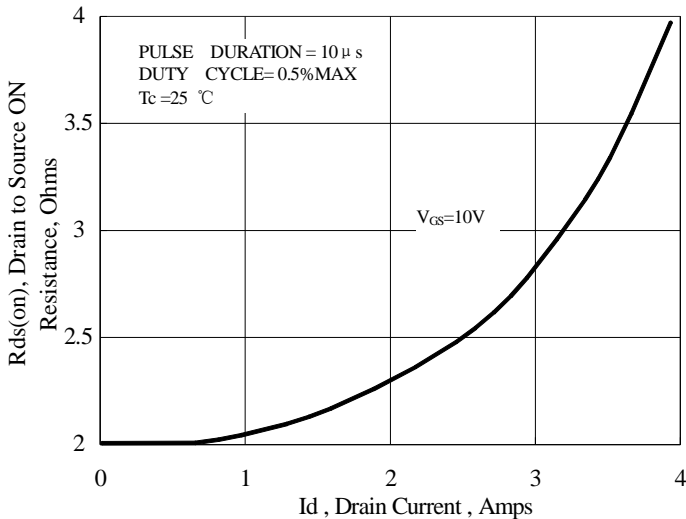


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

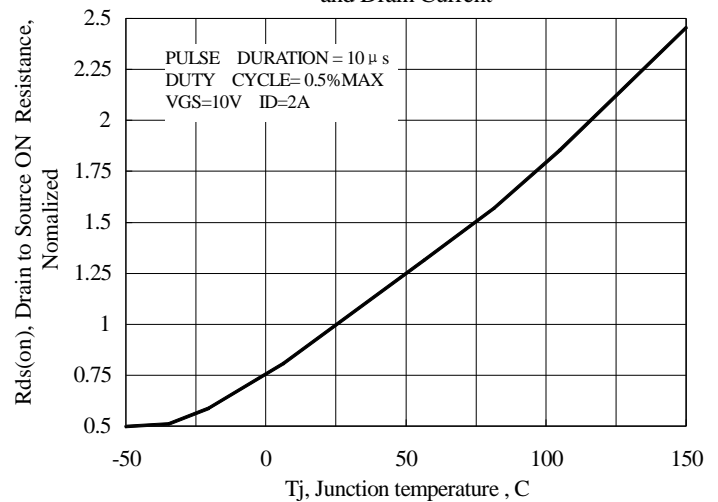


Figure 10 Typical Drain to Source on Resistance vs Junction Temperature

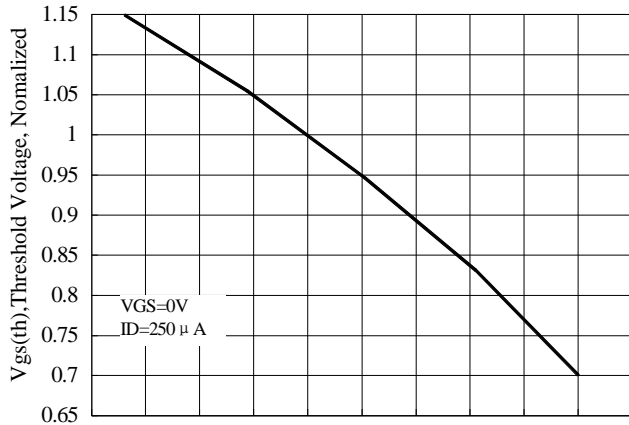


Figure 11 Typical Threshold Voltage vs Junction Temperature
Tj, Junction temperature, °C

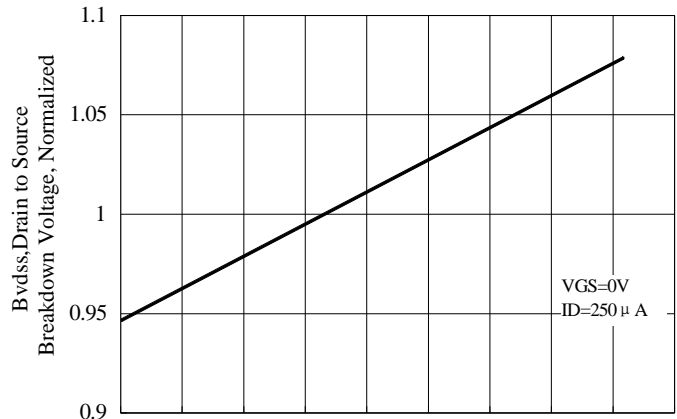


Figure 12 Typical Breakdown Voltage vs Junction Temperature
Tj, Junction temperature, °C

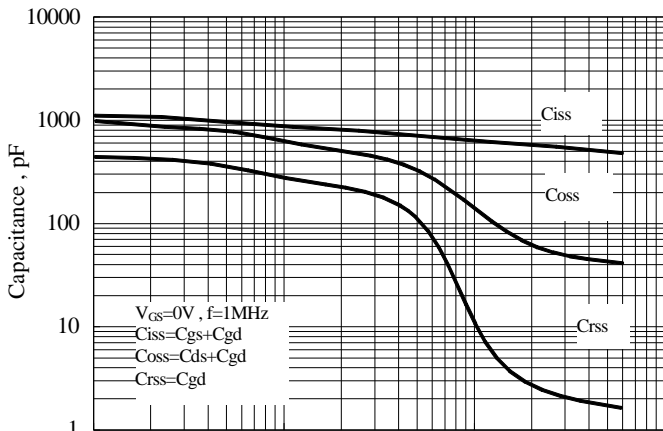


Figure 13 Typical Capacitance vs Drain to Source Voltage

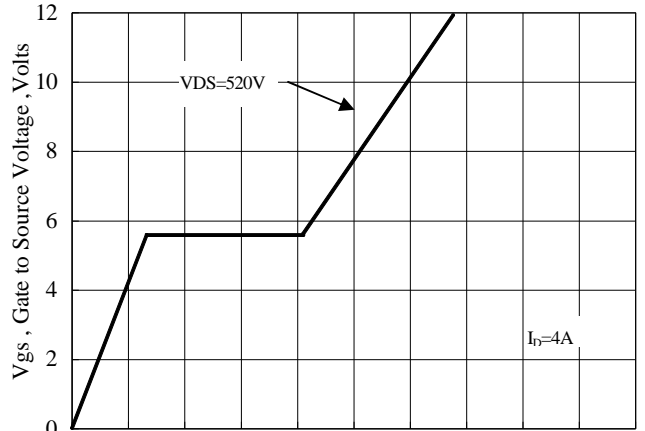


Figure 14 Typical Gate Charge vs Gate to Source Voltage
Qg, Total Gate Charge, nC

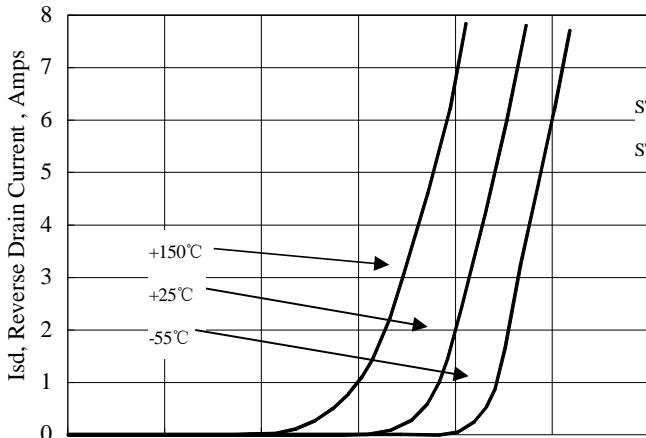


Figure 15 Typical Body Diode Transfer Characteristics
Vsd, Source - Drain Voltage, Volts

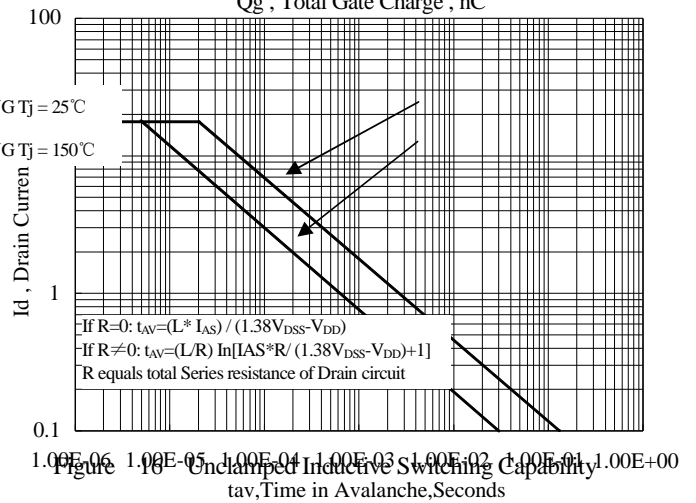


Figure 16 Unclamped Inductive Switching Capability
tAV, Time in Avalanche, Seconds

Test Circuit and Waveform

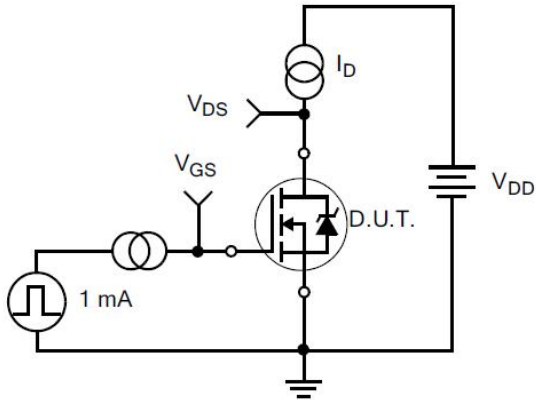


Figure 17. Gate Charge Test Circuit



Figure 18. Gate Charge Waveform



Figure 19. Resistive Switching Test Circuit



Figure 20. Resistive Switching Waveforms

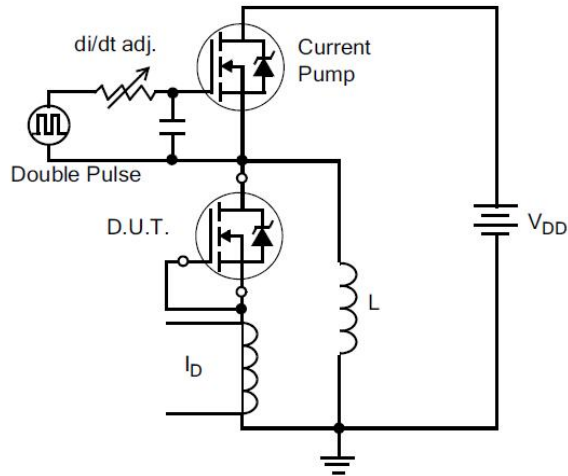


Figure 21. Diode Reverse Recovery Test Circuit

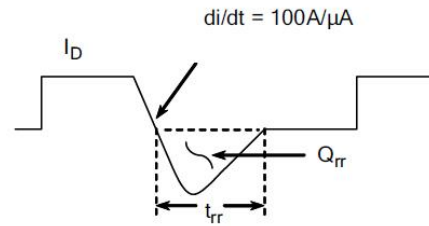


Figure 22. Diode Reverse Recovery Waveform

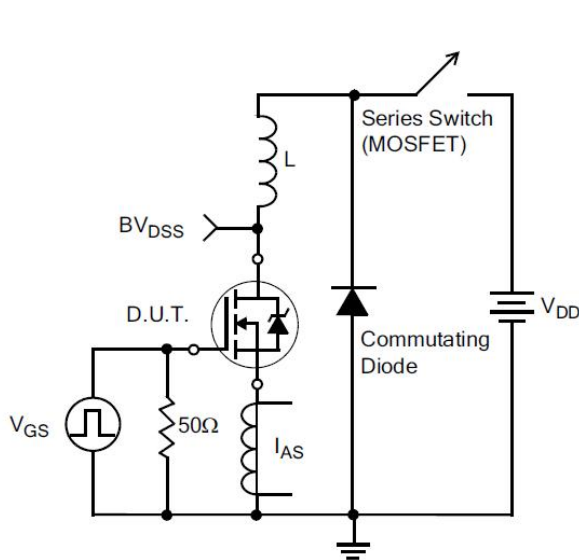


Figure 23. Unclamped Inductive Switching Test Circuit

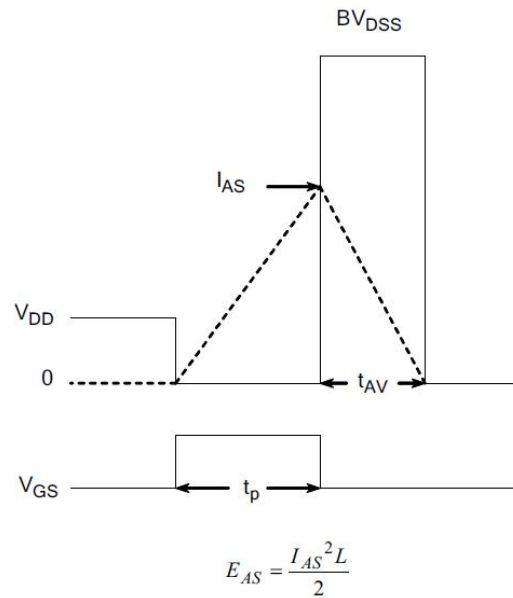
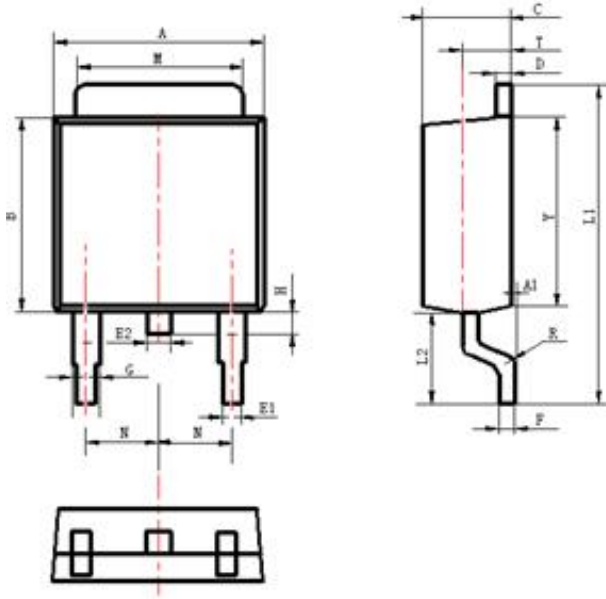


Figure 24. Unclamped Inductive Switching Waveforms

Package Information:



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.13
B	5.70	6.30
C	2.10	2.50
D	0.30	0.60
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.00
L1	9.60	10.30
L2	2.70	3.10
H	0.60	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package

