

High Performance, Integrated Current Mode PWM Controllers

Description

The CS5124/6 is a fixed frequency current mode controller designed specifically for DC-DC converters found in the telecommunications industry. The CS5124/6 integrates many commonly required current mode power supply features and allows the power supply designer to realize substantial cost and board space savings. The product matrix is as follows:

CS5124: 400kHz w/ V_{BIAS} Pin,
195mV first current sense threshold
CS5126: 200kHz w/ $SYNC$ Pin,
335mV first current sense threshold

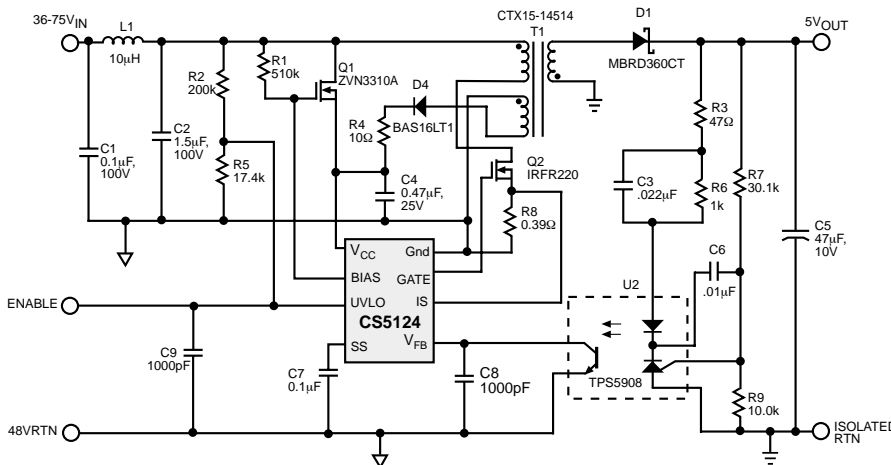
The CS5124/6 integrates the following features: Internal Oscillator, Slope Compensation, Sleep On/Off, Under Voltage Lock Out, Thermal Shutdown, Soft Start Timer, Low Voltage Current Sense for Resistive Sensing, Second Current Threshold for Pulse by Pulse Over Current Protection, a Direct Optocoupler Interface and Leading Edge Current Blanking.

The CS5124/6 has supply range of 7.7V to 20V and is available in 8 pin SO narrow package.

Features

- Line UVLO Monitoring
- Low Current Sense Voltage for Resistive Current Sensing
- External Synchronization to Higher or Lower Frequency Oscillator (CS5126 Only)
- Bias for Start up Circuitry (CS5124 Only)
- Thermal Shutdown
- Sleep On/Off Pin
- Soft Start Timer
- Leading Edge Blanking
- Direct Optocoupler Interface
- 90ns Propagation Delay
- 35ns Driver Rise and Fall Times
- Sleep Mode

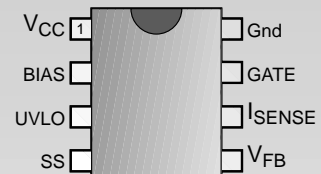
Applications Diagram



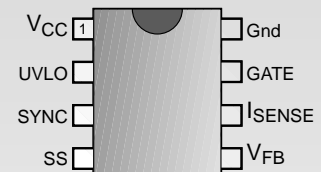
48V to 5V, 1A flyback converter using the CS5124

Package Options

8 Lead SO Narrow
CS5124



CS5126



Absolute Maximum Ratings

Pin Symbol	Lead Name	V _{MAX}	V _{MIN}	I _{SOURCE}	I _{SINK}
V _{CC}	V _{CC} Power Input	20V	-0.3V	1mA	1.5A Peak 200mA DC
SYNC (CS5126)	Clock Synchronization Input	20V	-0.3V	1mA	1mA
V _{BIAS} (CS5124)	V _{CC} Clamp Output	20V	-0.3V	1mA	1mA
UVLO	UVLO Shutdown Input	6V	-0.3V	1mA	1mA
SS	Soft Start Capacitor Input	6V	-0.3V	1mA	2mA
V _{FB}	Voltage Feed Back Input	6V	-0.3V	3mA	20mA
I _{SENSE}	Current Sense Input	6V	-0.3V	1mA	1mA
GROUND	Ground	0V	0V	1.5A peak 200mA DC	1mA
GATE	Gate Drive Output	20V	-0.3V	1.5A Peak 200mA DC	1.5A Peak 200mA DC

Operating Junction Temperature, T_J -40 to 135°C

Storage Temperature Range, T_S -40 to 150°C

ESD (Human Body Model) 2kV

ESD (Machine Model) 200V

Lead Temperature Soldering:

Reflow (SMD styles only)60 sec. max above 183°C, 230°C peak

Electrical Characteristics: -40°C ≤ T_J ≤ 125°C, -40°C ≤ T_A ≤ 105°C, 7.60V ≤ V_{CC} ≤ 20V, UVLO = 3.0V, I_{SENSE} = 0V,
C_{V(CC)} = 0.33μF, C_{GATE} = 1nF (ESR = 10Ω), C_{SS} = 470pF C_{V(FB)} = 100pF, unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ General					
I _{CC} Operating - V _{GATE} not switching.			10	13	mA
I _{CC} at V _{CC} Low	V _{CC} = 6V		500	750	μA
I _{CC} Sleep	V _{UVL} = 1V		210	275	μA
■ Low V_{CC} Lockout					
V _{CC} Turn-on Threshold Voltage		7.2	7.7	8.3	V
V _{CC} Turn-off Threshold Voltage		6.8	7.3	7.8	V
V _{CC} Hysteresis		350	425	500	mV
■ UVLO					
Sleep Threshold Voltage	UVLO decreasing	1.5	1.8	2.3	V
Sleep Threshold Voltage	UVLO increasing		1.88	2.45	V
Sleep Hysteresis		35	85	150	mV
UVLO Turn-off Threshold Voltage	(Note 1)	2.3	2.45	2.6	V
UVLO Turn-on Threshold Voltage	(Note 1)	2.50	2.63	2.76	V
UVLO Hysteresis	Turn-on – Turnoff (-40°C ≤ T _J ≤ 100°C) (Note 1)	170	185	200	mV
UVLO Hysteresis	Turn-on – Turnoff (100°C ≤ T _J ≤ 125°C) (Note 1)	50	185	400	mV
UVLO Input Bias Current		-1		1	μA
UVLO Clamp	With UVLO sinking 1mA.	5	7.5	12	V

Electrical Characteristics: $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$, $7.60\text{V} \leq V_{CC} \leq 20\text{V}$, $\text{UVLO} = 3.0\text{V}$, $I_{\text{SENSE}} = 0\text{V}$,
 $C_{V(\text{CC})} = 0.33\mu\text{F}$, $C_{\text{GATE}} = 1\text{nF}$ (ESR = 10 Ω), $C_{\text{SS}} = 470\text{pF}$ $C_{V(\text{FB})} = 100\text{pF}$, unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ V_{CC} Clamp and BIAS Pin		CS5124 Only. Connect an NFET as follows: BIAS = G, V_{CC} = S, V_{IN} = D.			
V _{CC} Clamp Voltage	$36\text{V} \leq V_{\text{IN}} \leq 60\text{V}$, $220\text{nF} \leq C_{\text{SS}} \leq 500\text{nF}$, $R = 500\text{k}$	7.275	7.9	8.625	V
BIAS Minimum Voltage	Measure Voltage on BIAS with: $10\text{V} \leq V_{\text{CC}} \leq 20\text{V}$ and $50\mu\text{A} \leq I_{\text{BIAS}} \leq 1\text{mA}$	1.6	2.8	4	V
BIAS Clamp	With BIAS pin sinking 1mA	12	15	20	V
■ 200kHz Oscillator		CS5126 Only			
Operating Frequency		175	200	225	kHz
Max Duty Cycle Clamp		78	82.5	85	%
Slope Compensation (Normal operation)		12	18	23	mV/ μs
Slope Compensation (Synchronized operation)	(Note 1)	7	12	16	mV/ μs
SYNC Input Threshold Voltage		1	2	3	V
SYNC Input Impedance	Measured with SYNC = 1V & 10V	50	120	230	k Ω
■ 400kHz Oscillator		CS5124 Only			
Operating Frequency		360	400	440	kHz
Max Duty Cycle Clamp		80.0	82.5	85.0	%
Slope Compensation		15	21	26	mV/ μs
■ Soft Start					
Soft Start Charge Current		7	10	13	μA
Soft Start Discharge Current		0.5	10.0		mA
V _{SS} Voltage when V _{FB} begins to Rise	V _{FB} = 300mV	1.40	1.62	1.80	V
Peak Soft Start Charge Voltage		4.7	4.9		V
Valley Soft Start Discharge Voltage		200	275	400	mV
■ Current Sense		CS5124 Only			
First Current Sense Threshold	At max duty cycle.	170	195	215	mV
Second Current Sense Threshold		250	275	315	mV
I _{SENSE} to GATE Prop. Delay	0 to 700mV pulse into I _{SENSE} (after blanking time)	60	90	130	ns
Leading Edge Blanking Time	0 to 400mV pulse into I _{SENSE}	90	130	180	ns
Internal Offset	(Note 1)		60		mV
■ Current Sense		CS5126 Only			
First Current Sense Threshold	At max duty cycle	300	335	360	mV
Second Current Sense Threshold		485	525	575	mV
I _{SENSE} to GATE Prop. Delay	0 to 800mV pulse into I _{SENSE} (after blanking time)	60	90	130	ns
Leading Edge Blanking Time	0 to 550mV pulse into I _{SENSE}	110	175	210	ns
Internal Offset	(Note 1)		125		mV

Electrical Characteristics: $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$, $7.60\text{V} \leq V_{CC} \leq 20\text{V}$, $\text{UVLO} = 3.0\text{V}$, $I_{\text{SENSE}} = 0\text{V}$, $C_{V(\text{CC})} = 0.33\mu\text{F}$, $C_{\text{GATE}} = 1\text{nF}$ (ESR = 10Ω), $C_{\text{SS}} = 470\text{pF}$, $C_{V(\text{FB})} = 100\text{pF}$, unless otherwise stated.

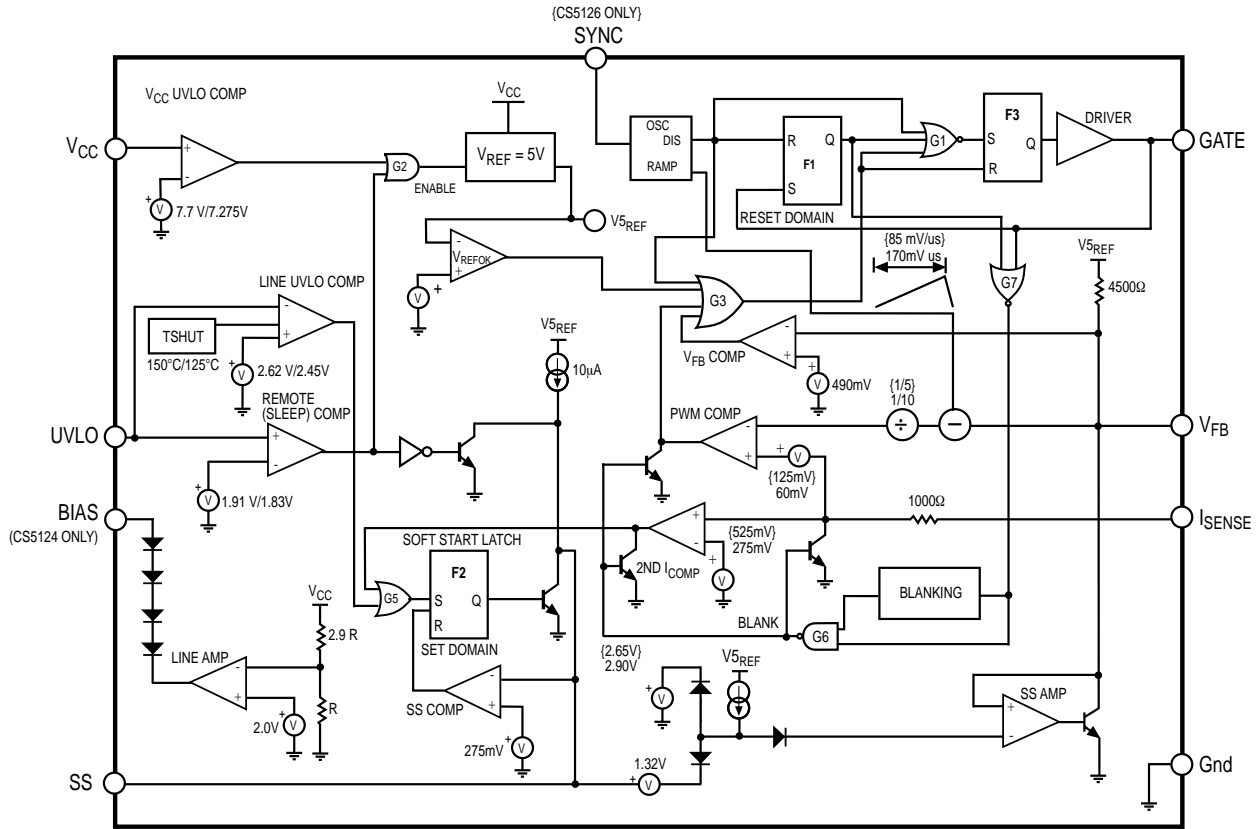
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Voltage Feedback					
V_{FB} Pull-up Res.		2.9	4.3	8.1	k Ω
V_{FB} Clamp Voltage	CS5124 Only	2.63	2.90	3.15	V
V_{FB} Clamp Voltage	CS5126 Only	2.40	2.65	2.90	V
V_{FB} Fault Voltage Threshold		460	490	520	mV
■ Output Gate Drive					
Maximum Sleep Pull-down Voltage	$V_{CC} = 6.0\text{V}$, $I_{\text{OUT}} = 1\text{mA}$		1.2	2.0	V
GATE High (AC)	Series resistance < 1Ω (Note 1)	$V_{CC}-1$	$V_{CC}-0.5$		V
GATE Low (AC)	Series resistance < 1Ω (Note 1)		0.0	0.5	V
GATE High Clamp Voltage	$V_{CC} = 20\text{V}$	11.0	13.5	16.0	V
Rise Time	Measure GATE rise time, $1\text{V} < \text{GATE} < 9\text{V}$; $V_{CC} = 12\text{V}$		45	65	ns
Fall Time	Measure GATE fall time, $9\text{V} > \text{GATE} > 1\text{V}$; $V_{CC} = 12\text{V}$		25	55	ns
■ Thermal Shutdown					
Thermal Shutdown Temperature (Note 1) (GATE low)		135	150	165	$^{\circ}\text{C}$
Thermal Enable Temperature	(Note 1) (GATE switching)	100	125	150	$^{\circ}\text{C}$
Thermal Hysteresis	(Note 1)	15	25	35	$^{\circ}\text{C}$

Notes

1. Not tested in production. Specification is guaranteed by design.

Package Lead Description

PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
8 Lead SO Narrow		
CS5124	CS5126	
1	1	V_{CC} V_{CC} Power Input Pin.
2	-	BIAS V_{CC} Clamp Output Pin. This pin will control the gate of an N-channel MOSFET that in turn regulates V_{CC} . This pin is internally clamped at 15V when the IC is in sleep mode.
-	3	SYNC Clock Synchronization Pin. A positive edge will terminate the current PWM cycle. Ground this pin when it is not used.
3	2	UVLO Sleep and under voltage lockout pin. A voltage greater than 1.8V causes the chip to "wake up" however the GATE remains low. A voltage greater than 2.6V on this pin allows the output to switch.
4	4	SS Soft Start Capacitor Pin. A capacitor placed between SS and GROUND is charged with $10\mu\text{A}$ and discharged with 10mA . The Soft Start capacitor controls both soft-start time and hiccup mode frequency.
5	5	V_{FB} Voltage Feedback Pin. The collector of an optocoupler is typically tied to this pin. This pin is pulled up internally by a $4.3\text{k}\Omega$ resistor to 5V and is clamped internally at 2.9V(2.65V). If V_{FB} is pulled $> 4\text{V}$, the oscillator is disabled and GATE will stay high. If the V_{FB} pin is pulled $< 0.49\text{V}$, GATE will stay low.
6	6	I_{SENSE} Current Sense Pin. This pin is connected to the current sense resistor on the primary side. If V_{FB} is floating, the GATE will go low if $I_{\text{SENSE}} = 195\text{mV}$ (335mV). If $I_{\text{SENSE}} > 275\text{mV}$ (525mV), Soft Start will be initiated.
7	7	GATE Gate Drive Output Pin. Capable of driving a 3nF load. GATE is nominally clamped to 13.5V.
8	8	Gnd Ground Pin.



Theory of Operation

Powering the IC

V_{CC} can be powered directly from a regulated supply and requires 500μA of start-up current. The CS5124/6 includes a line bias pin (BIAS) that can be used to control a series pass transistor for operation over a wide input voltage. The BIAS pin will control the gate voltage of an N-channel MOSFET placed between V_{IN} and V_{CC} to regulate V_{CC} at 8V.

V_{CC} and UVLO Pins

The UVLO pin has three different modes; low power shutdown, Line UVLO, and normal operation. To illustrate how the UVLO pin works; assume that V_{IN}, as shown in the application schematic, is ramped up starting at 0V with the UVLO pin open. The SS and I_{SENSE} pins also start at 0V. While the UVLO is below 1.8V, the IC will remain in a low current sleep mode and the BIAS pin of the CS5124 is internally clamped to a maximum of 15V. When the voltage on the UVLO pin rises to between 1.8V and 2.6V the reference for the V_{CC} UVLO is enabled and V_{CC} is regulated to 8V by the BIAS pin (CS5124 only), but the IC remains in a UVLO state and the output driver does not switch. When the UVLO pin exceeds 2.6V and the V_{CC} pin exceeds 7.7V, the GATE pin is released from a low state and can begin switching based on the comparison of the I_{SENSE} and V_{FB} pins. The Soft Start capacitor begins charging from 0V at

10μA. As the capacitor charges, a buffered version of the capacitor voltage appears on the V_{FB} pin and the V_{FB} voltage begins to rise. As V_{FB} rises the duty cycle increases until the supply comes into regulation.

Soft Start

Soft Start is accomplished by clamping the V_{FB} pin 1.32V below the SS pin during normal start up and during restart after a fault condition. When the CS5124/6 starts, the Soft Start capacitor is charged from a 10μA source from 0V to 4.9V. The V_{FB} pin follows the Soft Start pin offset by -1.32V until the supply comes into regulation or until the Soft Start error amp is clamped at 2.9V (2.65V for the CS5126). During fault conditions the Soft Start capacitor is discharged at 10mA.

Fault Conditions

The CS5124/6 recognizes the following faults: UVLO off, Thermal Shutdown, V_{REF(OK)}, and Second Current Threshold. Once a fault is recognized, fault latch F2 is set and the IC immediately shuts down the output driver and discharges the Soft Start capacitor. Soft Start will begin only after all faults have been removed and the Soft Start capacitor has been discharged to less than 0.275V. Each fault will be explained in the following sections.

Under Voltage Lockout (UVLO)

The UVLO pin is tied to typically the midpoint of a resistive divider between V_{IN} and GROUND. During a start up sequence, this pin must be above 2.6V in order for the IC to begin normal operation. If the IC is running and this pin is pulled below 1.8V, F2 shuts down the output driver and discharges the Soft Start capacitor in order to insure proper start-up. If the UVLO pin is pulled high again before the Soft Start capacitor discharges, the IC will complete the Soft Start discharge and, if no other faults are present, will immediately restart the power supply. If the UVLO pin stays low, then it will enter either the low current sleep mode or the UVLO state depending on the level of the UVLO pin.

Thermal Shutdown

If the IC junction temperature exceeds approximately 150°C the thermal shutdown circuit sets F2, which shuts down the output driver and discharges the Soft Start capacitor. If no other faults are present the IC will initiate Soft Start when the IC junction temperature has been reduced by 25°C.

$V_{REF(OK)}$

$V_{REF(OK)}$ is an internal monitor that insures the internal regulator is running before any switching occurs. This function does not trip the fault comparator like the other fault functions. To insure that Soft Start will occur at low line conditions the UVLO divider should be set up so that the V_{CC} UVLO comparator turns on before the LINE UVLO comparator.

Second Threshold Comparator

Since the maximum dynamic range of the I_{SENSE} signal in normal operation is 195mV (335mV for the CS5126), any voltage exceeding this threshold on the I_{SENSE} pin is considered a fault and the PWM cycle is terminated. The 2nd I_{COMP} compares the I_{SENSE} signal with a 275mV (525mV

for the CS5126) threshold. If the I_{SENSE} voltage exceeds the second threshold, F2 is set, the driver turns off, and the soft-start capacitor discharges. After the Soft Start capacitor has discharged to less than 0.275V Soft Start will begin. If the fault condition has been removed the supply will operate normally. If the fault remains the supply will operate in hiccup mode until the fault condition is removed.

V_{FB} Comparator

The V_{FB} comparator detects when the output voltage is too high. When the regulated output voltage is too high, the feedback loop will drive V_{FB} low. If V_{FB} is less than 0.49V the output of the V_{FB} comparator will go high and shut the output driver off.

Oscillator

The internally trimmed, 400kHz (CS5124) or 200kHz (CS5126) provides the slope compensation ramp as well as the pulse for enabling the output driver.

PWM Comparator and Slope Compensation

The CS5124/6 provides a fixed internal slope compensation ramp that is subtracted from the feedback signal. The pwm comparator compares peak primary current to a portion of the difference of the feedback voltage and slope compensation ramp. The 170mV/ μ s (85mV/ μ s for the CS5126) slope compensation ramp is subtracted from the voltage feedback signal internally. The difference signal is then divided by ten (five for the CS5126) before the PWM comparator to provide high noise rejection with a low voltage across the current sense network. (The effective ramp is 21mV/ μ s for the CS5124, and 18mV/ μ s for the CS5126). A 60mV (125mV for the CS5126) nominal offset on the positive input to the PWM comparator allows for operation with the I_{SENSE} pin at, or even slightly below Gnd.

A 4.3k Ω pull-up resistor internally connected to a 5V nominal reference provides the bias current to for an opto-coupler connection to the V_{FB} pin.

Application Information

UVLO and Thermal Shutdown Interaction

The UVLO pin and thermal shutdown circuit share the same internal comparator. During high temperature operation ($T_J > 100^\circ\text{C}$) the UVLO pin will interact with the thermal shutdown circuit. This interaction increases the turn-on threshold (and hysteresis) of the UVLO circuit. If the UVLO pin shuts down the IC during high temperature operation, higher hysteresis (see hysteresis specification) might be required to enable the IC.

BIAS Pin (CS5124 Only)

The bias pin can be used to control V_{CC} as shown in the main application diagram. In order to provide adequate phase margin for the bias control loop, the pole created by the series pass transistor and the V_{CC} bypass capacitor should be kept above 10kHz. The frequency of this pole can be calculated by Formula (1).

$$\text{Pole Frequency} = \frac{\text{Transconductance of pass Transistor}}{2 \times \pi \times C_{V(CC)}} \quad (1)$$

The Line BIAS pin shows a significant change in the regulated V_{CC} voltage when sinking large currents. This will show up as poor line regulation with a low value pull-up resistor. Typical regulated V_{CC} vs BIAS pin sink current is shown in Figure 1.

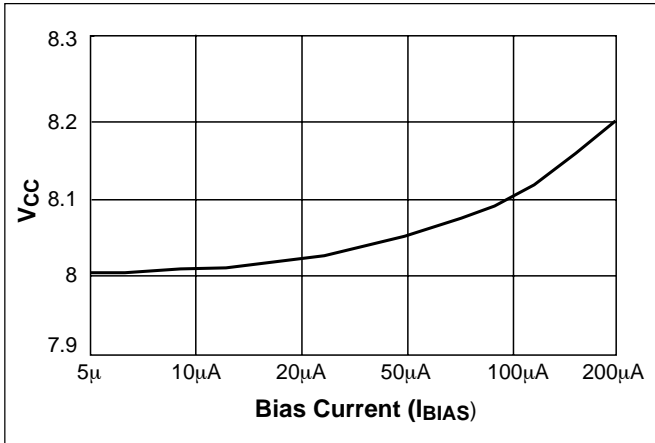


Figure 1. Regulated V_{CC} vs BIAS Sink Current

Clock Synchronization Pin (CS5126 Only)

The CS5126 can be synchronized to signals ranging from 30% slower to several times faster than the internal oscillator frequency. If the part is synchronized to a fast signal, maximum duty cycle will be reduced as the frequency increases as shown in Figure 2.

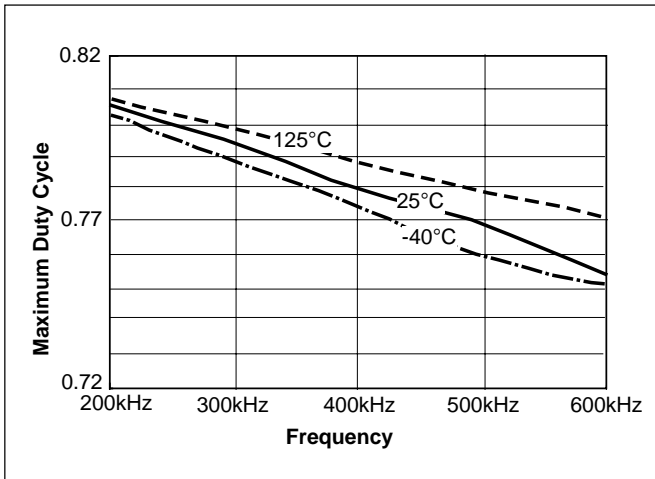


Figure 2: CS5126 Maximum Duty Cycle vs Frequency (Synchronized Operation)

If the converter is initially free running and a sync signal is applied, the current oscillator cycle will terminate and the oscillator will lock on to the sync signal. The SYNC pin works with a positive edge triggered signal. When the sync signal transitions high the current PWM cycle terminates and a new cycle begins as shown in Figure 3. The typical phase lag between the rising edge of the SYNC signal and

the rising edge of the Gate is shown in Figure 4. When this pin is held high or low the internal clock determines the oscillator frequency.

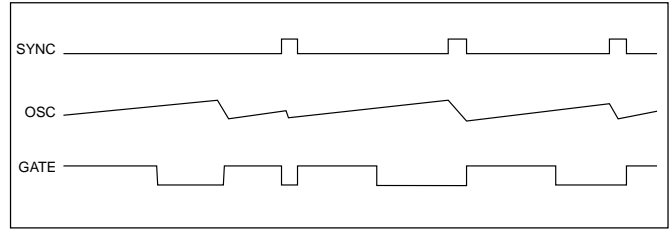


Figure 3. Synchronized Operation

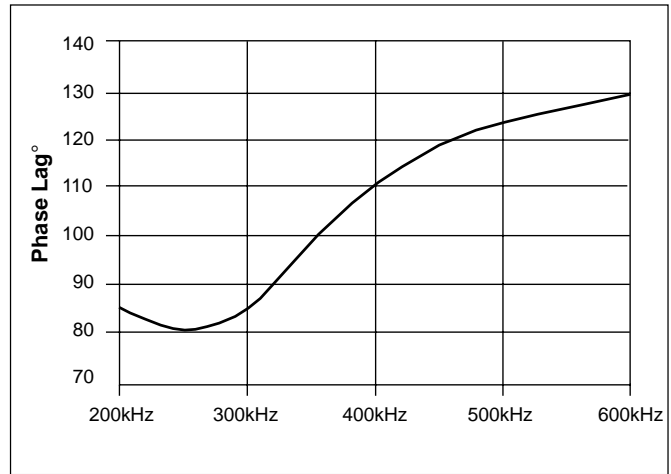


Figure 4: Typical Phase Lag between SYNC and GATE on.

Gate Drive

Rail to rail gate driver operation can be obtained (up to 13.5V) over a range of MOSFET input capacitance if the gate resistor value is kept low. Figure 5 shows the high gate drive level vs. the series gate resistance with $V_{CC} = 8V$ driving an IRF220.

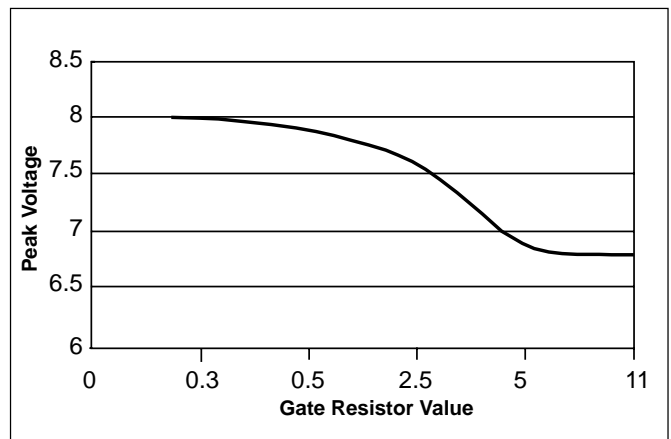


Figure 5. Gate Drive vs Gate Resistor Driving an IRF220 ($V_{CC} = 8V$)

A large negative dv/dt on the power MOSFET drain will couple current into the gate driver through the gate to drain capacitance. If this current is kept within absolute maximum ratings for the GATE pin it will not damage the IC. However if a high negative dv/dt coincides with the start of a PWM duty cycle, there will be small variations in oscillator frequency due to current in the controller substrate. If required, this can be avoided by choosing the transformer ratio and reset circuit so that a high dv/dt does not coincide with the start of a PWM cycle, or by clamping the negative voltage on the GATE pin with a schottky diode

First Current Sense Threshold

During normal operation the peak primary current is controlled by the level of the V_{FB} pin (as determined by the control loop) and the current sense network. Once the signal on the I_{SENSE} pin exceeds the level determined by V_{FB} pin the pwm cycle terminates. During high output currents the V_{FB} pin will rise until it reaches the V_{FB} clamp. The first current sense threshold determines the maximum signal allowed on the I_{SENSE} pin before the PWM cycle is terminated. Under this condition the maximum peak current is determined by the V_{FB} Clamp, the slope compensation ramp, the PWM comparator offset voltage and the PWM on time. The nominal first current threshold varies with on time and can be calculated from Formulas (2) & (3) below.

$$\text{CS5124} \\ \text{1st Threshold} = \frac{2.9V - 170mV/\mu s \times T_{ON}}{10} - 60mV \quad (2)$$

$$\text{CS5126} \\ \text{1st Threshold} = \frac{2.65V - 85mV/\mu s \times T_{ON}}{5} - 125mV \quad (3)$$

When the output current is high enough for the I_{SENSE} pin to exceed the first threshold, the pwm cycle terminates early and the converter begins to function more like a current source. The current sense network must be chosen so that the peak current during normal operation does not exceed the first current sense threshold.

Second Current Sense Threshold

The second threshold is intended to protect the converter from over-heating by switching to a low duty cycle mode when there are abnormally high fast rise currents in the converter. If the second current sense threshold is tripped, the converter will shut off and restart in Soft Start mode until the high current condition is removed. The dead time

after a second threshold over-current condition will primarily be determined by the time required to charge the Soft Start cap from 0.275V nominal to 1.32V.

The second threshold will only be reached when a high dv/dt is present at the current sense pin. The signal must be fast enough to reach the second threshold before the first threshold turns off the driver. This will normally happen if the forward inductor saturates or when there is a shorted load.

Excessive filtering of the current sense signal, a low value current sense resistor, or even an inductor that does not saturate during heavy output currents can prevent the second threshold from being reached. In this case the first current sense threshold will trip during each cycle of high output current conditions. The first threshold will limit output current but some components, especially the output rectifier, can overheat due to higher than normal average output current.

Slope Compensation

Current mode converters operating at duty cycles in excess of 50% require an artificial ramp to be added to the current waveform or subtracted from the feedback waveform. For the current loop to be stable the artificial ramp must be equivalent to at least 50% of the inductor current down slope and is typically chosen between 75% to 100% of the inductor down current down slope.

To choose an inductor value such that the internal slope compensation ramp will be equal to a certain fraction of the inductor down current slope use the Formula (4).

$$\frac{1}{\text{Internal Ramp}} \times (V_{OUT} + V_{RECTIFIER}) \times \frac{N_{SECONDARY}}{N_{PRIMARY}} \times R_{I(SENSE)} \times \text{Slope Value Factor} = \text{Inductor Value (H)} \quad (4)$$

Calculating the nominal inductor value for an artificial ramp equivalent to 100% of the current inductor down slope at CS5126 nominal conditions, a 5V output, a 200mΩ current sense resistor and a 4:1 transformer ratio yields

$$\frac{1}{20mV/\mu s} \times (5V + 0.3V) \times \frac{1}{4} \times 0.2\Omega \times 1 = 13.2 \mu H$$

To check that the slope compensation ramp will be greater than 50% of the inductor down under all conditions, substitute the minimum internal slope compensation value and use 0.5 for the slope compensation value. Then check that the actual inductor value will always be greater than the inductor value calculated.

During synchronized operation of the CS5126 the slope compensation ramp is reduced by 33%. If the CS5126 will

Package Specification

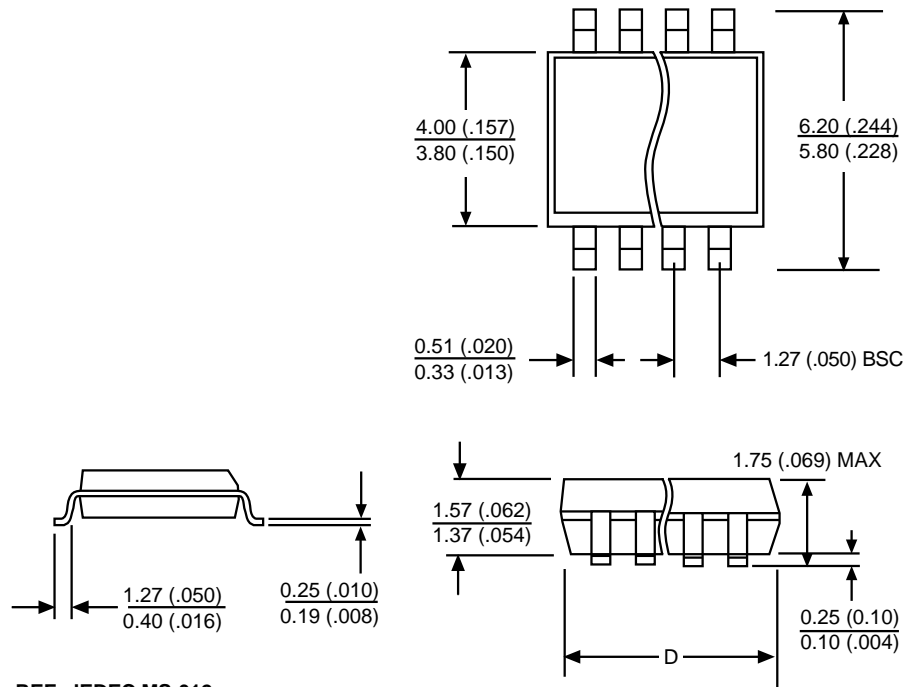
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8 Lead SO Narrow	5.00	4.80	.197	.189

PACKAGE THERMAL DATA

Thermal Data		8L SO Narrow	
R _{θJC}	typ	45	°C/W
R _{θJA}	typ	165	C/W

Surface Mount Narrow Body (D); 150 mil wide



Ordering Information

Part Number	Description
CS5124XD8	8 Lead SO Narrow
CS5124XDR8	8 Lead SO Narrow (<i>tape & reel</i>)
CS5126XD8	8 Lead SO Narrow
CS5126XDR8	8 Lead SO Narrow (<i>tape & reel</i>)

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