CS5210 Datasheet

HDMI to VGA Convertor

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1 Introduction

The Capstone CS5210 HDMI to VGA converter combines a HDMI input interface and an analog RGB DAC output. With support internal LDO, it saves cost and optimizes board space. The embedded MCU is based on an industrial standard 8051 core.

The CS5210 is suitable for multiple market segments and display applications, such as laptop, motherboard, desktop, dongle, and docking system.

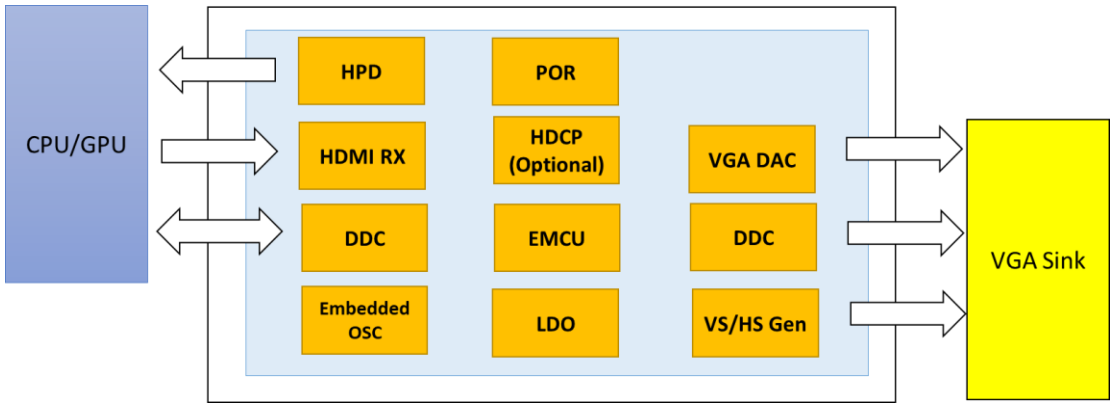

Figure 1-1 CS5210 Block Diagram

2 Features

General

- HDMI 1.4 compliant receiver
- VGA output interface, DAC speed up to ~200-MHz Pixel rate, 8-bit
- Video resolution support up to 1920x1200@60 and 1920X1080@60Hz
- Embedded oscillator and there's no need for external crystal
- Embedded linear dropout regulator (LDO)
- Embedded MCU
- On-chip HDCP Engine Which is compliant with HDCP 1.4 Specification (Optional)
- Integrated on-chip HDCP 1.4 Keys (Optional)
- Embedded EDID (CS5210 will response EDID if terminal device doesn't have it)
- Support EEPROM Free mode by using the internal pre-blew ROM
- Support Auto Power Saving mode
- VGA Connection detection supported
- Internal power-on-reset (POR)
- Dual Channel 16-bit resolution sigma-delta DAC
- I2C Slave interface and HDMI DDC interface are available for debug and firmware update.
- QFN32 4x4 package

HDMI Digital Input

- HDMI 1.4 compliant
- Built-in high-performance adaptive equalizer
- Support Hot Plug Detection

VGA Output Interface

- Triple 8-bit DAC (Digital-to-Analog Converter) with clock up to 200-MHz
- Video resolution support up to 1920x1200@60 and 1920X1080@60Hz
- Embedded V-sync/ H-sync 5V buffer
- HBM 4-KV for VGA connector pins
- VESA VSIS v1r2 compliant

Embedded MCU

- Industrial standard 8051 core
- Support I2C Master and Slave up to 400-KHz.

Power & Technology

- Single 5V power supply
- Ultralow standby power < 100uW

3 Pin Definition

3.1 Pin Assignments

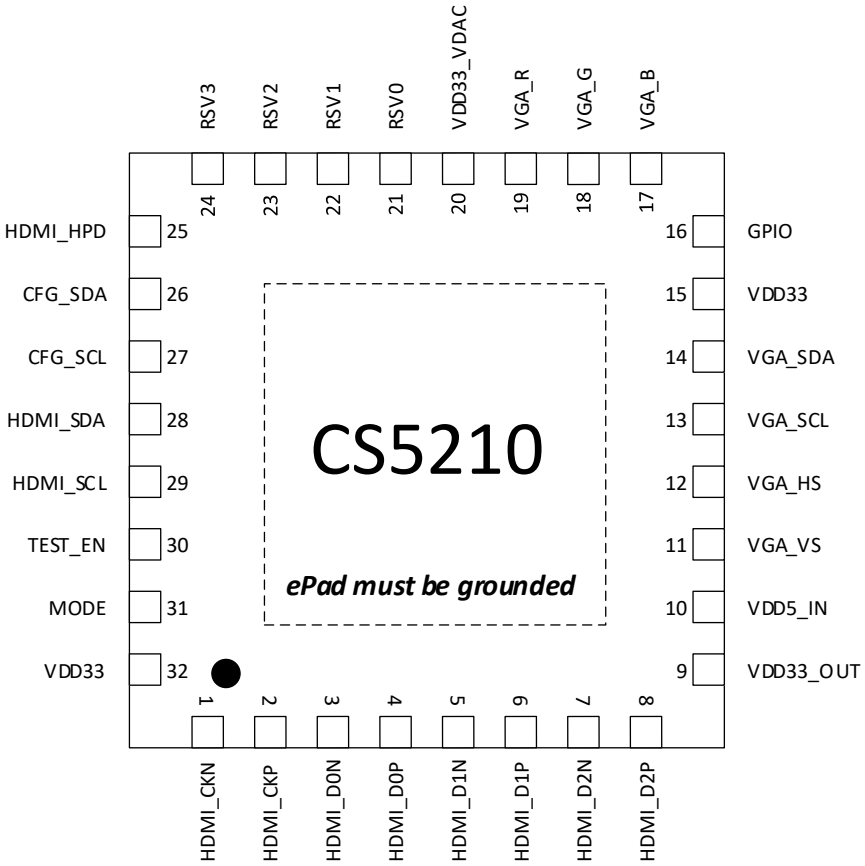

Figure 3-1 CS5210 Pin Layout

3.2 Pin Description

Table 3-1 CS5210 Pin Definitions

Pin #	Description	Type	PU/PD	Note
1	HDMI_CKN	I	-	HDMI clock differential pair N input
2	HDMI_CKP	I	-	HDMI clock differential pair P input
3	HDMI_D0N	I	-	HDMI data channel 0 different pair N input
4	HDMI_D0P	I	-	HDMI data channel 0 different pair P input
5	HDMI_D1N	I	-	HDMI data channel 1 different pair N input

Pin #	Description	Type	PU/PD	Note
6	HDMI_D1P	I	-	HDMI data channel 1 different pair P input
7	HDMI_D2N	I	-	HDMI data channel 2 different pair N input
8	HDMI_D2P	I	-	HDMI data channel 2 different pair P input
9	VDD33_OUT	P	-	3.3V power output
10	VDD5_IN	P	-	5V power input
11	VGA_VS	O	-	VGA vertical sync output
12	VGA_HS	O	-	VGA horizontal sync output
13	VGA_SCL	I/O	-	VGA DDC clock
14	VGA_SDA	I/O	-	VGA DDC data
15	VDD33	P	-	3.3V power input
16	GPIO	I	-	General GPIO
17	VGA_B	O	-	VGA Blue channel output
18	VGA_G	O	-	VGA Green channel output
19	VGA_R	O	-	VGA Red channel output
20	VDD33_VDAC	P	-	3.3V Video DAC power input, connect with VDD33_OUT
21	RSV0		-	Reserved pin, keep it as N/C
22	RSV1		-	Reserved pin, keep it as N/C
23	RSV2		-	Reserved pin, keep it as N/C
24	RSV3		-	Reserved pin, keep it as N/C
25	HDMI_HPD	I/O	PD	HDMI Hot Plug detect output
26	CFG_SDA	I/O	-	I2C slave DATA pin
27	CFG_SCL	I/O	-	I2C slave CLOCK pin
28	HDMI_SDA	I/O	-	HDMI DDC data
29	HDMI_SCL	I/O	PU	HDMI DDC clock
30	TEST_EN	I	PD	1: Test mode. 0: Normal mode
31	MODE	I	PU	1: Flash mode. 0: Reserved (Don’t pull down)
32	VDD33	P	-	3.3V power input

4 Interfaces and Capability

4.1 HDMI Input

The HDMI input is compliant with the HDMI 1.4b standard. It supports HDCP(Optional) 1.4 content protection standard.

The DDC_SCL and DDC_SDA signals are used to access EDID. Because of pull-up resistors on these signals has been integrated into Chip, so there is no need external pull-up resistor anymore.

4.2 HDCP(Optional)

The CS5210 supports HDCP 1.4 on the output video link with an embedded HDCP key. The Digital Rights Management (DRM) policy of the operating system running on the source application processor decides whether or not to enable HDCP on the link, depending on the content.

The HDCP(Optional) authentication is performed before the video transmission. The HDCP authentication and encryption can be performed by the hardware HDCP module. Pre-programmed HDCP keys and Key Selector Value (KSV) stored in the internal memory are used in the HDCP process.

4.3 Analog VGA output

CS5210 integrates triple 8bit-250MHz-DAC (Digital-to-Analog Converters), with each DAC assigned for each color, R (red), G (green), and B (blue). The Analog VGA interface of CS5210 is compliant with the VESA VSIS v1r2. Real-time Hot plug detection mechanism is also integrated into CS5210.

The most popular video formats supported by CS5210 are shown in the following Table 4 1. However, the formats supported by CS5210 are not limited to this table. Those formats with (a) the data transmission bandwidth lower than the maximal bandwidth, the pixel frequency slower than the maximal DAC speed 200-MHz can also be supported by CS5210.

Table 4-1 Supported Popular Timing/ Resolution

Resolution	Refresh Rate (Hz)	Horizontal Freq. (kHz)	Pixel Freq. (MHz)	Standard Type	Ori. Document	Date
800 x 600	60	37.9	40.000	VESA Guidelines	VG900602	8/6/90
	72	48.1	50.000	VESA Standard	VS900603A	8/6/90
	75	46.9	49.500	VESA Standard	VDMT75HZ	10/4/93
	85	53.7	56.250	VESA Standard	VDMTPROP	3/1/96
848 x 480	60	31.0	33.750	VESA Standard	AddDMT	3/4/03
1024 x 768	43	35.5	44.900	Industry Standard		
	60	48.4	65.000	VESA Guidelines	VG901101A	9/10/91
	70	56.5	75.000	VESA Standard	VS910801-2	8/9/91
	75	60.0	78.750	VESA Standard	VDMT75HZ	10/4/93
	85	68.7	94.500	VESA Standard	VDMTPROP	3/1/96
1152 x 864	75	67.5	108.000	VESA Standard	VDMTPROP	3/1/ 96
1280 x 720	60	45.0	74.250	CEA Standard	CEA -861	
1280 x 768	60	47.4	68.250	CVT Red. Blanking	AddDMT	3/4/03
	60	47.8	79.500	CVT	AddDMT	3/4/03
	75	60.3	102.250	CVT	AddDMT	3/4/03
	85	68.6	117.500	CVT	AddDMT	3/4/03
1280 x 800	60	49.3	71.000	CVT Red. Blanking	CVT1.0 2MA-R	5/1/ 07
	60	49.7	83.500	CVT	CVT 1.02MA	5/1/07
	75	62.8	106.500	CVT	CVT 1.02MA	5/1/07
	85	71.6	122.500	CVT	CVT 1.02MA	5/1/07
1280 x 960	60	60.0	108.000	VESA Standard	VDMTPROP	3/1/ 96
	85	85.9	148.500	VESA Standard	VDMTPROP	3/1/ 96
1280 x 1024	60	64.0	108.000	VESA Standard	VDMTREV	12/18/96
	75	80.0	135.000	VESA Standard	VDMT75HZ	10/4/93
	85	91.1	157.500	VESA Standard	VDMTPROP	3/1/96
1360x768	60	48.0	72.000	VESA Standard	DMT Update	11/30/07
	60	47.7	85.500	VESA Standard	AddDMT	3/4/03
	60	47.7	85.500	VESA Standard	DMT Update	11/30/07
1400 x 1050	60	64.7	101.000	CVT Red. Blanking	AddDMT	5/13/03
	60	65.3	121.750	CVT	AddDMT	3/4/03
	75	82.3	156.000	CVT	AddDMT	3/4/03
	85	93.9	179.500	CVT	AddDMT	3/4/03
1440 x 900	60	55.5	88.750	CVT Red. Blanking	CVT1.30MA-R	7/14/04
	60	55.9	106.500	CVT	CVT1.30MA-R	7/14/04
	75	70.6	136.750	CVT	CVT1.30MA-R	7/14/04
	85	80.4	157.000	CVT	CVT1.30MA-R	7/14/04
1600 x 900	60	60.0	108.000	VESA Standard	VDMTREV	11/17/08
1600 x 1200	60	75.0	162.000	VESA Standard	VDMTREV	12/18/96
	65	81.3	175.500	VESA Standard	VDMTREV	12/18/96
	70	87.5	189.000	VESA Standard	VDMTREV	12/18/96
	75	93.75	202.5	VESA Standard	VDMTREV	12/18/96
1680 x 1050	60	64.7	119.000	CVT Red. Blanking	CVT1.76MA-R	7/14 /04
	60	65.3	146.250	CVT	CVT1.76MA-R	7/14 /04
	75	82.3	187.000	CVT	CVT1.76MA-R	7/14 /04
1920 x 1080	60	67.5	148.500	CEA Standard	CEA -861	-
1920 x 1200	60	74.0	154.000	CVT Red. Blanking	AddDMT	3/4/03
	60	74.6	193.250	CVT	AddDMT	3/4/03
1920 x 1440	60	88.822	184.750	CVT Red. Blanking	CVT2.76M3-R	-
2048 x 1152	60	70.992	156.750	CVT Red. Blanking	VDMT REV	11/17 /08
2048 x 1536	60	94.769	209.250	CVT Red. Blanking	CVT3.15M3-R	-
2560 x 1080	60	66.636	181.250	Cinema 21:9 Aspect Ratio	N/A	N/A

5 Electrical Specifications

5.1 Absolute Maximum Conditions

Permanent damage may occur if absolute maximum conditions are violated. Refer to Section 5.2 for functional operating limits.

Table 5-1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD5_IN	5V Power Input	-0.3	—	6	V
VDD33	3.3V power input	-0.3	—	3.96	V
VDD33_VDAC	3.3V Video DAC power input	-0.3	—	3.96	V
T_A	Junction temperature	-40	—	125	°C
Q_{JA}	Storage temperature1	-65	—	150	°C
ESD_{HBM}	ESD protection (Human body model)	—	—	±8	KV
ESD_{CDM}	ESD protection (Charge Device model)	—	—	700	V

1. Max 260°C can be guaranteed with max 8 sec soldering time.

5.2 Operating Conditions

Table 5-2 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33_OUT	3.3V LDO output	3.0	3.3	3.6	V
VDD5_IN	5V Power Input	4.75	5	5.25	V
VDD33	3.3V power input	3.0	3.3	3.6	V
VDD33_VDAC	3.3V Video DAC power input	3.0	3.3	3.6	V
T_A	Ambient temperature	-10		70	°C
Q_{JA}	Package thermal resistance, no air flow	—	39.3	—	°C/W

5.3 Electrical Specification

Table 5-3 DC Electrical Specification

Symbol	Parameter	For 3.3V I/O		
		Min	Typ	Max
V_{il} (V)	Input low voltage	—	—	0.8
V_{ih} (V)	Input high Voltage	2.0	—	—
V_{ol} (V)	Output low voltage	0	—	0.4
V_{oh} (V)	Output high voltage[1]	2.4	—	—

Symbol	Parameter	For 3.3V I/O		
		Min	Typ	Max
I_{in} (uA)	Input leakage current	-10	—	+10
I_{hiz} (uA)	Output tri-state leakage current	-10	—	+10

Table 5-4 AC Electrical Specification

Symbol	Description	Min	Typ	Max	Unit
T_{DPS}	Intra-Pair Differential Input Skew			0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew			1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance			0.3	T_{bit}
F_{RXC}	TMDS Clock Frequency	25		200	MHz

5.4 CS5210 Power Consumption

Different applications would result in different power consumptions of CS5210. For example, whether to adopt the embedded oscillator, and how fast of the video clock frequency are all definitely the key factors of the power consumption of CS5210. The following tables show the reference power consumption of CS5210 in several different application conditions.

Table 5-5 CS5210 Typical Power Consumption

Active Resolution / Standby	Min	Typ	Max	Unit
800x600x60 (74.25-MHz)	-	TBD	-	mW
1024x768x60 (103-MHz)	-	TBD	-	mW
1920x1080x60 (148-MHz)	-	TBD	-	mW

Note: In practice, the measured power consumption might be slightly different from the tables above due to the different video content and the different measurement equipment

6 Package Specification

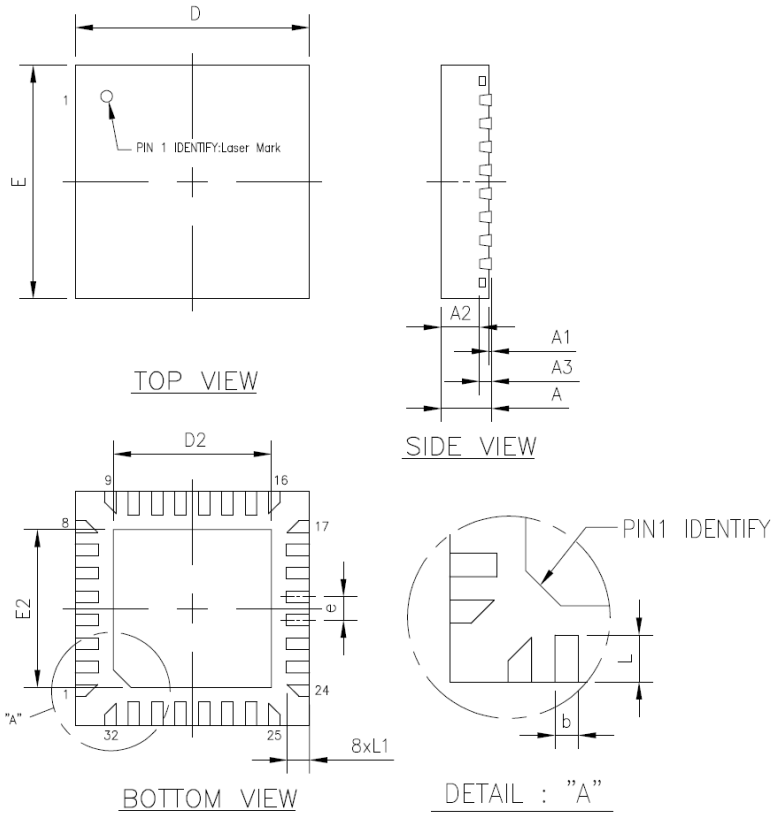

Figure 6-1 CS5210 Package Outline (QFN32 Leads 4x4mm)

Table 6-1 Package Dimension

Symbol	Dimension in mm			Dimension in inch		
	Min	Normal	Max	Min	Normal	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	—	0.65	0.70	—	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.080	0.010
D/E		4.00 BSC			0.157 BSC	
D2/E2	2.55	2.70	2.85	0.096	0.106	0.116
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.282	0.382	0.482	0.011	0.015	0.019

7 Ordering Information

The CS5210 can be ordered using the part numbers in Table 7-1. Please consult sales for further details.

Table 7-1 CS5210 Ordering Information

Part No.	Description	Temperature Range	Packing Type
CS5210	32 Pin (QFN) Lead-free package	Commercial: 0 to 70 degree C	Tape

8 Revision History

Table 8-1 Document Revision History

Revision	Date	Changes
Release 1	Oct. 2020	Initial version