CapStone

CS5218AN Datasheet

Jitter Cleaning 3.0Gbps HDMI Repeater

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1 Introduction

The Capstone CS5218AN is a single port HDMI/DVI Level Shifter/Repeater with re-timing. It supports AC and DC coupled TMDS signals up to 3.0-Gbps operation with programmable equalization and jitter cleaning. It includes Type 2 Dual-Mode DP Cable Adaptor registers which can be used to identify the cable adaptor's capabilities. The jitter cleaning PLL can better meet HDMI jitter compliance for higher data rates. Device operation and configuration can be realized through pin settings or I2C bus. Automatic power down and squelch provide flexible power management.

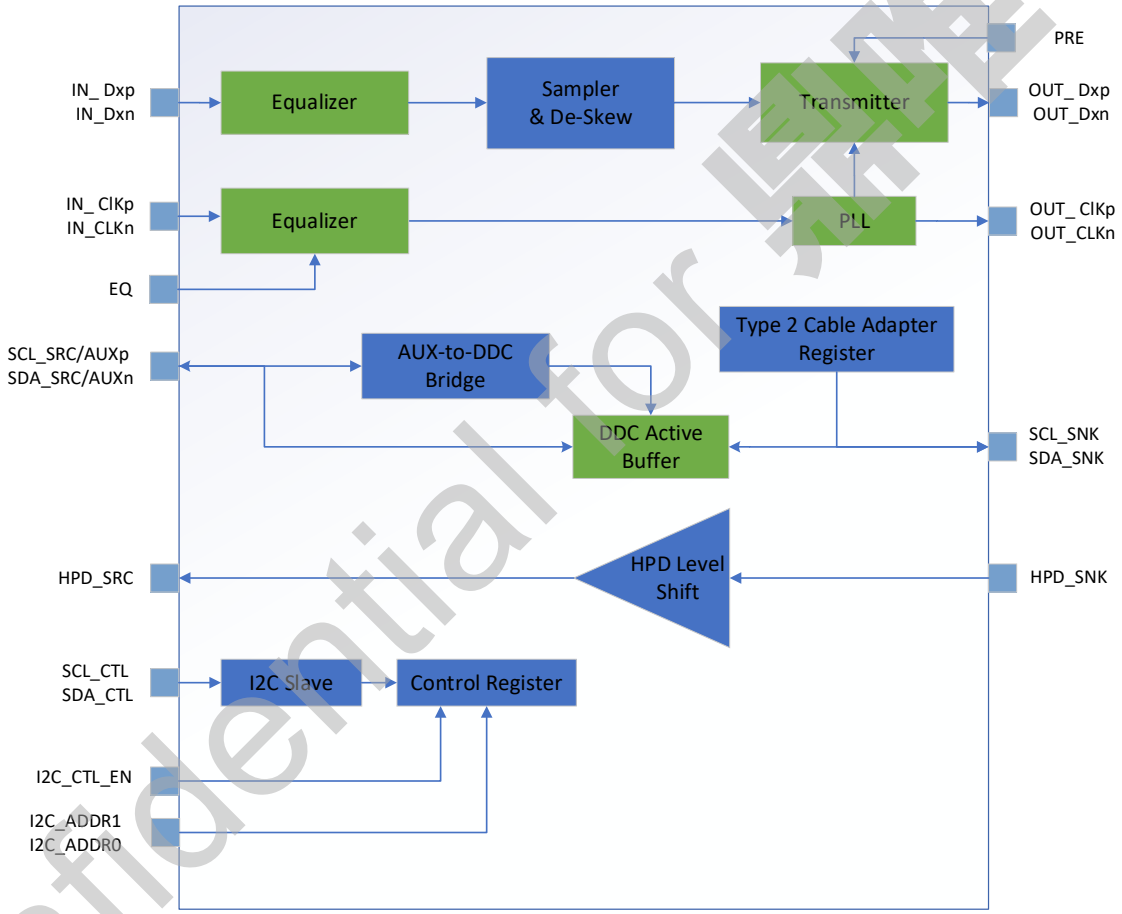

Figure 1-1 CS5218AN Block Diagram

2 Features

General

- Compliant to HDMI 1.4b specification up to 3.0Gbps
- Supports 4K x 2K & 3D video formats over HDMI
- AC coupling capable for level shifting
- DC coupling capable for repeating
- Programmable receiver equalization to compensate for PCB and/or connector losses
- Jitter Cleaning PLL for best compliance
- Superior Intra-pair and Inter-pair de-skewing
- Built-in DDC Active buffering Side-band Signals
- Programmable TMDS output pre-emphasis
- Automatic power down management
- Automatic squelch for fail-safe and power management
- Type 2 Dual-Mode DP Cable Adaptor registers accessible by I2C-over-AUX or DDC
- Built-in AUX to I2C bridge to support AUX-only GPU
- Low power consumption
- Pin control mode or I2C control mode for flexibility

HDMI Digital Input

- HDMI 1.4b compliant
- Built-in high-performance adaptive equalizer
- Support Hot Plug Detection

HDMI Digital Output

- HDMI 1.4b compliant
- Max data rate up to 3-Gbps per channel
- Support up to 3840 x 2160@30Hz or 4096x2160@30Hz

MISC

- 5x5mm 40-pin QFN RoHS compliant and lead-free package
- 0° to 70°C operating temperature range
- ESD: HBM 4 kV

Power & Technology

- Single 3.3V power supply
- Build-in 1.2V LDO for save BOM cost

3 Pin Definition

3.1 Pin Assignments

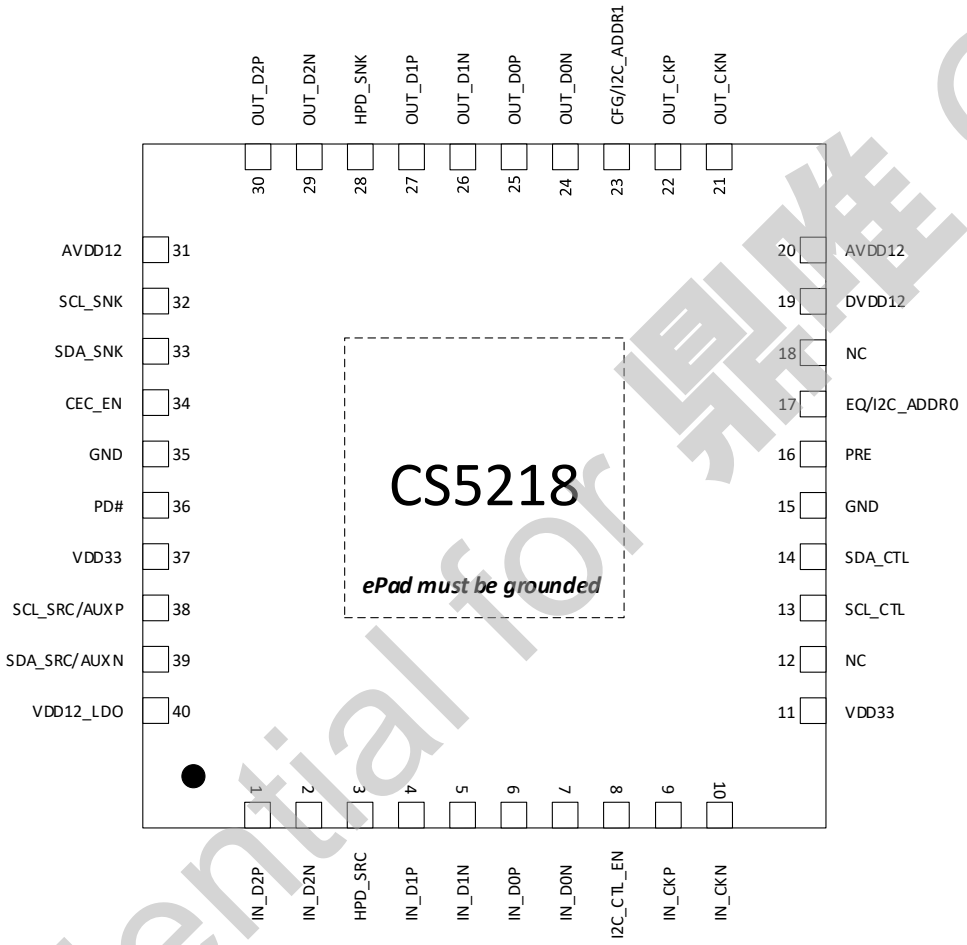

Figure 3-1 CS5218AN Pin Layout

3.2 Pin Description

Table 3-1 CS5218AN Pin Definitions

Pin #	Description	Type	PU/PD	Note
Power/Ground				
11	VDD33		P	3.3V Power
37	VDD33		P	3.3V Power, also LDO input
19	DVDD12		P	Digital 1.2V Power

Pin #	Description	Type	PU/PD	Note
20,31	AVDD12		P	Analog 1.2V Power
40	VDD12		P	LDO output
41	GND		G	e-PAD
High-speed Interface				
1,2	IN_D2P/N	Analog	I	HDMI data channel 2 different pair input
4,5	IN_D1P/N	Analog	I	HDMI data channel 1 different pair input
6,7	IN_D0P/N	Analog	I	HDMI data channel 0 different pair input
9,10	IN_CKP/N	Analog	I	HDMI clock differential pair input
30,29	OUT_D2P/N	Analog	O	HDMI data channel 2 different pair output
27,26	OUT_D1P/N	Analog	O	HDMI data channel 1 different pair output
25,24	OUT_D0P/N	Analog	O	HDMI data channel 0 different pair output
22,21	OUT_CKP/N	Analog	O	HDMI clock differential pair output
Low-speed Interface				
3	HPD_SRC	LVTTL	O	Hot plug detection to Source, 3.3V CMOS output
28	HPD_SNK	LVTTL	I	Hot plug detection from Sink. Internal pull down at 150kΩ±20%; 5V tolerant CMOS input Note: When automatic power down is enabled, chip will be powered down when no cable is plugged in (no Sink devices detected).
39	SDA_SRC/AUXN	Analog	I/O	Multi-input pins .Either for source side DDC data lines or AUX-only sideband. Need external 2KΩ resistor pull up to 3.3V.
38	SCL_SRC/AUXP	Analog	I/O	Multi-input pins .Either for source side DDC clock lines or AUX-only sideband. Need external 2KΩ resistor pull up to 3.3V.
33	SDA_SNK	LVTTL	I/O	Sink side DDC data line. 5V tolerant I/O.
32	SCL_SNK	LVTTL	I/O	Sink side DDC clock line. 5V tolerant I/O.
34	CEC_EN	LVTTL	O	CEC connection enable
Configuration				
36	PD#	LVTTL	I	L: Power down LDO H: Power up LDO
8	I2C_CTL_EN	3-state	I	L, M: Pin control with full jitter cleaning H: I2C control with default I2C address
14	DDCBUF/CSDA	3-state	I/O	In Pin control mode: L: DDC buffer with default threshold M: DDC buffer with threshold 1 H: DDC buffer with threshold 2 In I2C control mode: Config I2C data
13	CSCL	LVTTL	I	In Pin control mode: Reserved. In I2C control mode:

Pin #	Description	Type	PU/PD	Note
				Config I2C clock
17	EQ/I2C_ADDR0	3-state	I	In Pin control mode: L: EQ for channel loss of 12.4dB M: EQ for channel loss of 4.3dB H: EQ for channel loss of 8.6dB In I2C control mode: I2C ADDR select 0
23	CFG/I2C_ADDR1	LVTTL	I	In Pin control mode: L: DVI ID mode H: HDMI ID mode In I2C control mode: I2C ADDR select 1

4 Electrical Specifications

4.1 Absolute Maximum Conditions

Permanent damage may occur if absolute maximum conditions are violated. Refer to Section 4.2 for functional operating limits.

Table 4-1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	3.3V power input	-0.3	—	3.96	V
VDD12	1.2V power input	-0.3	—	1.44	V
T_A	Junction temperature	-40	—	125	°C
Q_{JA}	Storage temperature1	-65	—	150	°C
ESD_{HBM}	ESD protection (Human body model)	—	—	4	KV
ESD_{CDM}	ESD protection (Charge Device model)	—	—	700	V

1. Max 260°C can be guaranteed with max 8 sec soldering time.

4.2 Operating Conditions

Table 4-2 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD12_OUT	1.2V LDO output	1.1	1.2	1.3	V
VDD33	3.3V power input	3.0	3.3	3.6	V
DVDD12	1.2V power input	1.1	1.2	1.3	V
AVDD12	1.2V power input	1.1	1.2	1.3	V
T_A	Ambient temperature	0		70	°C
Q_{JA}	Package thermal resistance, no air flow	—	39.3	—	°C/W

4.3 Electrical Specification

Table 4-3 DC Electrical Specification

Symbol	Parameter	Min	Typ	Max	Unit
Three-level control pins: DDCBUF, PRE, EQ					
V_{IH}	Three-level input HIGH	VDD33 –0.6			V
V_{IM}	Three-level input MID	VDD33/2– 0.5		VDD33/2+0.5	V
V_{IL}	Three-level input LOW			0.6	V
$\|I_{IH}\|$	Input High-level current V_{IH} = VDD33			40	uA

Symbol	Parameter	Min	Typ	Max	Unit
$\|I_{IL}\|$	Input Low-level current V_{IL} = 0.5 V			10	uA
Control pins (Internal pull-down): I2C_CTL_EN, DCIN_EN, I2C_ADDR1, I2C_ADDR0, CFG					
V_{IH}	LVTTL input High-level voltage	2		VDD33	V
V_{IL}	LVTTL input Low-level voltage	GND		0.8	V
$\|I_{IH}\|$	Input High-level current V_{IH} = 2V to VDD33			40	µA
$\|I_{IL}\|$	Input Low-level current V_{IL} = GND to 0.8V			10	µA
Control pins (Internal pull-up): PD#					
V_{IH}	LVTTL input High-level voltage	2		VDD33	V
V_{IL}	LVTTL input Low-level voltage	GND		0.8	V
$\|I_{IH}\|$	Input High-level current V_{IH} = 2V to VDD33			10	µA
$\|I_{IL}\|$	Input Low-level current V_{IL} = GND to 0.8V			40	µA
Control I2C Pins: SCL_CTL, SDA_CTL					
V_{OH}	High-level output voltage External 1.5 kΩ pull-up to VDD33, IOL = 8 mA			VDD33	V
V_{OL}	Low-level output voltage			0.4	V
HPD input pin: HPD_SNK					
V_{IH}	LVTTL input High-level voltage	2		5.3	V
V_{IL}	LVTTL input Low-level voltage	GND		0.8	V
$\|I_{IH}\|$	Input High-level current V_{IH} = 2 V to 5.3 V			80	uA
$\|I_{IL}\|$	Input Low-level current V_{IL} = GND to 0.8 V			20	uA
Status output pins: HPD_SRC					
V_{OH}	LVTTL High-level output voltage I_{OH} = -8 mA	2.4			V
V_{OL} LVTTL Low-level output voltage	I_{OL} = 8 mA			0.4	V
TMDS Differential inputs: IN_Dxp, IN_Dxn, IN_CKp, IN_CKn					
V_{ID}	Peak-to-peak differential input voltage	150		1560	mV
V_{IC}	Input common mode voltage	2.2		AVcc -0.04	V
AVcc	TMDS termination voltage	3	3.3	3.6	V
R_T	Input termination resistance		45	50	55
TMDS Differential Outputs: OUT_Dxp, OUT_Dxn, OUT_CKp, OUT_CKn					

Symbol	Parameter	Min	Typ	Max	Unit
V_{OD}	Peak-to-peak differential output swing	800	1000	1200	mV
V_{OH}	Single end high-level output voltage AVcc = 3.3 V,	AVcc-10		AVcc+10	mV
V_{OL}	Single end low-level output voltage RT = 50 ohm	AVcc-600		AVcc-400	mV
I_{OFF}	Single end standby output current	-10		10	uA
I_{SC}	Output short circuit current			12	mA
Resistors					
$R_{RX-TERM}$	Differential input termination resistor	80		120	Ω

Note: All typical values are measured at 25 °C and 3.3V / 1.2V power supply.

Table 4-4 AC Electrical Specification

Symbol	Parameter	Min	Typ	Max	Unit
TMDS differential outputs: OUT_Dyp, OUT_Dyn, OUT_CKp, OUT_CKn					
Propagation delay					
t_{PLH}	low-to-high propagation delay (300 MHz clock)			1	ms
t_{PHL}	high-to-low propagation delay (300 MHz clock)			1	ms
Rise time/fall time (20%~80%)					
t_r	differential output rise time AVcc = 3.3V, RT = 50 Ω	90		243	ps
t_f	differential output fall time AVcc = 3.3V, RT = 50 Ω	90		243	ps
Intra-pair/Inter-pair skew					
t_{sk_intra}	intra-pair differential skew			0.15	T_{bit}
t_{sk_inter}	inter-pair differential skew			0.5	T_{bit}
Clock jitter/Data jitter					
t_{jit}	Clock input jitter Clock > 165MHz			151.5	ps
	Clock input jitter Clock <= 165MHz			0.25	Tbit
t_{jit}	Clock output jitter @297MHz			84.2	ps
	Clock output jitter @222.5MHz			112.4	ps
t_{jit}	Data input jitter			0.6	T_{bit}
	Data output jitter			0.3	T_{bit}
Clock jitter attenuation	Out-of-band TMDS clock jitter attenuation @ 0.5Tbit input jitter	12			dB

Note: All typical values are measured at 25 °C and 3.3V / 1.2V power supply.

5 Package Specification

Figure 5-1 CS5218AN Package Outline (QFN40 Leads 5x5mm²)

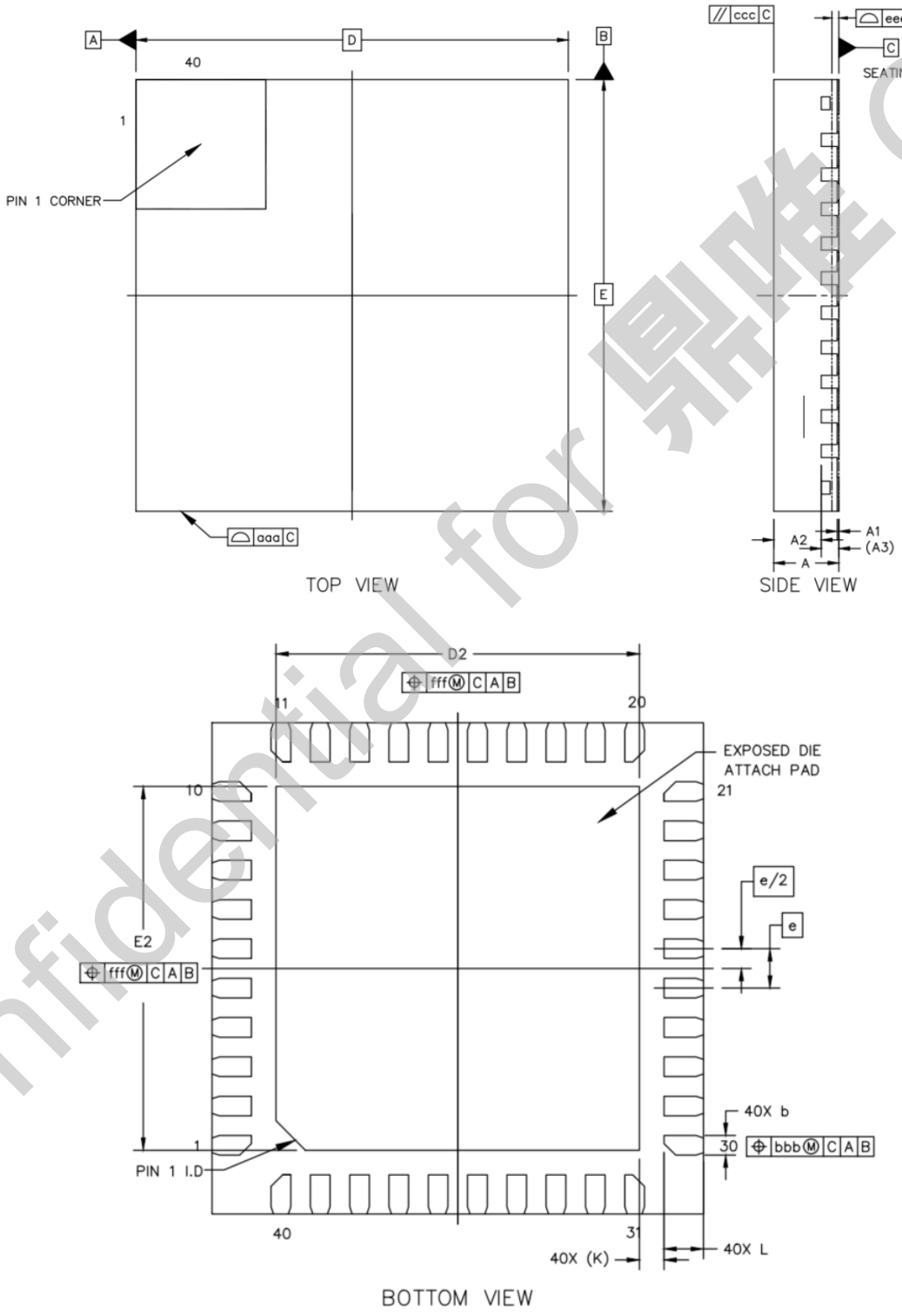

Table 5-1 Package Dimension

Symbol	Dimension in mm			Dimension in inch		
	Min	Normal	Max	Min	Normal	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	—	0.65	0.70	—	0.026	0.028
A3		0.203 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.080	0.010
D/E		5.00 BSC			0.197 BSC	
D2/E2	3.55	3.70	3.85	0.140	0.146	0.152
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

6 Ordering Information

The CS5218AN can be ordered using the part numbers in Table 6-1. Please consult sales for further details.

Table 6-1 CS5218AN Ordering Information

Part No.	Description	Temperature Range	Packing Type
CS5218AN	40Pin (QFN) Lead-free package	Commercial : 0 to 70 degree C	5K / T &R

7 Revision History

Table 7-1 Document Revision History

Revision	Date	Changes
Draft 1	Jan. 2021	Draft version
Draft 2	Feb. 2021	Draft version
Release v1.0	May. 2021	Official release
Release v1.1	June. 2021	Update some pin description