CapStone

CS5268AN Datasheet

USB Type-C to HDMI2.0b 4k@30Hz and VGA Converter with PD3.0 and USB 3.1 Support

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1 Introduction

The Capstone CS5268AN is a high-performance Type-C/DP1.4 to HDMI2.0b and VGA converter, designed to connect a USB Type-C source or a DP1.4 source to an HDMI2.0b sink. The CS5268AN integrates a DP1.4 compliant receiver, an HDMI2.0b compliant transmitter and a VGA output interface. Also, two CC controllers are included for CC communication to implement DP Alt Mode and power delivery function, one for upstream Type-C port and another for downstream port.

The DP interface comprises 2 main lanes, AUX channel, and HPD signal. The receiver supports maximum 5.4Gbps (HBR2) data rate per lane. The DP receiver incorporates both HDCP1.4 and HDCP2.3 content protection scheme with embedded key for secure transmission of digital audio-video content.

The HDMI interface includes 4 TMDS clock/data pairs, DDC, and HPD signal. The HDMI transmitter is capable of supporting up to 3Gpbs data rate, quite adequate for handling video resolutions up to FHD 1080p 120Hz and UHD 4k 30Hz formats. The HDMI transmitter incorporates HDCP engines which support both HDCP1.4 and HDCP2.3. With the inclusion of HDCP, the CS5268AN allows secure transmission of protected content. Embedded key is available that provides the highest level of HDCP key security.

The CS5268AN is a highly integrated single chip suitable for multiple market segments and display applications, such as the dongle, docking station etc.

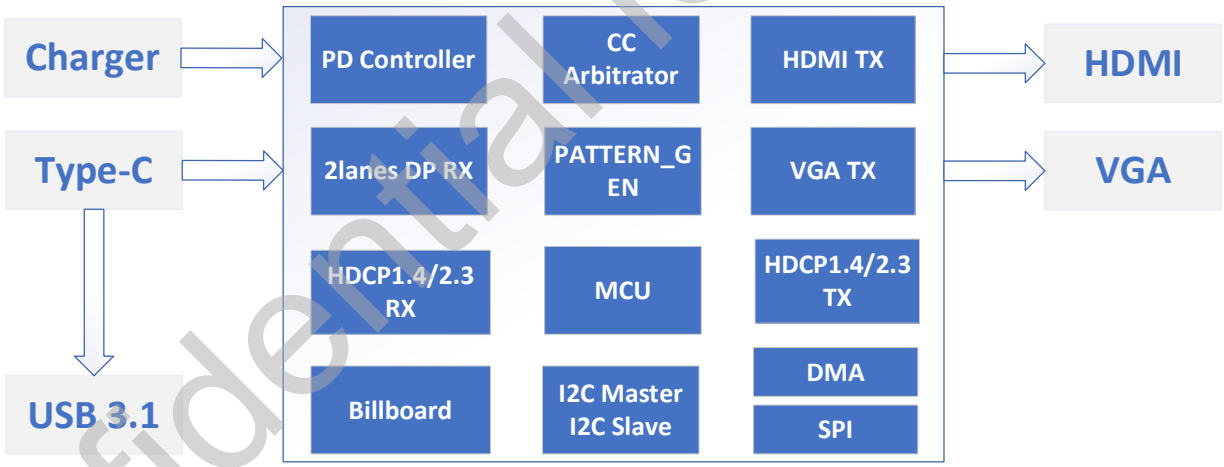

Figure 1-1 CS5268AN Block Diagram

2 Features

General

- USB Type-C Specification 1.2
- VESA DisplayPort™ (DP) v1.4 compliant receiver
- HDMI specification v2.0b compliant transmitter, data rate up to 3-Gbps per channel.
- USB Power Delivery(PD) v 3.0 compliant
- Support all USB Type-C Channel Configuration (CC)
- Embedded oscillator and there's no need for the external crystal
- Embedded MCU and SPI flash
- Embedded V-sync/H-sync buffer
- Embedded EDID (CS5268AN will response EDID if terminal device doesn't have it)
- Support both HDCP 1.4 & HDCP2.3 with on-chip keys to support HDCP repeater.
- Support RGB 4:4:4 8/10bit bpc and YCbCr 4:4:4 , 4:2:2 ,4:2:0 8/10-bit bpc
- Max audio sample rate of 192KHz x8 channels
- LPCM and Compressed Audio encoding formats
- AUX channel, I2C host interface for chip control

USB Type-C DisplayPort(DP) Alt Mode Input (receiver)

- USB Type-C Specification 1.2 and backward compatible with Type-C Specification 1.0
- VESA DisplayPort™ v1.4 compliant. Support 2-lane.
- Built-in CC controller for plug and orientation detection
- Dual CC ports for charger and normal communication
- Up to HBR2(5.4-Gbps) input. Built-in high-performance adaptive equalizer. Support 1-MHz AUX channel
- USB Type-C Channel Configuration (CC) function
- USB Power Delivery Spec 3.0 compliant-Integrated USB Power Delivery (PD-BMC) PHY. Support for Message Protocol. Support for Policy Engine. Support for basic Device Policy Manager
- Support Hot Plug Detect (HPD)
- Support USB 3.0 for dongle application

HDMI Digital Output

- HDMI 2.0b compliant
- Max data rate up to 3-Gbps per channel
- Support up to 3840 x 2160@30Hz or 4096x2160@30Hz
- Audio stream handling
- LPCM and Compressed Audio encoding formats
- Max audio sample rate of 192k Hz x8 channels Support High Dynamic Range (HDR) metadata handling

VGA Output Interface

- Triple 8-bit DAC (Digital-to-Analog Converter) with clock up to 210-MHz
- Support up to 1920x1200@60Hz, 1920x1440@60Hz (reduced blanking), 2048x1152@60Hz (reduced blanking), and 2048x1536@60Hz (reduced blanking)
- Embedded V-sync/ H-sync buffer
- VESA VSIS v1r2 compliant

MISC

- Support I2C Master and Slave up to 400-kHz.
- HBM 4KV for connector pins
- 8*8mm 68-pin QFN package with e-Pad

Power & Technology

- 5V/1.0V system voltage, integrated 3.3V LDO and 1.8V LDO.

3 Pin Definition

3.1 Pin Assignments

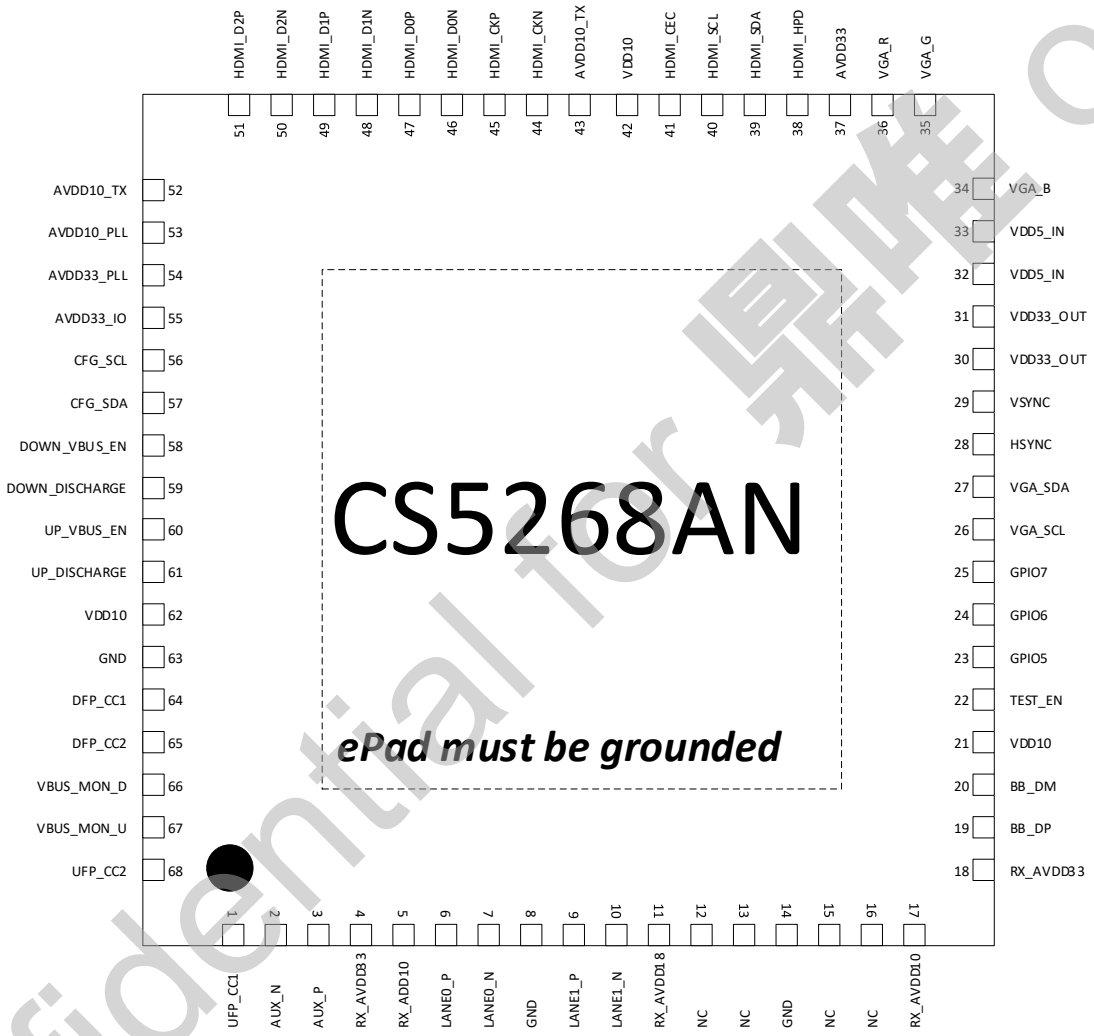

Figure 3-1 CS5268AN Pin Layout

3.2 Pin Description

Table 3-1 CS5268AN Pin Definitions

Pin #	Description	Type	PU/PD	Note
1	UFP_CC1	AIO		USB Type-C configuration channel for UFP
2	AUX_N	AIO		DisplayPort AUX channel negative

Pin #	Description	Type	PU/PD	Note
3	AUX_P	AIO		DisplayPort AUX channel positive
4	RX_AVDD33	P	-	3.3V power input
5	RX_AVDD10	P	-	1.0V power input
6	LANE0_P	AI		DisplayPort Rx lane0 positive
7	LANE0_N	AI		DisplayPort Rx lane0 negative
8	GND	P		GND
9	LANE1_P	AI		DisplayPort Rx lane1 positive
10	LANE1_N	AI		DisplayPort Rx lane1 negative
11	RX_AVDD18	P	-	1.8V LDO output, connect a 4.7uF capacitor on it.
12	NC	--		Reserved
13	NC	--		Reserved
14	GND	P		GND
15	NC	--		Reserved
16	NC	--		Reserved
17	RX_AVDD10	P	-	1.0V power input
18	RX_AVDD33	P	-	3.3V power input
19	BB_DP	AIO		USB Type-C D+ signal for billboard device
20	BB_DM	AIO		USB Type-C D- signal for billboard device
21	VDD10	P	-	1.0V power input
22	TEST_EN	I	PD	1: Test mode. 0: Normal mode.
23	GPIO5	I/O		General input output
24	GPIO6	I/O		General input output
25	GPIO7	I/O	-	General input output
26	VGA_SCL	I/O		VGA DDC clock (GPIO13)
27	VGA_SDA	I/O	-	VGA DDC data (GPIO12)
28	HSYNC	O	-	VGA horizontal sync output
29	VSYNC	O	-	VGA vertical sync output
30	VDD33_OUT	P	-	3.3V power output
31	VDD33_OUT	P	-	3.3V power output
32	VDD5_IN	P	-	5V power input
33	VDD5_IN	P	-	5V power input
34	VGA_B	O		VGA Blue channel output
35	VGA_G	O	-	VGA Green channel output
36	VGA_R	O	-	VGA Red channel output
37	AVDD33	P	-	3.3V power
38	HDMI_HPD	I/O	PD	HDMI Hot Plug detect input (GPIO11)

Pin #	Description	Type	PU/PD	Note
39	HDMI_SDA	I/O	PU	HDMI DDC data (GPIO10)
40	HDMI_SCL	I/O	PU	HDMI DDC clock (GPIO9)
41	HDMI_CEC	I/O		HDMI CEC Pin (GPIO8)
42	VDD10	P		1.0V power input
43	AVDD10_TX	P	-	1.0V power input
44	HDMI_CKN	I	-	HDMI clock differential pair N output
45	HDMI_CKP	I	-	HDMI clock differential pair P output
46	HDMI_D0N	I	-	HDMI data channel 0 different pair N output
47	HDMI_D0P	I	-	HDMI data channel 0 different pair P output
48	HDMI_D1P	I	-	HDMI data channel 1 different pair N output
49	HDMI_D1P	I	-	HDMI data channel 1 different pair P output
50	HDMI_D2N	I	-	HDMI data channel 2 different pair N output
51	HDMI_D2P	I	-	HDMI data channel 2 different pair P output
52	AVDD10_TX	P		1.0V power input
53	AVDD10_PLL	P	-	1.0V power input
54	AVDD33_PLL	P	-	3.3V power input
55	AVDD33_IO	P		3.3V power input
56	CFG_SCL	I/O	-	I2C slave CLOCK pin for debug
57	CFG_SDA	I/O	-	I2C slave DATA pin for debug
58	DOWN_VBUS_EN	I/O		GPIO1 for Downstream port power enable.
59	DOWN_DISCHARGE	I/O		GPIO2 for Downstream port power discharge.
60	UP_VBUS_EN	I/O		GPIO3 for Upstream port power enable.
61	UP_DISCHARGE	I/O		GPIO4 for Upstream port power discharge.
62	VDD10	P	-	1.0V power input
63	GND	P		GND
64	DFP_CC1	AIO		USB Type-C configuration channel for DFP
65	DFP_CC2	AIO		USB Type-C configuration channel for DFP
66	VBUS_MON_D	AI		Vbus voltage monitor for DFP
67	VBUS_MON_U	AI		Vbus voltage monitor for UFP
68	UFP_CC2	AIO		USB Type-C configuration channel for UFP

4 Electrical Specifications

4.1 Absolute Maximum Conditions

Permanent damage may occur if absolute maximum conditions are violated. Refer to Section 4.2 for functional operating limits.

Table 4-1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD5_IN	5V Power Input	-0.3	—	6	V
VDD33	3.3V power input	-0.3	—	3.96	V
VDD10	1.0V power input	-0.3	—	1.2	V
T_A	Junction temperature	-40	—	125	°C
Q_{JA}	Storage temperature1	-65	—	150	°C
ESD_{HBM}	ESD protection (Human body model)	—	—	±4	KV
ESD_{CDM}	ESD protection (Charge Device model)	—	—	700	V

1. Max 260°C can be guaranteed with max 8 sec soldering time.

4.2 Operating Conditions

Table 4-2 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33_OUT	3.3V LDO output	3.0	3.3	3.6	V
VDD5_IN	5V Power Input	4.75	5	5.25	V
VDD33	3.3V power input	3.0	3.3	3.6	V
VDD10	1.0V power input	0.95	1.0	1.1	V
T_A	Ambient temperature	0		70	°C
Q_{JA}	Package thermal resistance, no air flow	—	39.3	—	°C/W

4.3 Electrical Specification

Table 4-3 DC Electrical Specification

Symbol	Parameter	For 3.3V I/O		
		Min	Typ	Max
V_{il} (V)	Input low voltage	—	—	0.8
V_{ih} (V)	Input high Voltage	2.0	—	—
V_{ol} (V)	Output low voltage	0	—	0.4
V_{oh} (V)	Output high voltage	2.4	—	—

Symbol	Parameter	For 3.3V I/O		
		Min	Typ	Max
I_{in} (uA)	Input leakage current	-10	—	+10
I_{hiz} (uA)	Output tri-state leakage current	-10	—	+10

5 Package Specification

Figure 5-1 CS5268AN Package Outline (QFN68 Leads 8x8mm2)

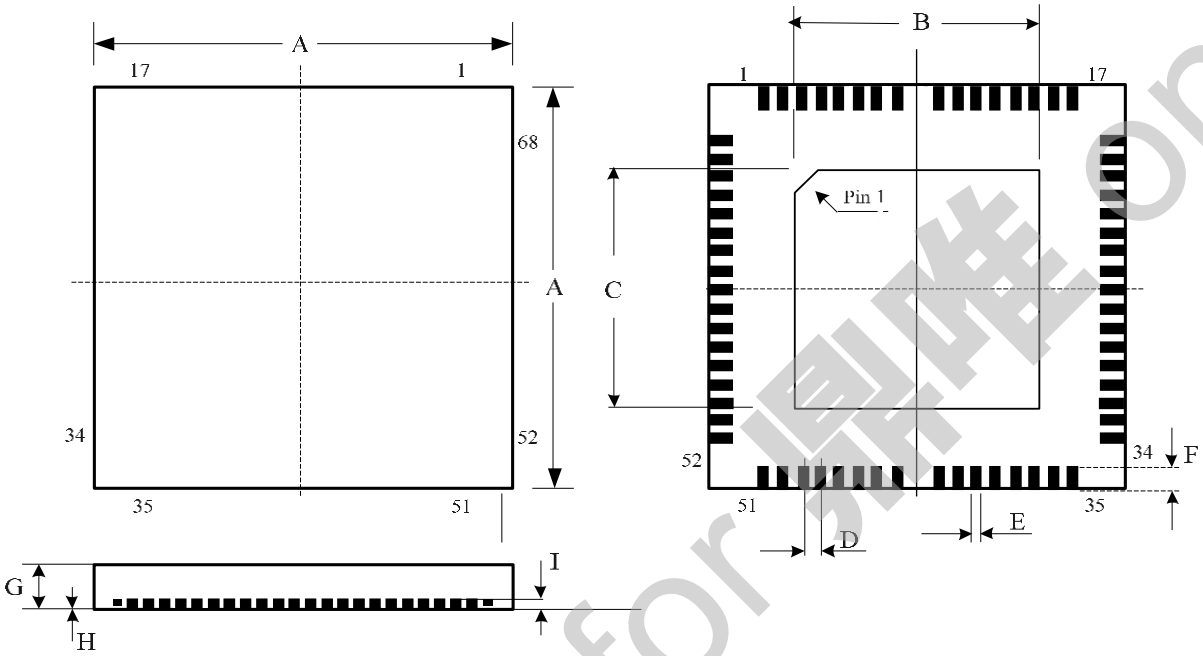

Table 5-1 Package Dimension

Symbol	Dimension in mm			Dimension in inch		
	Min	Normal	Max	Min	Normal	Max
A	7.9	8.0	8.1	0.311	0.314	0.319
B	5.50	5.70	5.90	0.217	0.224	0.232
C	5.50	5.70	5.90	0.217	0.224	0.232
D		0.40 BSC			0.016 BSC	
E	0.15	0.20	0.25	0.006	0.008	0.010
F	0.30	0.40	0.50	0.012	0.016	0.020
G	0.80	0.85	0.90	0.031	0.033	0.035
H	0	0.02	0.05	0	0.001	0.002
I		0.20 REF			0.008 REF	

6 Ordering Information

The CS5268AN can be ordered using the part numbers in Table 6-1. Please consult sales for further details.

Table 6-1 CS5268AN Ordering Information

Part No.	Description	Temperature Range	Packing Type
CS5268AN	68 Pin (QFN) Lead-free package	Commercial : 0 to 70 degree C	Sample

7 Revision History

Table 7-1 Document Revision History

Revision	Date	Changes
Draft V0.1	Oct. 2020	First draft version.
Draft V0.2	Dec. 2020	Update Pin Assignments.
Draft V0.3	Mar. 2021	First release.
Release V1.0	June. 2021	Update Package Specification.
Release V1.1	June. 2021	Update Some Pin description.