Semiconductor Corporation

CS5326 CS5327
CS5328 CS5329

16 & 18-Bit, Stereo A/D Converters for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates
  - 30 kHz to 50 kHz
- Low Noise and Distortion
  - 95 dB dynamic range, 16-Bit
  - 97 dB dynamic range, 18-Bit
  - 100 dB dynamic range, 19-Bit Mono
  - 0.0015% THD
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.001dB Passband Ripple
  - 86dB Stopband Rejection
- Low Power Dissipation: 450 mW
  - Power-Down Mode for Portable Applications

General Description

The CS5326, CS5327, CS5328 & CS5329 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16 or 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

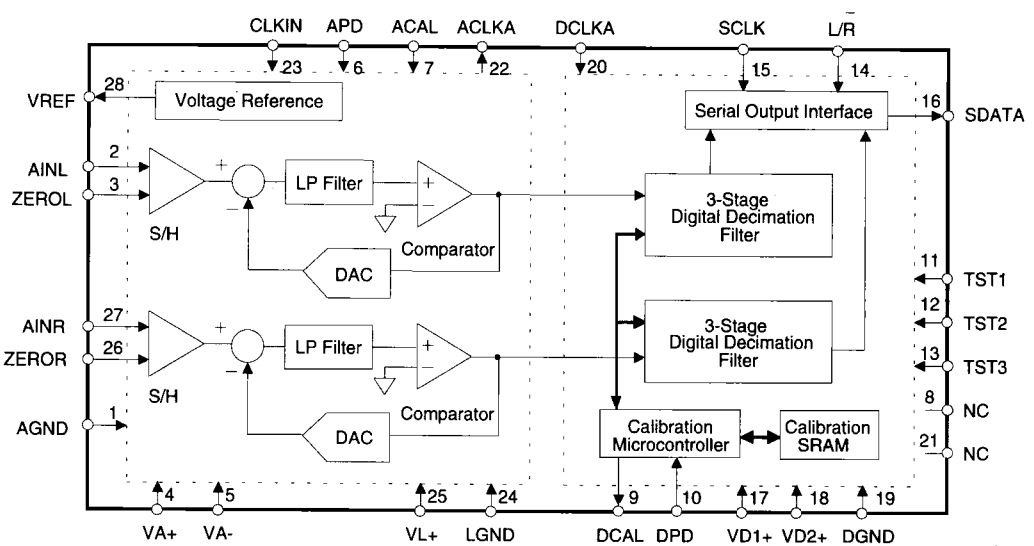
The ADCs use delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5326 & CS5327 are 16-bit ADCs, achieving 95 dB dynamic range. The CS5328 & CS5329 are 18-bit ADCs with 97 dB dynamic range in stereo mode and 100 dB dynamic range in mono mode.

The CS5326 & CS5328 have digital filters which are compatible with CD requirements. The CS5327 & CS5329 have filters which guarantee no aliasing. The filters have linear phase, 0.001 dB passband ripple, and >86 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP.

ORDERING INFORMATION: Page 3-23



ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VL+,VD1+,VD2+ = 5V; VA- = -5V; Full-Scale Input Sinewave, 4kHz; CLKIN = 6.144MHz; SCLK = 3.072 MHz; Source Impedance = 50Ω with 10 nF to AGND; Measurement Bandwidth is 10 Hz to 20 kHz; Digital Inputs: Logic 1 = VD+, Logic 0 = DGND; unless otherwise specified.)

Parameter*			Symbol	Specification min	typ	max	Units
Resolution		CS5326, CS5327		16			Bits
		CS5328, CS5329		18			Bits
Dynamic Performance							
Dynamic Range		CS5326, CS5327		92.7	95.7		dB
		CS5328, CS5329		94.7	97.1		dB
(Note 1)	Mono	CS5328, CS5329			100.1		dB
Signal-to-		CS5326, CS5327		90.7	92.7		dB
(Noise + Distortion)		CS5328, CS5329	S/(N+D)	92.5	94.5		dB
(Note 1)	Mono	CS5328, CS5329			97		dB
Total Harmonic Distortion							
Vin = ± FS			THD	0.003	0.0015		%
Vin = -20 dB					0.001		%
Interchannel Phase Deviation					0.0001		Degrees
Interchannel Isolation (dc to 20 kHz)				100	106		dB
dc Accuracy							
Interchannel Gain Mismatch					0.01	0.05	dB
Gain Error					± 1	± 5	%
Gain Drift					50		ppm/ °C
Bipolar Offset Error		CS5326, CS5327			± 5	± 15	LSB (16-bit)
(After Calibration)		CS5328, CS5329			± 20	± 60	LSB (18-bit)
Analog Input							
Input Voltage Range	(± Full Scale)		VIN	± 3.50	± 3.68		Volts
Input Impedance			ZIN		65		kΩ
Power Supplies							
Power Supply Current	(VA+) + (VL+)		IA+		25	35	mA
with APD,DPD low	VA-		IA-		25	35	mA
(Normal Operation)	(VD1+) + (VD2+)		ID+		40	55	mA
Power Supply Current	(VA+) + (VL+)		IA+		10	15	uA
with APD,DPD high	VA-		IA-		10	15	uA
(Power-Down Mode)	(VD1+) + (VD2+)		ID+		5	7	mA
Power Consumption	(APD, DPD Low)		PDN		450	625	mW
	(APD, DPD High)		PDS		25	35	mW
Power Supply Rejection Ratio (dc to 26 kHz)			PSRR		54		dB
(26 kHz to 3.046 MHz)					100		dB

Notes: 1. Mono means connecting AINL & AINR together and adding together the output words from each channel.

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 ° C; VA+, VL+ ,VD1+,VD2+= 5V ± 5%; VA- = -5V ± 5%; CLKIN = 6.144MHz)

Parameter		Symbol	Min	Typ	Max	Units
Passband (-3 dB)	CS5326, CS5328		0		23.5	kHz
(-3 dB)	CS5327, CS5329		0		21.6	kHz
(-0.001 dB)	CS5326, CS5328		0		21.8	kHz
(-0.001 dB)	CS5327, CS5329		0		20.0	kHz
Passband Ripple					0.001	dB
Stopband	CS5326, CS5328		26		3046	kHz
	CS5327, CS5329		24		3052	kHz
Stopband Attenuation	(Note 2)		86			dB
Group Delay		t_{gd}		4274/CLKIN		s
Group Delay Variation vs. Frequency		$\triangle t_{gd}$			0.0	us

Notes: 2. The analog modulator samples the input at 3.072MHz for a CLKIN of 6.144MHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 3.072MHz ±21.8kHz for the CS5326 & CS5328, or n x 3.072MHz ±20.0kHz for the CS5327 & CS5329 , where n = 0,1,2,3...).

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD1+,VD2+= 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (CLKIN)	V_{IH}	(VD+) - 1.0	-	-	V
Low-Level Input Voltage (CLKIN)	V_{IL}	-	-	1.0	V
High-Level Input Voltage (except CLKIN)	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage (except CLKIN)	V_{IL}	-	-	30% VD+	V
High-Level Output Voltage at Io = -20uA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20uA	V_{OL}	-	-	0.1	V
Input Leakage Current	Iin	-	1.0	-	uA

RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD1+,VD2+	4.75	5.0	5.25	V
	Positive Logic	VL+	4.75	5.0	VA+	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	-4.75	-5.0	-5.25	V
Analog Input Voltage	(Note 3)	V_{AIN}	-3.68	-	3.68	V
CLKIN Frequency		f_{CLK}	3.84	-	6.4	MHz
SCLK Frequency		f_{SCLK}	f_{CLK} /2	-	f_{CLK}	Hz
L/$\overline{R}$ Frequency		$f_{L/\overline{R}}$	f_{CLK} /128	-	f_{CLK} /128	Hz

Notes: 3. The ADCs accept input voltages up to the analog supplies (VA+, VA-). They will produce a positive full-scale output for inputs above 3.68 V and negative full-scale output for inputs below -3.68 V. These values are subject to the gain error tolerance specification.

SWITCHING CHARACTERISTICS

(T_A = 25 °C; VA+, VL+, VD1+ , VD2+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20 pF)

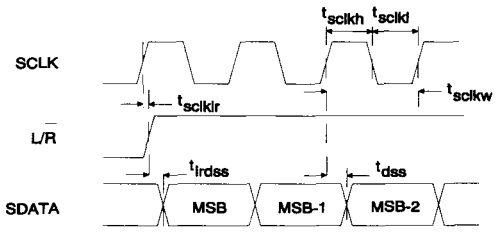
Parameter	Symbol	Min	Typ	Max	Units
CLKIN Period	t_{clkw}	155	-	260	ns
CLKIN Low	t_{clkl}	50	-	-	ns
CLKIN High	t_{clkh}	50	-	-	ns
CLKIN Rising to ACLKA edge (Note 4)	t_{clka}	40	-	100	ns
ACLKA Falling to L/$\overline{R}$ Edge (Note 4)	t_{aclr}	-140	-	140	ns
CLKIN Rising to L/$\overline{R}$ Edge (Note 4) ACLKA to CLKIN phase correct ACLKA to CLKIN phase unknown	t_{clr}	 -10 -10	 - -	 170 30	ns
SCLK Pulse Width Low	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High	t_{sclkh}	60	-	-	ns
SCLK Period	t_{sclkw}	155	-	-	ns
SCLK Rising to SDATA Valid	t_{dss}	-	-	45	ns
L/$\overline{R}$ edge to MSB Valid	t_{lrdss}	-	-	50	ns
SCLK Rising to L/$\overline{R}$ edge	t_{sclklr}	-40	-	40	ns
DPD, APD pulse width	t_{pd}	150	-	-	ns
CLKIN Falling to APD Falling	t_{apdclk}	-30	-	30	ns

Notes: 4. It is recommended that L/$\overline{R}$ be generated by dividing ACLKA by 64. If CLKIN is used to generate L/$\overline{R}$, a longer CLKIN to L/$\overline{R}$ delay may be tolerated if the phase of ACLKA is determined through the use of the APD pin. When high, the APD pin resets the divide-by-two circuit that generates ACLKA from CLKIN (that is, ACLKA is reset to "0"). APD should be brought low on a falling edge of CLKIN. This falling edge should be chosen such that L/$\overline{R}$ edges nominally occur at ACLKA falling edges.

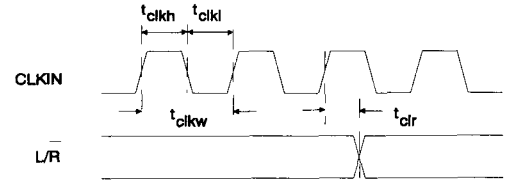
ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	+6.0	V
	Negative Analog	VA-	+0.3	-6.0	V
	Positive Logic	VL+	-0.3	(VA+) + 0.3	V
	Positive Digital	VD1+,VD2+	-0.3	+6.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	± 10	mA
Analog Input Voltage (AIN and ZERO pins)		V_{INA}	(VA-)- 0.3	(VA+)+ 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VD+) + 0.3	V
Ambient Temperature (power applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

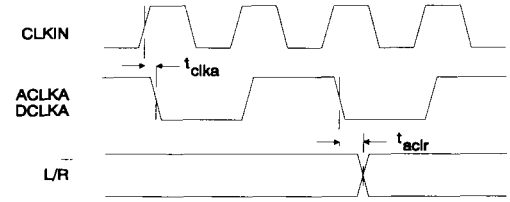
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.



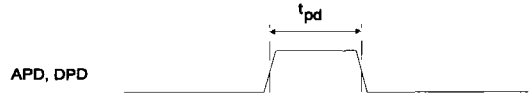
Serial Data Timing



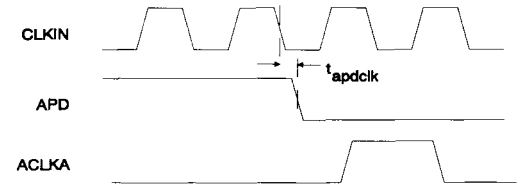
Channel Selection Timing Using L/R Derived From CLKIN/128



Channel Selection Timing Using L/R Derived from ACLKA/64



Power Down Timing



ACLKA Phase Determination using APD

GENERAL DESCRIPTION

The CS5326, CS5327, CS5328 and CS5329 are 16 & 18-bit, 2-channel A/D converters designed specifically for stereo digital audio applications. The devices use two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64× sampling rate. A three-stage digital filter then constructs pairs of 16-bit or 18-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for an input signal range of ± 3.68 volts. Any zero offset can be internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16 or 18-bit numbers. Typical power consumption of only 450 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside these

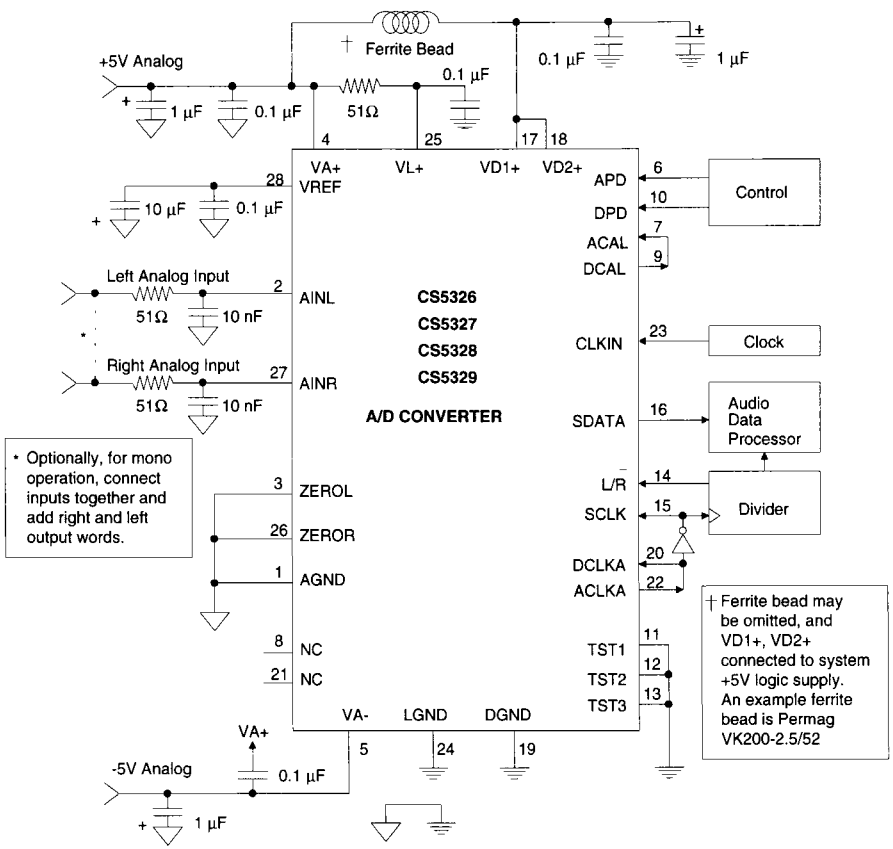


Figure 1. Typical Connection Diagram

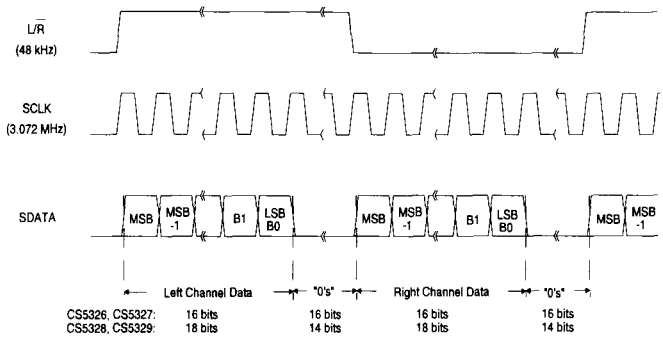


Figure 2. Data Output Timing

ADCs, see the references at the end of this data sheet.

SYSTEM DESIGN WITH THE CS5326/7/8/9

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required.

Clocks and Data Output Format

All timing and control inputs to the ADC can be easily generated from a master system clock. This clock, connected to the CLKIN pin on the device, must be exactly equal to 128 times the desired output word rate. Standard digital audio rates are 32 kHz, 44.1 kHz and 48 kHz, requiring master clock rates of 4.096 MHz, 5.6448 MHz and 6.144 MHz, respectively.

The CLKIN signal should be greater than 4 volts for a logic one and less than 1 volt for a logic zero. This is to minimize any clock related jitter in the sampling process, which can smear high frequency signals. Indeed, a low jitter (such as a crystal-based) clock is recommended.

Data bits are clocked out via the SDATA pin using the SCLK and L/$\overline{R}$ inputs. The rising edge of SCLK causes the part to output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge. Even so, a rising SCLK edge must occur coincident (within the timing tolerance) with the L/$\overline{R}$ edge for internal housekeeping purposes.

It is recommended to connect SCLK to ACLKA, as shown in Figure 1. Fourteen or sixteen trailing zero's will be clocked out on SDATA as part of each data word, as shown in Figure 2. ACLKA's frequency is the analog modulator sampling rate, and if a lower frequency is used for SCLK, slight degradation of the ADC dynamic range can occur due to interference effects.

Selection of left channel or right channel data is accomplished using the L/$\overline{R}$ input pin. The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled inputs.

Rising edges of L/$\overline{R}$ are used to synchronize the digital filter; therefore L/$\overline{R}$'s frequency must be CLKIN/128. It is preferable to generate L/$\overline{R}$ by dividing ACLKA by 64. If CLKIN is used to generate L/$\overline{R}$, it is best to determine the phase of ACLKA through the use of the APD pin. (When high, the APD pin resets the internal divide-by-two circuit that generates ACLKA. See Figure 4 for an example circuit.) If ACLKA phase is left indeterminate, then the CLKIN to L/$\overline{R}$ delay must

be shorter than the smaller delay shown in the Switching Characteristics table (see Note 4.).

Analog Connections

The analog inputs are presented to the modulators via the AINR and AINL pins. The analog input signal range is determined by the internal voltage reference value, which is typically -3.68 volts. The input signal range therefore is typically ± 3.68 volts.

The ADC samples the analog inputs at 3.072 MHz for a 6.144 MHz CLKIN. For the CS5326 & CS5328 the digital filter rejects all noise between 26 kHz and (3.072 MHz-26 kHz). For the CS5327 & CS5329 the digital filter rejects all noise between 24 kHz and (3.072 MHz-24 kHz). However, the filter will not reject frequencies right around 3.072 MHz. Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 51 Ω resistor in series with the analog input, and a 10 nF NPO or COG capacitor to ground will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins.

The on-chip voltage reference output is brought out to the VREF pin. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Note the negative value of VREF when using polarized capacitors. No load current may be taken from the VREF output pin.

The analog input level used as zero during the offset calibration period (described later) is input on the ZEROL and ZEROR pins. Typically, these pins are directly attached to AGND. For the ultimate in offset nulling, networks can be attached to ZEROR and ZEROL whose impedances match the impedances present on AINL and AINR.

Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 20 mW. In addition, exiting the power-down state initiates the offset calibration procedure. This can be important for digital audio applications since any initial offset manifests itself as an audible power-on click.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle, whereas APD going low sets the phase of the ACLKA signal. If not using the power down feature and if not using APD to set the phase of ACLKA, APD should be tied to ground. When using the power down feature, DPD and APD may be tied together if the capacitor on VREF is not greater than 10 µF, as stated in the "Power-Up Considerations" section.

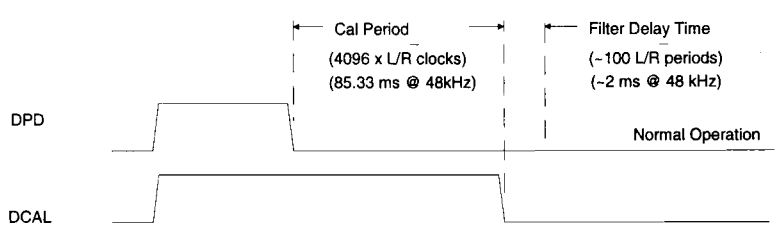


Figure 3. Initial Calibration Cycle Timing

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AINL and AINR) or the zero pins (ZEROL and ZEROR) depending on the state of the ACAL pin. With ACAL low, the analog input pin voltages are measured, and with ACAL high, the zero pin voltages are measured.

As shown in Figure 3, the DCAL output is high during calibration, which takes 4096 L/$\overline{R}$ clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage on ZEROR and ZEROL. These should be connected directly to ground or through a network matched to that present on the analog input pins. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to ground the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present on the front end.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any power-on click that might otherwise be experienced. A short delay of approximately 100 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals. The transition is simply the natural filter response and is, of course, graceful.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference, however, can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/µF. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10 µF. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows powering the part from single ± 5 volt supplies. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. The VREF decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from VREF to Pin 1 AGND and to minimize the path between VREF and the capacitors.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Multiple ADC's

In systems where multiple ADC's are used, care must be taken to ensure that the ACLKA phases are synchronized if simultaneous sampling is desired. In the absence of this synchronization, the sampling difference could be one CLKIN cycle (typically 162 ns). If this difference is unacceptable, the parts may be synchronized to within several nanoseconds by using the circuit shown in Figure 4. This circuit ensures that when the ADC's come out of power-down mode, ACLKA will have the same phase between all ADC's. The APD signal is used to reset the internal divide-by-two flip-flop which generates ACLKA. The circuit also ensures that $L/\overline{R}$ and SCLK occur at the correct time.

PERFORMANCE

FFT Tests

For FFT based tests, a very pure sine wave is presented to the ADC, and an FFT analysis is performed on the output data. The resulting spectrum is a measure of the performance of the ADC.

Figure 5 shows the spectral purity of the CS5326 with a 1 kHz, -10 dB input. Notice the low noise floor, the absence of any harmonic distortion, and the Dynamic Range value of 94.63 dB.

Figure 6 shows the CS5326 high frequency performance. The input signal is a -10 dB, 9 kHz sine wave. Notice the small 2nd harmonic at -112 dB.

Figure 7 shows the low-level performance of the CS5326. Notice the lack of any distortion components. Traditional R-2R ladder based ADC's can have problems with this test, since differential non-linearities around the zero point become very significant. Figure 8 shows the same very low input amplitude performance, but at 9kHz input frequency.

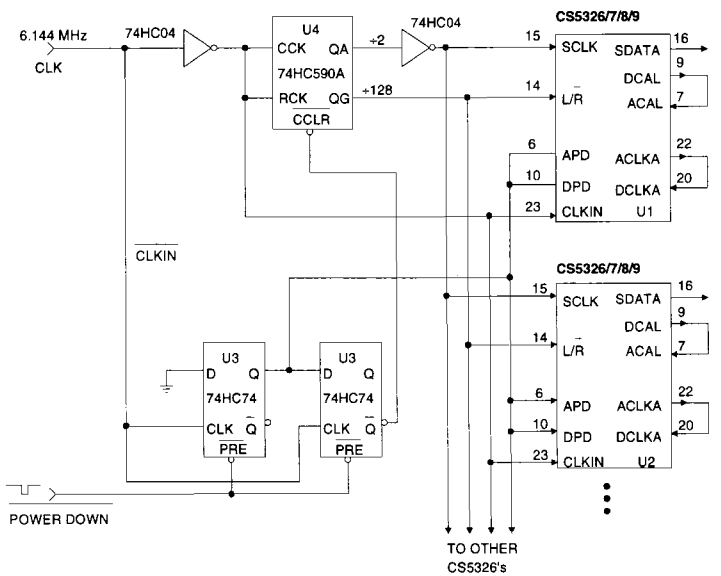


Figure 4. Connections for Synchronization of Multiple CS5326/7/8/9 ADC's.

Figure 9 shows the CS5327 FFT plot with an input signal of 1 kHz at -10 dB. This is very similar to the CS5326 plot, but notice the reduction in the noise floor between 22 kHz and 24 kHz. This is caused by the digital filter attenuating the noise in its transition band.

Figure 10 shows a plot of Signal to (Noise + Distortion) versus input amplitude relative to full

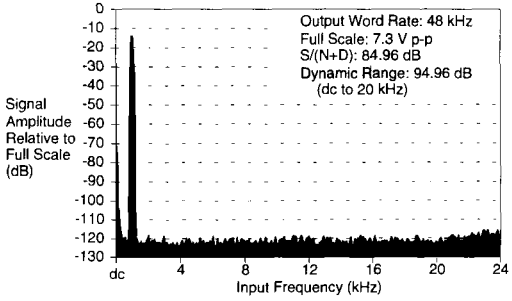


Figure 5. CS5326 FFT Plot with -10 dB, 1 kHz Input

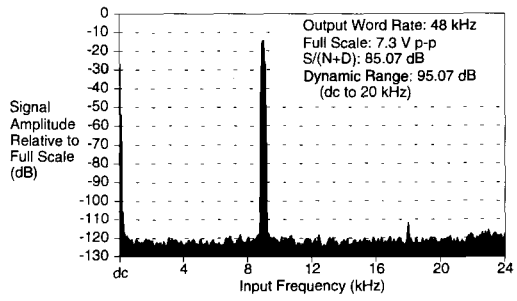


Figure 6. CS5326 FFT Plot with -10 dB, 9 kHz Input

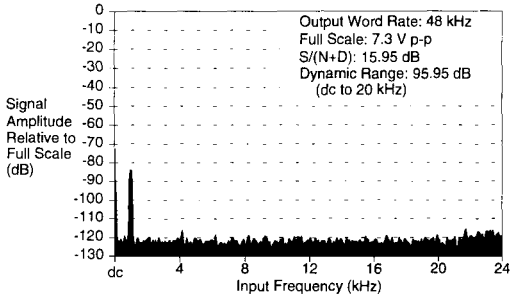


Figure 7. CS5326 FFT Plot with -80 dB, 1 kHz Input

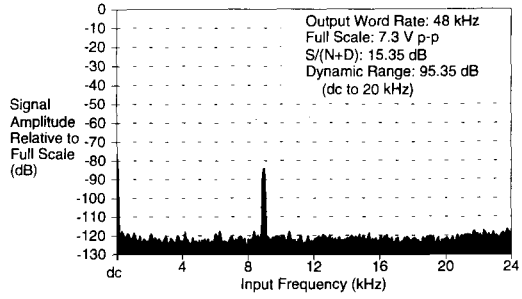


Figure 8. CS5326 FFT Plot with -80 dB, 9 kHz Input

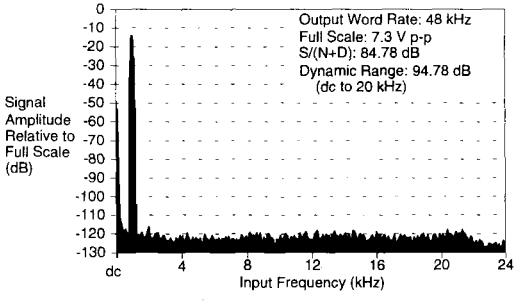


Figure 9. CS5327 FFT Plot with -10 dB, 1 kHz Input

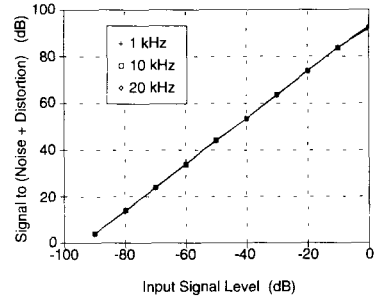


Figure 10. CS5326, CS5327 Signal to Noise+Distortion Ratio vs. Input Level

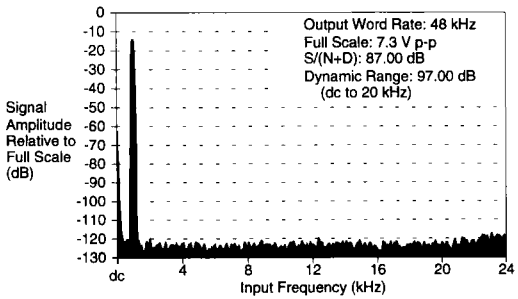


Figure 11. CS5328 FFT Plot with -10 dB, 1 kHz Input

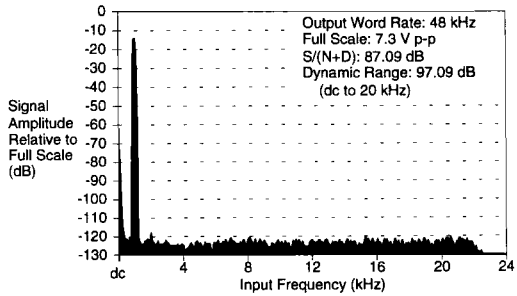


Figure 12. CS5329 FFT Plot with -10 dB, 1 kHz Input

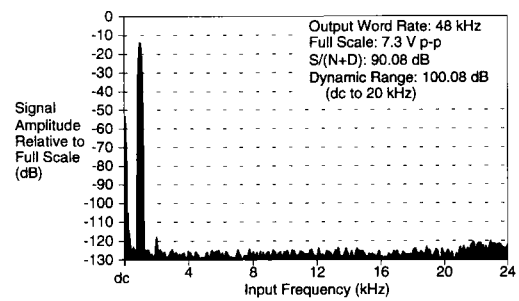


Figure 13. CS5328 in Mono Mode FFT Plot with -10 dB, 1 kHz Input

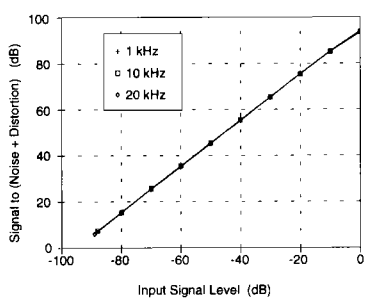


Figure 14. CS5328 Signal to Noise+Distortion Ratio vs. Input Level

scale. For an ideal ADC, this plot would be a straight line at 45° for all input frequencies between dc and half the output word rate. The measured data from a CS5326 shows both the excellent high frequency performance as well as the maintenance of good performance with low input levels.

Figure 11 shows the18-bit CS5328 FFT plot. Notice the 2 dB improvement in dynamic range over the CS5326.

Figure 12 shows the18-bit CS5329 FFT plot. Notice the filter cut-off at 22 kHz, and the 2 dB improvement in dynamic range over the CS5327.

Figure 13 shows the CS5328 operated in 19-bit mono mode, with the two inputs joined together, and the output words added. Notice the 3 dB improvement over Figure 11.

Figure 14 shows a plot of Signal to Noise + Distortion versus Input Level for the 18-bit CS5328. Notice the improvement in values over Figure 10.

DNL Tests

A Differential Non-Linearity test is also shown. Here, the converter is presented with a linear ramp signal. The resulting output codes are counted to yield a number which is proportional to the codewidth. A plot of codewidth versus code graphically illustrates the uniformity of the

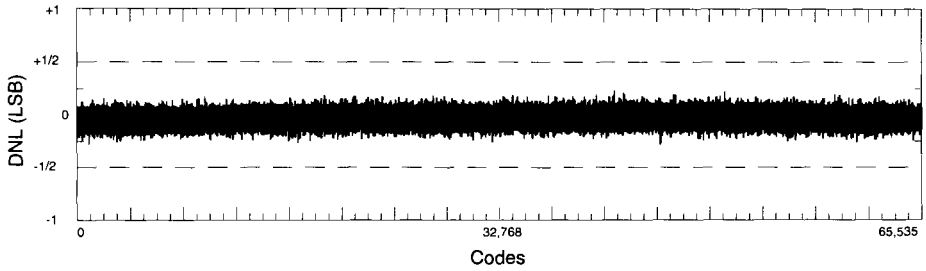


Figure 15. CS5326 Differential Non-Linearity Plot

codewidths. Figure 15 shows the excellent Differential Non-Linearity of the CS5326. This plot displays the worst case positive and negative errors in each of 512 groups of 128 codes. Codewidths typically are within ± 0.2 LSB's of ideal. A delta-sigma modulator based ADC has no inherent mechanism for generating DNL errors. The residual small deviations shown in Figure 10 are a result of noise. Nevertheless, the performance shown is extremely good, and is superior to typical R-2R ladder based designs.

Digital Filter

Figures 16 through 21 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz, with a CLKIN frequency of 6.144 MHz. The filter frequency response will scale precisely with changes in CLKIN frequency. The passband ripple is flat to ±0.001 dB maximum. Stopband rejection is greater than 86 dB.

Figures 16,18 &20 show the CS5326 and CS5328 filter characteristics. Figure 20 is an expanded view of the transition band.

Figures 17,19 & 21 show the CS5327 and CS5329 filter characteristics. Figure 21 is an expanded view of the transition band. Notice how the filter enters the stopband at exactly 24 kHz, which is half the output word rate, thereby guaranteeing no aliasing.

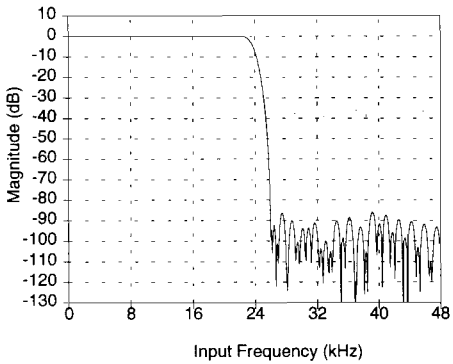


Figure 16. CS5326 /8 Digital Filter Stopband Rejection

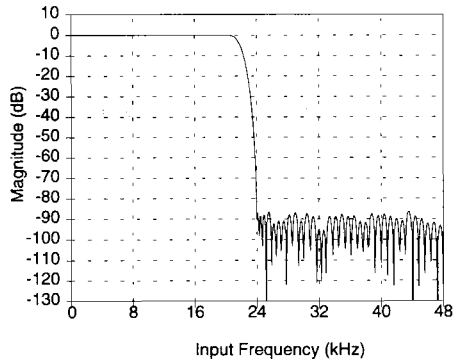


Figure 17. CS5327/9 Digital Filter Stopband Rejection

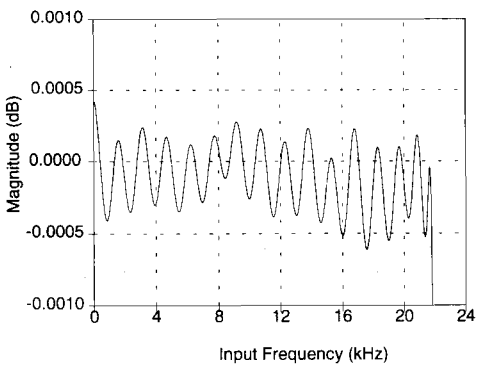


Figure 18. CS5326/8 Digital Filter Passband Ripple

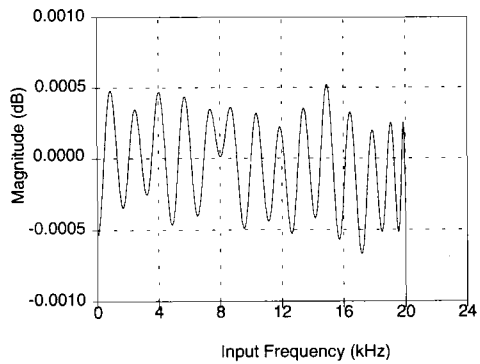


Figure 19. CS5327/9 Digital Filter Passband Ripple

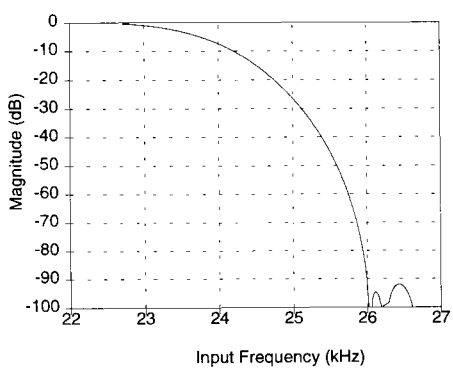


Figure 20. CS5326/8 Digital Filter Transition Band

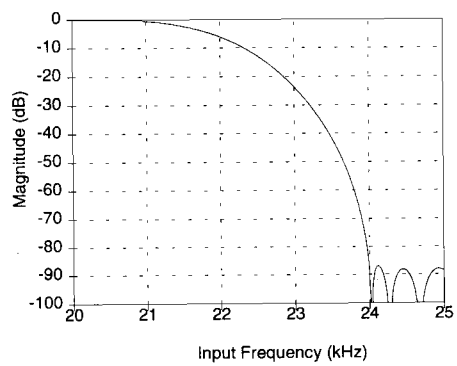
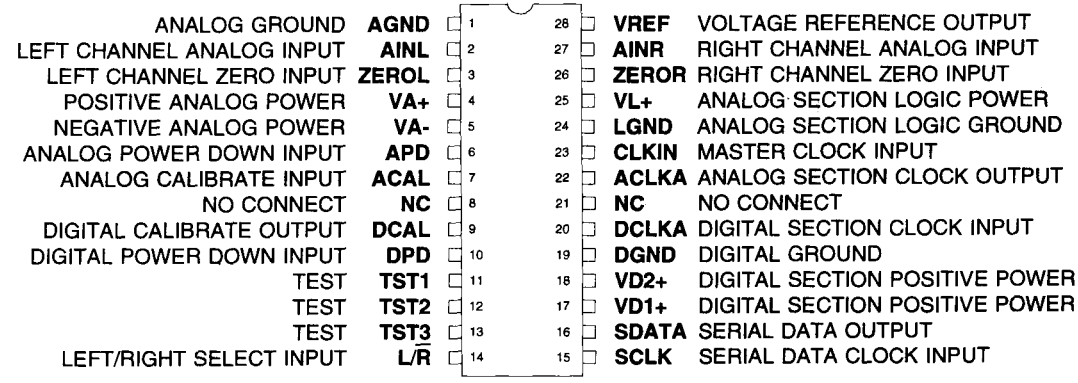


Figure 21. CS5327/9 Digital Filter Transition Band

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 4.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 25.
Positive logic supply for the analog section. Nominally +5 volts.

VA- - Negative Analog Power, PIN 5.
Negative analog supply. Nominally -5 volts.

AGND - Analog Ground, PIN 1.
Analog ground reference.

LGND - Logic Ground, PIN 24
Ground for the logic portions of the analog section.

VD1+, VD2+ - Positive Digital Power, PINS 17, 18.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 19.
Digital ground for the digital section.

Analog Inputs

AINL, AINR - Left and Right Channel Analog Inputs, PINS 2, 27
Analog input connections for the left and right input channels. Nominally ±3.68 volts full scale.

ZEROL, ZEROR - Zero Level Inputs for Left and Right Channels, PINS 3, 26.

Analog zero level inputs for the left and right channels. The levels present on these pins can be used as zero during the offset calibration cycle. Normally connected to AGND, optionally through networks matched to the analog input networks..

Analog Outputs

VREF - Voltage Reference Output, PIN 28.

Nominally -3.68 volts. Normally connected to a 0.1µF ceramic capacitor in parallel with a 10µF or larger electrolytic capacitor. Note the negative output polarity.

Digital Inputs

CLKIN - Master Input Clock, PIN 23.

This clock is internally divided by 2 to set the modulators sample rate. Sampling rates, output rates, and digital filter characteristics scale to CLKIN frequency. CLKIN frequency of 6.144 MHz corresponds to an output word rate of 48 kHz per channel.

DCLKA - Digital Section Input Clock, PIN 20.

This clock is used to clock the modulator output data into the digital section. Must be connected to ACLKA.

SCLK - Serial Output Data Clock, PIN 15.

Data bits are output on the rising edge of SCLK.

L/$\overline{R}$ - Left/Right Select, PIN 14.

Select the left or right channel for output on SDATA. The rising edge of L/$\overline{R}$ starts the MSB of the left channel data. Thereafter, CLKIN, SCLK and L/$\overline{R}$ should run synchronously. L/$\overline{R}$ must be equal to CLKIN/128. Although the outputs of each channel are transmitted at different times, the two words in a L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

APD - Analog Power Down, PIN 6.

Analog section power-down command. When high the analog circuitry is in power-down mode. It also causes the analog section to reset the clock output (ACLKA). APD is normally connected to DPD when using the power down feature.

DPD - Digital Power Down, PIN 10

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 L/$\overline{R}$ periods (85.33 ms with a 6.144 MHz clock). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 7.

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to ZEROL and ZEROR inputs respectively. May be connected to DCAL.

Digital Outputs

ACLKA - Analog Section Output Clock, PIN 22.

This clock is CLKIN/2. It is used by the digital section to clock in the modulator output data. ACLKA must be connected to DCLKA. The phase of ACLKA may be reset by using APD.

SDATA - Serial Data Output, PIN 16.

Data bits are presented MSB first, in 2's complement format.

DCAL - Digital Calibrate Output, PIN 9.

This pin rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 $\overline{L/R}$ periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 6.144 MHz CLKIN). May be connected to ACAL. (See Figure 3)

Miscellaneous

NC - No Connection, PINS 8,21.

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

TST1, TST2, TST3 -Test Inputs, PINS 11, 12, 13.

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Signal-to-Noise plus Distortion Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Dynamic Range - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error -The deviation of the gain value from the typical number given in the analog specifications table.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

Differential Non-Linearity - The deviation of a code's width from the ideal width. Units in LSB's.

REFERENCES **(All reprinted in the back of this data book)**

1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

2) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

3) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

Ordering Guide

Model	Resolution	Filter Enters Stopband	Temperature	Package
CS5326-KP	16-bits	26 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5327-KP	16-bits	24 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5328-KP	18-bits	26 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5329-KP	18-bits	24 kHz	0°C to 70 °C	28-pin Plastic DIP

CDB5326	CS5326 Evaluation Board
CDB5327	CS5327 Evaluation Board
CDB5328	CS5328 Evaluation Board
CDB5329	CS5329 Evaluation Board