CS5490

Two Channel Energy Measurement IC

Features

- Superior Analog Performance with Ultra-low Noise Level & High SNR
- Energy Measurement Accuracy of 0.1% over a 4000:1 Dynamic Range
- Two Independent 24-bit, 4th-order, Delta-Sigma Modulators for Voltage and Current Measurements
- Configurable Digital Output for Energy Pulses, Interrupt, zero-crossing, and Energy Direction
- Supports Shunt Resistor, CT, and Rogowski Coil Current Sensors
- On-chip Measurements/Calculations:
  - Active, Reactive, and Apparent Power
  - RMS Voltage and Current
  - Power Factor and Line Frequency
  - Instantaneous Voltage, Current, and Power
- Overcurrent, Voltage Sag, and Voltage Swell Detection
- Ultra-fast On-chip Digital Calibration
- Configurable No-load Threshold for Anti-creep
- Internal Register Protection via Checksum and Write Protection
- UART Serial Interface
- On-chip Temperature Sensor
- On-chip Voltage Reference (25ppm/°C Typ.)
- Single 3.3 V Power Supply
- Ultra-fine Phase Compensation
- Low Power Consumption: <13 mW
- Power Supply Configurations:
  - GNDA = 0 V, VDDA: +3.3 V
- Low-cost 16-pin SOIC Package

Description

The CS5490 is a high-accuracy, two-channel, energy measurement analog front end.

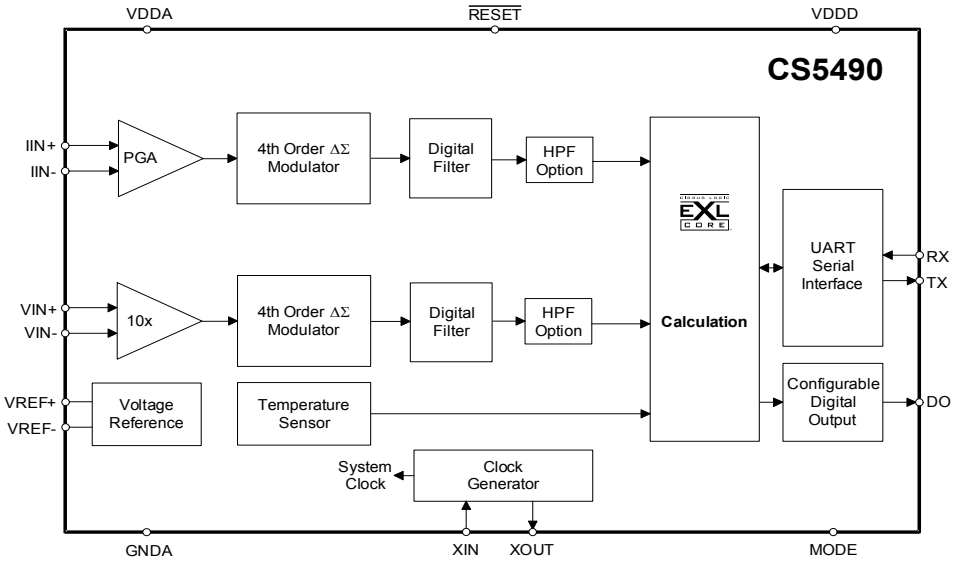
The CS5490 incorporates independent 4th order Delta-Sigma analog-to-digital converters for both channels, reference circuitry, and the proven EXL signal processing core to provide active, reactive, and apparent energy measurement. In addition, RMS and power factor calculations are available. Calculations are output via a configurable energy pulse, or direct UART serial access to on-chip registers. Instantaneous current, voltage, and power measurements are also available over the serial port. The two-wire UART minimizes the cost of isolation where required.

A configurable digital output provides energy pulses, zero-crossing, energy direction, or interrupt functions. Interrupts can be generated for a variety of conditions including voltage sag or swell, overcurrent, and more. On-chip register integrity is assured via checksum and write protection. The CS5490 is designed to interface to a variety of voltage and current sensors, including shunt resistors, current transformers, and Rogowski coils.

On-chip functionality makes digital calibration simple and ultra fast to minimize the time required at the end of the customer production line. Performance across temperature is ensured with an on-chip voltage reference with low drift. A single 3.3V power supply is required, and power consumption is low at <13mW. To minimize space requirements, the CS5490 is offered in a low-cost 16-pin SOIC package.

ORDERING INFORMATION

See Page 57.



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1. OVERVIEW

The CS5490 is a CMOS power measurement integrated circuit that uses two ΔΣ analog-to-digital converters to measure line voltage and current. The CS5490 calculates active, reactive, and apparent power as well as RMS voltage and current and peak voltage and current. It handles other system-related functions, such as energy pulse generation, voltage sag and swell, overcurrent and zero-crossing detection, and line frequency measurement. A separate analog-to-digital converter is used for on-chip temperature measurement.

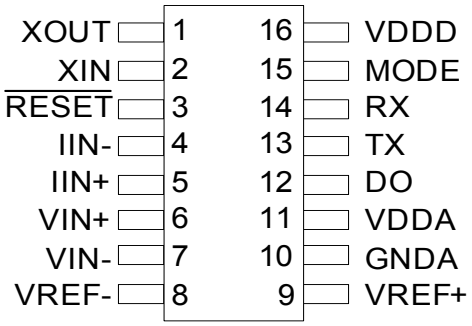
The CS5490 is optimized to interface to current transformers, shunt resistors, or Rogowski coils for current measurement, and to resistive dividers or voltage transformers for voltage measurement. Two full-scale ranges are provided on the current input to accommodate different types of current sensors. The CS5490's two differential inputs have a common-mode input range from analog ground (GNDA) to the positive analog supply (VDDA).

An on-chip voltage reference (typically 2.4 volts) is generated and provided at analog output, VREF±.

The digital output (DO) provides a variety of output signals and, depending on the mode selected, provides energy pulses, zero-crossings, or other choices.

The CS5490 includes a UART serial host interface to an external microcontroller. The UART signals include serial data input (RX) and serial data output (TX).

2. PIN DESCRIPTION



Clock Generator		
Crystal In **Crystal Out**	2,1	**XIN, XOUT** — Connect to an external quartz crystal. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
Control Pins and Serial Data I/O		
Digital Output	12	**DO** — Configurable digital output for energy pulses, interrupt, energy direction, and zero-crossings.
Reset	3	**$\overline{\text{RESET}}$** — An active-low Schmitt-trigger input used to reset the chip.
Serial Interface	13,14	**TX, RX** — UART serial data output/input.
Operating Mode Select	15	**MODE** — Connect to VDDA for proper operation.
Analog Inputs/Outputs		
Voltage Input	6,7	**VIN+, VIN-** — Differential analog input for the voltage channel.
Current Input	5,4	**IIN+, IIN-** — Differential analog input for the current channel.
Voltage Reference Input	9,8	**VREF+, VREF-** — The voltage reference output and return.
Power Supply Connections		
Internal Digital Supply	16	**VDDD** — Decoupling pin for the internal digital supply.
Positive Analog Supply	11	**VDDA** — The positive analog supply.
Analog Ground	10	**GNDA** — Analog ground.

2.1 Analog Pins

The CS5490 has two differential inputs, one for voltage (VIN±) and one for current (IIN±). The CS5490 also has two voltage reference pins (VREF±) between which a 0.1µ bypass capacitor must be placed.

2.1.1 Voltage Input

The output of the line voltage resistive divider or transformer is connected to the VIN± input of the CS5490. The voltage channel is equipped with a 10x, fixed-gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±250 mV. If the input signal is a sine wave, the maximum RMS voltage is $250\,\text{mVp} / \sqrt{2} \approx 176.78\,\text{mV}_{\text{RMS}}$, which is approximately 70.7% of maximum peak voltage.

2.1.2 Current Input

The output of the current-sensing shunt resistor or transformer is connected to the IIN± input pins of the CS5490. To accommodate different current-sensing elements, the current channel incorporates a programmable gain amplifier (PGA) with two selectable input gains, as described in the *Config0* register description *6.6.1 Configuration 0 (Config0) – Page 0, Address 0* on page 32. There is a 10x gain setting and a 50x gain setting. The full-scale signal level for the current channel is ±50 mV and ±250 mV for 50x and 10x gain settings, respectively. If the input signal is a sine wave, the maximum RMS voltage is $35.35\,\text{mV}_{\text{RMS}}$ or $176.78\,\text{mV}_{\text{RMS}}$, which is approximately 70.7% of maximum peak voltage.

2.1.3 Voltage Reference

The CS5490 generates a stable voltage reference of 2.4V between the VREF± pins. The reference system also requires a filter capacitor of at least 0.1µF between the VREF± pins.

The reference system is capable of providing a reference for the CS5490 but has limited ability to drive external circuitry. It is strongly recommended that nothing other than the required filter capacitor is connected to the VREF± pins.

2.1.4 Crystal Oscillator

An external, 4.096MHz quartz crystal can be connected to the XIN and XOUT pins as shown in Figure 1. To reduce system cost, each pin is supplied with an on-chip load capacitor.

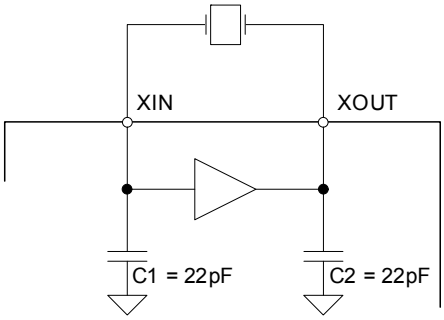


Figure 1. Oscillator Connections

Alternatively, an external clock source can be connected to the XIN pin.

2.2 Digital Pins

2.2.1 Reset Input

The active-low $\overline{\text{RESET}}$ pin, when asserted for longer than 120µs, will halt all CS5490 operations and reset internal hardware registers and states. When de-asserted, an initialization sequence begins, setting the default register values. To prevent erroneous, noise-induced resets to the part, an external pull-up resistor and a decoupling capacitor are necessary on the $\overline{\text{RESET}}$ pin.

2.2.2 Digital Output

The CS5490 provides a configurable digital output (DO). It can be configured to output energy pulses, interrupt, zero-crossings, or energy directions. Refer to the description of the *Config1* register in section *6.6 Register Descriptions* on page 32 for more details.

2.2.3 UART Serial Interface

The CS5490 provides two pins, RX and TX, for communication between a host microcontroller and the CS5490.

2.2.3.1 UART

The CS5490 provides a two-wire, asynchronous, full-duplex UART port. The CS5490 UART operates in 8-bit mode, which transmits a total of 10 bits per byte. Data is transmitted and received LSB first, with one start bit, eight data bits, and one stop bit.

Figure 2. UART Serial Frame Format

The baud rate is defined in the *SerialCtrl* register. After chip reset, the default baud rate is 600, if MCLK is 4.096MHz. The baud rate is based on the contents of bits BR[15:0] in the *SerialCtrl* register and is calculated as follows:

$$BR[15:0] = \text{Baud Rate} \times (524288/MCLK)$$

or

$$\text{Baud Rate} = BR[15:0] / (524288/MCLK)$$

The maximum baud rate is 512K if MCLK is 4.096MHz.

The UART has two signals: TX and RX. TX is the serial data output from the CS5490; RX is the serial data input to the CS5490.

2.2.4 MODE Pin

The MODE pin must be tied to VDDA for normal operation. The MODE pin is used primarily for factory test procedures.

3. CHARACTERISTICS & SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Analog Power Supply	VDDA	3.0	3.3	3.6	V
Specified Temperature Range	T_A	-40	-	+85	°C

POWER MEASUREMENT CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Active Energy (Note 1 & 2)	All Gain Ranges Current Channel Input Signal Dynamic Range 4000:1	P_{Avg}	-	±0.1	-	%
Reactive Energy (Note 1 & 2)	All Gain Ranges Current Channel Input Signal Dynamic Range 4000:1	Q_{Avg}	-	±0.1	-	%
Apparent Power (Note 1 & 3)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	S	-	±0.1	-	%
Current RMS (Note 1, 3, & 4)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	I_{RMS}	-	±0.1	-	%
Voltage RMS (Note 1 & 3)	Voltage Channel Input Signal Dynamic Range 20:1	V_{RMS}	-	±0.1	-	%
Power Factor (Note 1 & 3)	All Gain Ranges Current Channel Input Signal Dynamic Range 1000:1	PF	-	±0.1	-	%

Notes:
1. Specifications guaranteed by design and characterization.
2. Active energy is tested with power factor PF = 1.0. Reactive energy is tested with Sin(φ) = 1.0. Energy error measured at system level using single energy pulse. Where: 1) One energy pulse = 0.5Wh or 0.5Varh; 2) VDDA = +3.3V, T_A = 25°C, MCLK = 4.096MHz; 3) System is calibrated.
3. Calculated using register values; N≥4000.
4. I_{RMS} error calculated using register values. 1) VDDA = +3.3V; T_A = 25°C; MCLK = 4.096MHz; 2) AC offset calibration applied.

TYPICAL LOAD PERFORMANCE

- Energy error measured at system level using single energy pulse; where 1 energy pulse = 0.5Wh or 0.5Varh.
- I_{RMS} error calculated using register values
- VDDA = +3.3V; T_A = 25°C; MCLK = 4.096MHz

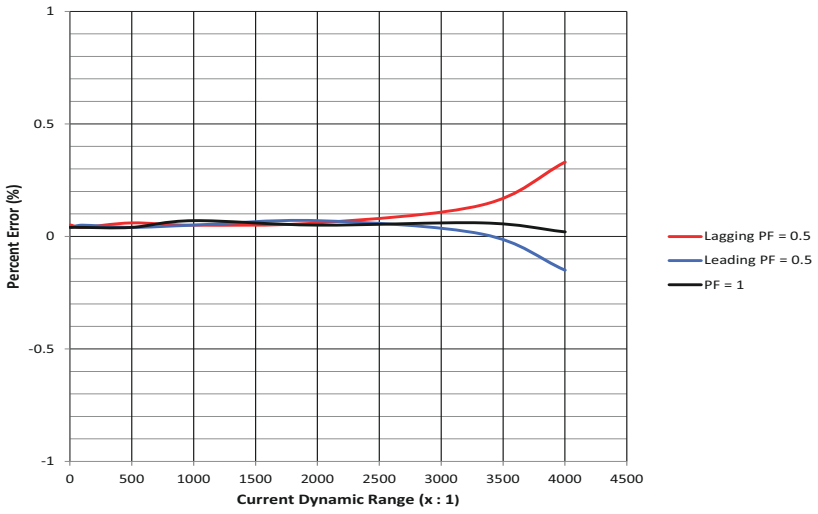


Figure 3. Active Energy Load Performance

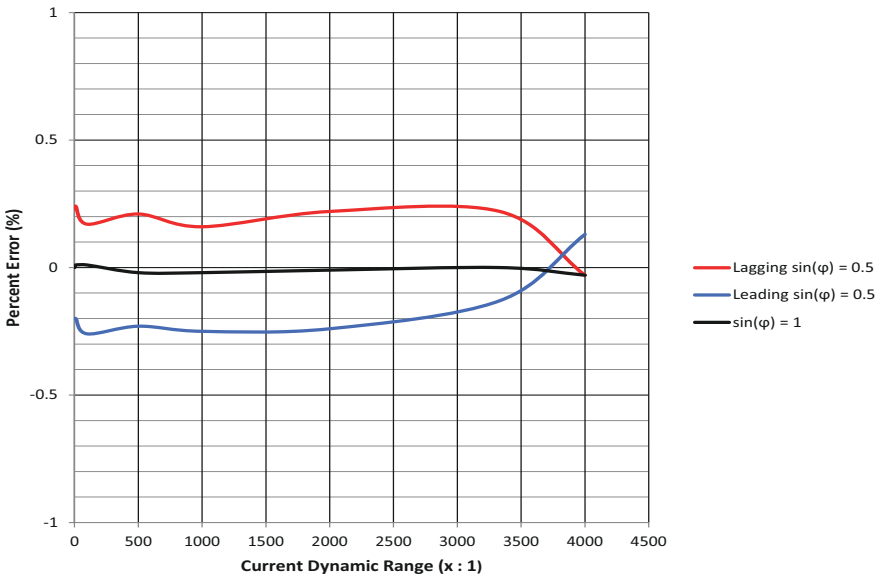


Figure 4. Reactive Energy Load Performance

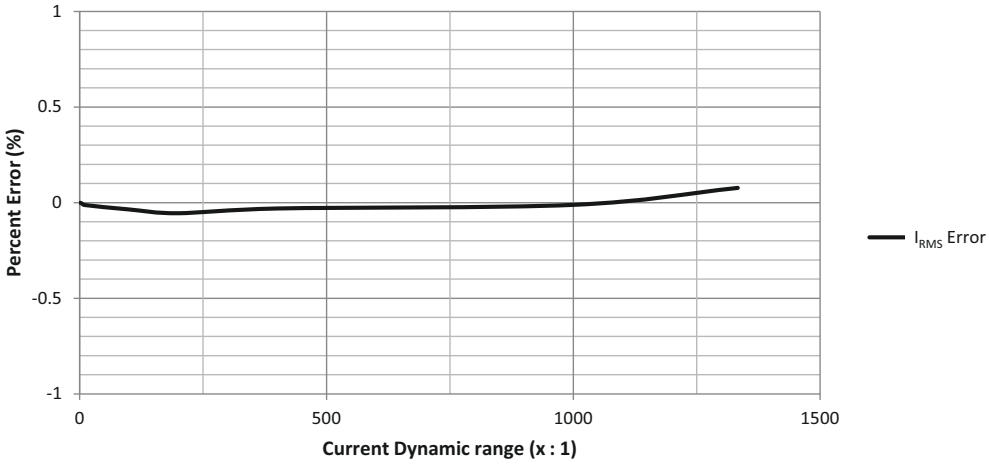


Figure 5. I_{RMS} Load Performance

ANALOG CHARACTERISTICS

- Min/Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = 0V. All voltages with respect to 0V.
- MCLK = 4.096MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Analog Inputs (Current Channels)						
Common Mode Rejection	(DC, 50, 60Hz)	CMRR	80	-	-	dB
Common Mode+Signal			-0.25	-	VDDA	V
Differential Full-scale Input Range [(IIN+) – (IIN-)]	(Gain = 10) (Gain = 50)	IIN	- -	250 50	- -	mV_P mV_P
Total Harmonic Distortion	(Gain = 50)	THD	90	100	-	dB
Signal-to-Noise Ratio (SNR)	(Gain = 10) (Gain = 50)	SNR	- -	80 80	- -	dB dB
Crosstalk from Voltage Inputs at Full Scale	(50, 60Hz)		-	-115	-	dB
Crosstalk from Current Input at Full Scale	(50, 60Hz)		-	-115	-	dB
Input Capacitance		IC	-	27	-	pF
Effective Input Impedance		EII	30	-	-	kΩ
Offset Drift (Without the High-pass Filter)		OD	-	4.0	-	µV/°C
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_I	- -	9 2.2	- -	μV_{RMS} μV_{RMS}
Power Supply Rejection Ratio (Note 7)	(60Hz) (Gain = 10) (Gain = 50)	PSRR	 60 68	 65 75	 - -	 dB dB
Analog Inputs (Voltage Channels)						
Common Mode Rejection	(DC, 50, 60Hz)	CMRR	80	-	-	dB
Common Mode+Signal			-0.25	-	VDDA	V
Differential Full-scale Input Range	[(VIN+) – (VIN-)]	VIN	-	250	-	mV_P
Total Harmonic Distortion		THD	80	88	-	dB
Signal-to-Noise Ratio (SNR)		SNR	-	73	-	dB
Crosstalk from Current Inputs at Full Scale	(50, 60Hz)		-	-115	-	dB
Input Capacitance		IC	-	2.0	-	pF
Effective Input Impedance		EII	2	-	-	MΩ
Noise (Referred to Input)		N_V	-	40	-	μV_{RMS}
Offset Drift (Without the High-pass Filter)		OD	-	16.0	-	µV/°C
Power Supply Rejection Ratio (Note 7)	(60Hz) (Gain = 10)	PSRR	60	65	-	dB
Temperature						
Temperature Accuracy	(Note 6)	T	-	±5	-	°C

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies						
Power Supply Currents (Active State)	I_{A+} (VDDA = +3.3V)	PSCA	-	3.9	-	mA
Power Consumption (Note 5)	Active State (VDDA = +3.3V)	PC	-	12.9	-	mW
	Stand-by State		-	4.5	-	mW

Notes:
5. All outputs unloaded. All inputs CMOS level.
6. Temperature accuracy measured after calibration is performed.
7. Measurement method for PSRR: VDDA = +3.3V, a 150mV (zero-to-peak) (60Hz) sinewave is imposed onto the +3.3V DC supply voltage at the VDDA pin. The "+" and "-" input pins of both input channels are shorted to GNDA. The CS5490 is then commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as V_{eq} PSRR is (in dB):

$$PSRR = 20 \cdot \log\left[\frac{150}{V_{eq}}\right]$$

VOLTAGE REFERENCE

Parameter		Symbol	Min	Typ	Max	Unit
Reference	(Note 8)					
Output Voltage		VREF	+2.3	+2.4	+2.5	V
Temperature Coefficient	(Note 9)	TC_{VREF}	-	25	-	ppm/°C
Load Regulation	(Note 10)	ΔV_R	-	30	-	mV

Notes:
8. It is strongly recommended that no connection other than the required filter capacitor be made to VREF±.
9. The voltage at VREF± is measured across the temperature range. From these measurements the following formula is used to calculate the VREF temperature coefficient:

$$TC_{VREF} = \left(\frac{VREF_{MAX} - VREF_{MIN}}{VREF_{AVG}}\right)\left(\frac{1}{T_A MAX - T_A MIN}\right)(1.0 \times 10^6)$$

10. Specified at maximum recommended output of 1µA sourcing. VREF is a very sensitive signal, the output of the VREF circuit has a very high output impedance so that the 0.1µF reference capacitor provides attenuation even to low frequency noise, such as 50Hz noise on the VREF output. As such VREF intended for the CS5490 only and should not be connected to any external circuitry. The output impedance is sufficiently high that standard digital multi-meters can significantly load this voltage. The accuracy of the metrology IC can not be guaranteed when a multimeter or any component other than the 0.1µF capacitor is attached to VREF. If it is desired to measure VREF for any reason other than a very course indicator of VREF functionality, Cirrus recommends a very high input impedance multimeter such as the Keithley Model 2000 Digital Multimeter be used, but still cannot guarantee the accuracy of the metrology with this meter connected to VREF.

DIGITAL CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = 0V. All voltages with respect to 0V.
- MCLK = 4.096MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Characteristics						
XIN Clock Frequency	Internal Gate Oscillator	MCLK	2.5	4.096	5	MHz
XIN Clock Duty Cycle			40	-	60	%
Filter Characteristics						
Phase Compensation Range	(60Hz, OWR = 4000Hz)		-10.79	-	+10.79	°
Input Sampling Rate			-	MCLK/8	-	Hz
Digital Filter Output Word Rate	(Both channels)	OWR	-	MCLK/1024	-	Hz
High-pass Filter Corner Frequency	-3dB		-	2.0	-	Hz
Input/Output Characteristics						
High-level Input Voltage (All Pins)		V_{IH}	0.6(VDDA)	-	-	V
Low-level Input Voltage (All Pins)		V_{IL}	-	-	0.6	V
High-level Output Voltage (Note 12)	DO, I_{out} = +10mA I_{out} = +5mA	V_{OH}	VDDA-0.3 VDDA-0.3	- -	- -	V V
Low-level Output Voltage (Note 12)	DO, I_{out} = -12mA All Other Outputs, I_{out} = -5mA	V_{OL}	- -	- -	0.5 0.5	V V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-state Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	5	-	pF

Notes: 11. All measurements performed under static conditions.
12. XOUT pin used for crystal only. Typical drive current<1mA.

SWITCHING CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all Recommended Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VDDA = +3.3V ±10%; GNDA = 0V. All voltages with respect to 0V.
- Logic Levels: Logic 0 = 0V, Logic 1 = VDDA.

Parameter		Symbol	Min	Typ	Max	Unit
Rise Times (Note 13)	DO Any Digital Output Except DO	t_{rise}	- -	- 50	1.0 -	µs ns
Fall Times (Note 13)	DO Any Digital Output Except DO	t_{fall}	- -	- 50	1.0 -	µs ns
Start-up						
Oscillator Start-up Time	XTAL = 4.096 MHz (Note 14)	t_{ost}	-	60	-	ms

Notes: 13. Specified using 10% and 90% points on waveform of interest. Output loaded with 50pF.

14. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Note 15)	VDDA	-0.3	-	+4.0	V
Input Current	(Notes 16 and 17)	I_{IN}	-	-	±10	mA
Input Current for Power Supplies		-	-	-	±50	-
Output Current	(Note 18)	I_{OUT}	-	-	100	mA
Power Dissipation	(Note 19)	P_D	-	-	500	mW
Input Voltage	(Note 20)	V_{IN}	-0.3	-	(VDDA) + 0.3	V
Junction-to-Ambient Thermal Impedance	2 Layer Board 4 Layer Board	θ_{JA}	- -	140 70	- -	°C/W °C/W
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes:
15. VDDA and GNDA must satisfy [(VDDA) – (GNDA)] ≤ + 4.0V.
16. Applies to all pins, including continuous overvoltage conditions at the analog input pins.
17. Transient current of up to 100mA will not cause SCR latch-up.
18. Applies to all pins, except VREF±.
19. Total power dissipation, including all input currents and output currents.
20. Applies to all pins.

WARNING:

Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

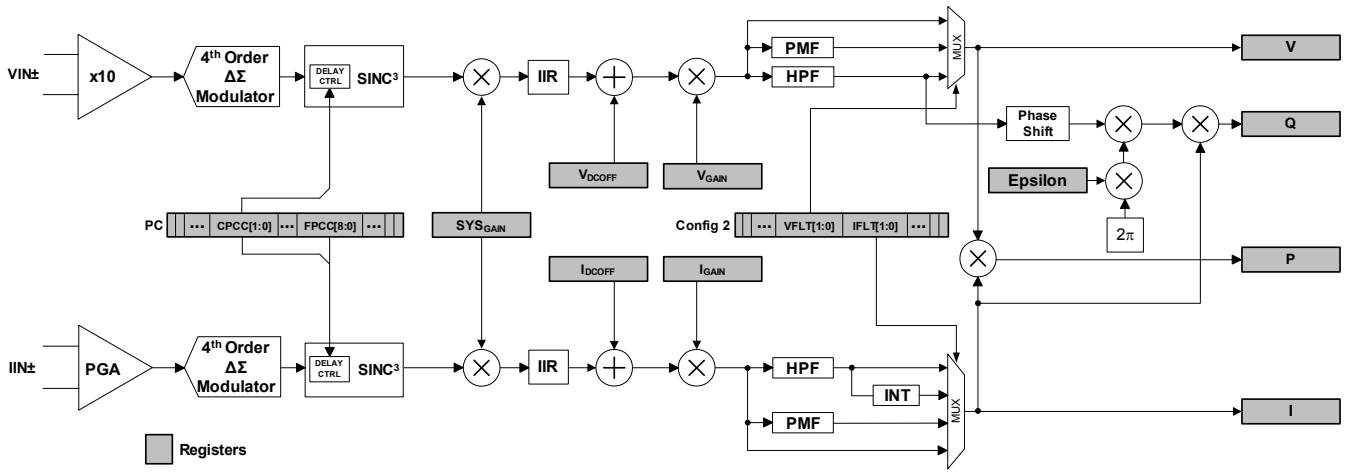


Figure 6. Signal Flow for V, I, P, and Q Measurements

4. SIGNAL FLOW DESCRIPTION

The signal flow for voltage, current measurement, and the other calculations is shown in Figure 6.

The signal flow consists of a current and a voltage channel. The current and voltage channels have differential input pins.

4.1 Analog-to-Digital Converters

Both input channels use fourth-order delta-sigma modulators to convert the analog inputs to single-bit digital data streams. The converters sample at a rate of MCLK/8. This high sampling provides a wide dynamic range and simplifies anti-alias filter design.

4.2 Decimation Filters

The single-bit modulator output data is widened to 24 bits and down sampled to MCLK/1024 with low-pass decimation filters. These decimation filters are third-order Sinc filters. The filter outputs pass through an IIR "anti-sinc" filter.

4.3 IIR Filter

The IIR filter is used to compensate for the amplitude roll-off of the decimation filters. The droop-correction filter flattens the magnitude response of the channel out to the Nyquist frequency, thus allowing for accurate measurements of up to 2kHz (MCLK = 4.096MHz). By default, the IIR filters are enabled. The IIR filters can be bypassed by setting the IIR_OFF bit in the *Config2* register.

4.4 Phase Compensation

Phase compensation changes the phase of voltage relative to current by adding a delay in the decimation filters. The amount of phase shift is set by the PC register bits CPCC[1:0] and FPCC[8:0] for the current channel. For the voltage channel, only bits CPCC[1:0] affect the delay.

Fine phase compensation control bits, FPCC[8:0], provide up to 1/OWR delay in the current channel. Coarse phase compensation control bits, CPCC[1:0], provide an additional 1/OWR delay in the current channel or up to 2/OWR delay in the voltage channel. Negative delay in the voltage channel can be implemented by setting longer delay in the current channel than the voltage channel. For a OWR of 4000Hz, the delay range is ±500µs, a phase shift of ±8.99° at 50Hz and ±10.79° at 60Hz. The step size is 0.008789° at 50Hz and 0.010547° at 60Hz. For more information about phase compensation, see section *7.2 Phase Compensation* on page 53.

4.5 DC Offset & Gain Correction

The system and CS5490 inherently have component tolerances, gain, and offset errors, which can be removed using the gain and offset registers. Each measurement channel has its own set of gain and offset registers. For every instantaneous voltage and current sample, the offset and gain values are used to correct DC offset and gain errors in the channel (see section *7. System Calibration* on page 52 for more details).

4.6 High-pass & Phase Matching Filters

Optional high-pass filters (HPF in Figure 6) remove any DC component from the selected signal paths. Each power calculation contains a current and voltage channel. If an HPF is enabled in only one channel, a phase-matching filter (PMF) should be applied to the other channel to match the phase response of the HPF. For AC power measurement, high-pass filters should be enabled on the voltage and current channels. For information about how to enable and disable the HPF or PMF on each channel, refer to *Config2* register descriptions in section *6.6 Register Descriptions* on page 32.

4.7 Digital Integrators

Optional digital integrators (INT in Figure 6) are implemented on the current channel to compensate for the 90° phase shift and 20dB/decade gain generated by the Rogowski coil current sensor. When a Rogowski coil is used as the current sensor, the integrator (INT) should be enabled on that current channel. For information about how to enable and disable the INT on the current channel, refer to *Config2* register descriptions in section *6.6 Register Descriptions* on page 32.

4.8 Low-rate Calculations

All the RMS and power results come from low-rate calculations by averaging the output word rate (OWR) instantaneous values over *N* samples, where *N* is the value stored in the *SampleCount* register. The low-rate interval or averaging period is *N* divided by OWR (4000Hz if MCLK = 4.096MHz). The CS5490 provides two averaging modes for low-rate calculations: Fixed Number of Sample Averaging mode and Line-cycle Synchronized Averaging mode. By default, the CS5490 averages with the Fixed Number of Samples Averaging mode. By setting the AVG_MODE bit in the *Config2* register, the CS5490 will use the Line-cycle Synchronized Averaging mode.

4.8.1 Fixed Number of Samples Averaging

N is the preset value in the *SampleCount* register and should not be set less than 100. By default, the *SampleCount* register is 4000. With MCLK = 4.096 MHz, the averaging period is fixed at N/4000 = 1 second, regardless of the line frequency.

4.8.2 Line-cycle Synchronized Averaging

When operating in Line-cycle Synchronized Averaging mode, and when line frequency measurement is enabled (see section *5.4 Line Frequency Measurement* on page 19), the CS5490 uses the voltage (V) channel zero crossings and measured line frequency to automatically adjust *N* such that the averaging period will be equal to the number of half line-cycles in the *CycleCount* register. For example, if the line frequency is 51Hz, and the *CycleCount* register is set to 100, *N* will be $4000 \times (100/2)/51 = 3921$ during continuous conversion. *N* is self-adjusted according to the line frequency, therefore the averaging period is always close to the whole number of half line-cycles, and the low-rate calculation results will minimize ripple and maximize resolution, especially when the line frequency varies. Before starting a low-rate conversion in the Line-cycle Synchronized Averaging mode, the

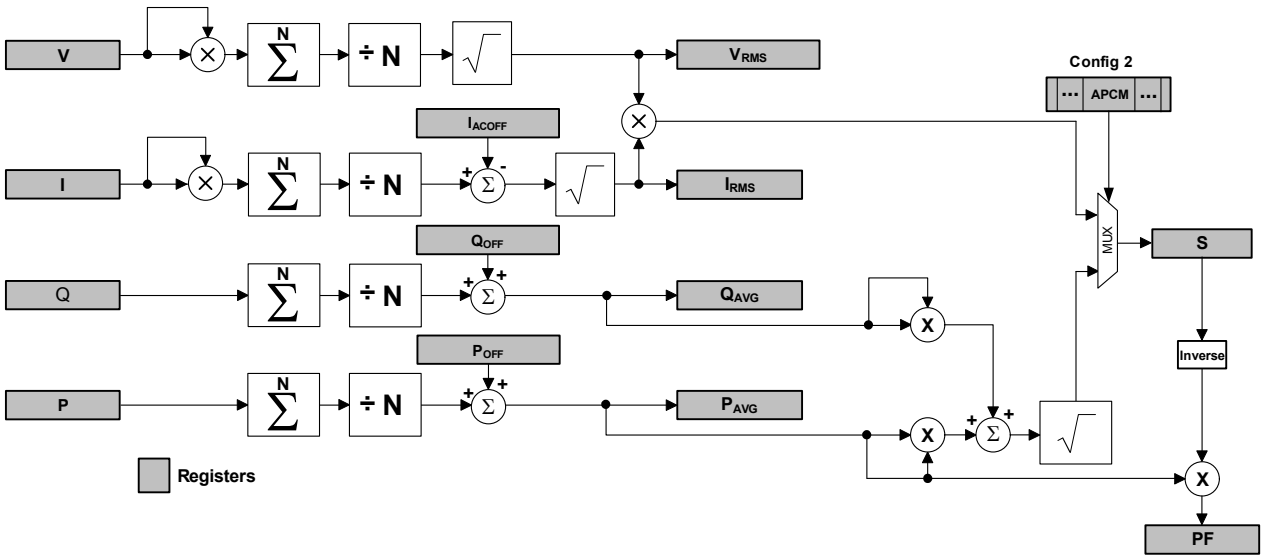


Figure 7. Low-rate Calculations

SampleCount register should not be changed from its default value of 4000, and bit AFC of the *Config2* register must be set. During continuous conversion, the host processor should not change the *SampleCount* register.

4.8.3 RMS Current & Voltage

The root mean square (*RMS* in Figure 7) calculations are performed on *N* instantaneous voltage and current samples using Equation 1:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} I_n^2}{N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} V_n^2}{N}} \qquad \text{[Eq.1]}$$

4.8.4 Active Power

The instantaneous voltage and current samples are multiplied to obtain the instantaneous power (*P*) (see Figure 6). The product is then averaged over *N* samples to compute active power (P_{AVG}).

4.8.5 Reactive Power

Instantaneous reactive power (*Q*) is the sample rate result obtained by multiplying instantaneous current (*I*) by instantaneous quadrature voltage (*Q*). These values are created by phase shifting instantaneous voltage (*V*) 90° using first-order integrators (see Figure 6). The gain of these integrators is inversely related to line frequency, so their gain is corrected by the *Epsilon* register, which is based on line frequency. Reactive power (Q_{AVG}) is generated by integrating the instantaneous quadrature power over *N* samples.

4.8.6 Apparent Power

By default, the CS5490 calculates the apparent power (*S*) as the product of RMS voltage and current. See Equation 2:

$$S = V_{RMS} \times I_{RMS} \qquad \text{[Eq.2]}$$

The CS5490 also provides an alternate apparent power calculation method. The alternate apparent power method uses real power (P_{AVG}) and reactive power (Q_{AVG}) to calculate apparent power. See Equation 3.

$$S = \sqrt{Q_{AVG}^2 + P_{AVG}^2} \qquad \text{[Eq.3]}$$

The APCM bit in the *Config2* register controls which method is used for apparent power calculation.

4.8.7 Peak Voltage & Current

Peak current (I_{PEAK}) and peak voltage (V_{PEAK}) are calculated over *N* samples and recorded in the corresponding channel peak register documented in the register map. This peak value is updated every *N* samples.

4.8.8 Power Factor

Power factor (*PF*) is active power divided by apparent power, as shown below. The sign of the power factor is determined by the active power. See Equation 4.

$$PF = \frac{P_{ACTIVE}}{S} \qquad \text{[Eq.4]}$$

4.9 Average Active Power Offset

The average active power offset register, P_{OFF}, can be used to offset erroneous power sources resident in the system not originating from the power line. Residual power offsets are usually caused by crosstalk into the current channel from the voltage channel, or from ripple on the meter's or chip's power supply, or from inductance from a nearby transformer.

These offsets can be either positive or negative, indicating crosstalk coupling either in phase or out of phase with the applied voltage input. The power offset register can compensate for either condition.

To use this feature, measure the average power at no load and take the measured result (from the P_{AVG} register), invert (negate) the value, and write it to the associated power offset register, P_{OFF}.

4.10 Average Reactive Power Offset

The average reactive power offset register, Q_{OFF}, can be used to offset erroneous power sources resident in the system not originating from the power line. Residual reactive power offsets are usually caused by crosstalk into the current channel from the voltage channel, or from ripple on the meter's or chip's power supply, or from inductance from a nearby transformer.

These offsets can be either positive or negative, depending on the phase angle between the crosstalk coupling and the applied voltage. The reactive power offset register can compensate for either condition. To use this feature, measure the average reactive power at no load. Take the measured result from the Q_{AVG} register, invert (negate) the value and write it to the reactive power offset register, Q_{OFF}.

5. FUNCTIONAL DESCRIPTION

5.1 Power-on Reset (POR)

The CS5490 has an internal power supply supervisor circuit that monitors the VDDA and VDDD power supplies and provides the master reset to the chip. If any of these voltages are in the reset range, the master reset is triggered.

Both the analog and the digital supply have their own POR circuit. During power-up, both supplies have to be above the rising threshold for the master reset to be de-asserted.

Each POR is divided into 2 blocks: rough and fine. Rough POR triggers the fine POR. Rough POR depends only on the supply voltage. The trip point for the fine POR is dependent on bandgap voltage for precise control.

The POR circuit also acts as a brownout detect. The fine POR detects supply drops and asserts the master reset.

The rough and fine PORs have hysteresis in their rise and fall thresholds which prevents the reset signal from chattering.

The following plot shows the POR outputs for each of the power supplies. The POR_Fine_VDDA and POR_Fine_VDDD signals are AND-ed to form the actual power-on reset signal to the digital circuity. The digital circuitry, in turn, holds the master reset signal for 130ms and then de-asserts the master reset.

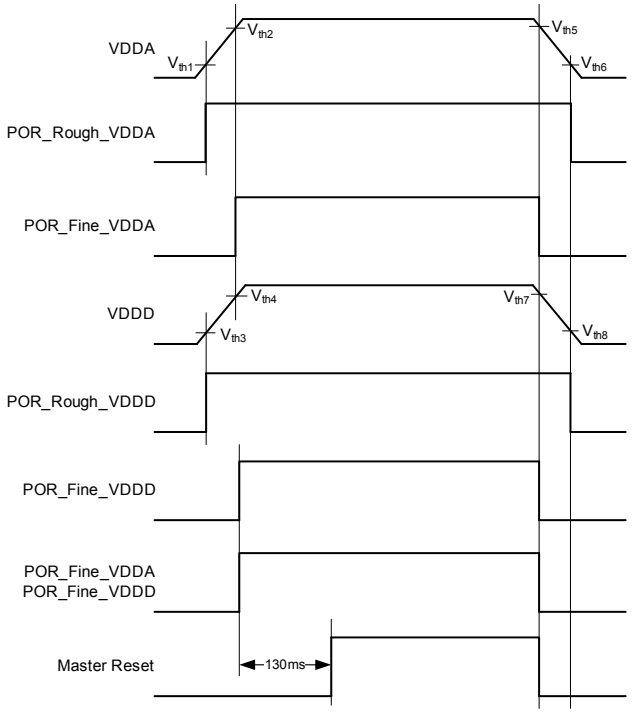


Figure 8. Power-on Reset Timing

Table 1. POR Thresholds

Typical POR Threshold		Rising	Falling
VDDA	Rough	V_{th1} = 2.34V	V_{th6} = 2.06V
	Fine	V_{th2} = 2.77V	V_{th5} = 2.59V
VDDD	Rough	V_{th3} = 1.20V	V_{th8} = 1.06V
	Fine	V_{th4} = 1.51V	V_{th7} = 1.42V

5.2 Power Saving Modes

Power Saving modes for CS5490 are accessed through the Host Instruction Commands (see *6.1 Host Commands* on page 24).

- Standby: Powers down all the ADCs, rough buffer, and the temperature sensor. Standby mode disables the system time calculations. Use the wake-up command to come out of standby mode.
- Wake-up: Clears the ADC power-down bits and starts the system time calculations.

After any of these commands are completed, the DRDY bit is set in the *Status0* register.

5.3 Zero-crossing Detection

Zero-crossing detection logic is implemented in CS5490. A low-pass filter can be enabled by setting ZX_LPF bit in register *Config2*. The low-pass filter has a cut-off frequency of 80Hz. It is used to eliminate any harmonics and to help the zero-crossing detection on the 50Hz or 60Hz fundamental component. The zero-crossing level registers are used to set the minimum threshold over which the channel peak has to exceed in order for the zero-crossing detection logic to function. There are two separate zero-crossing level registers: VZX_{LEVEL} is the threshold for the voltage channels, and IZX_{LEVEL} is the threshold for the current channels.

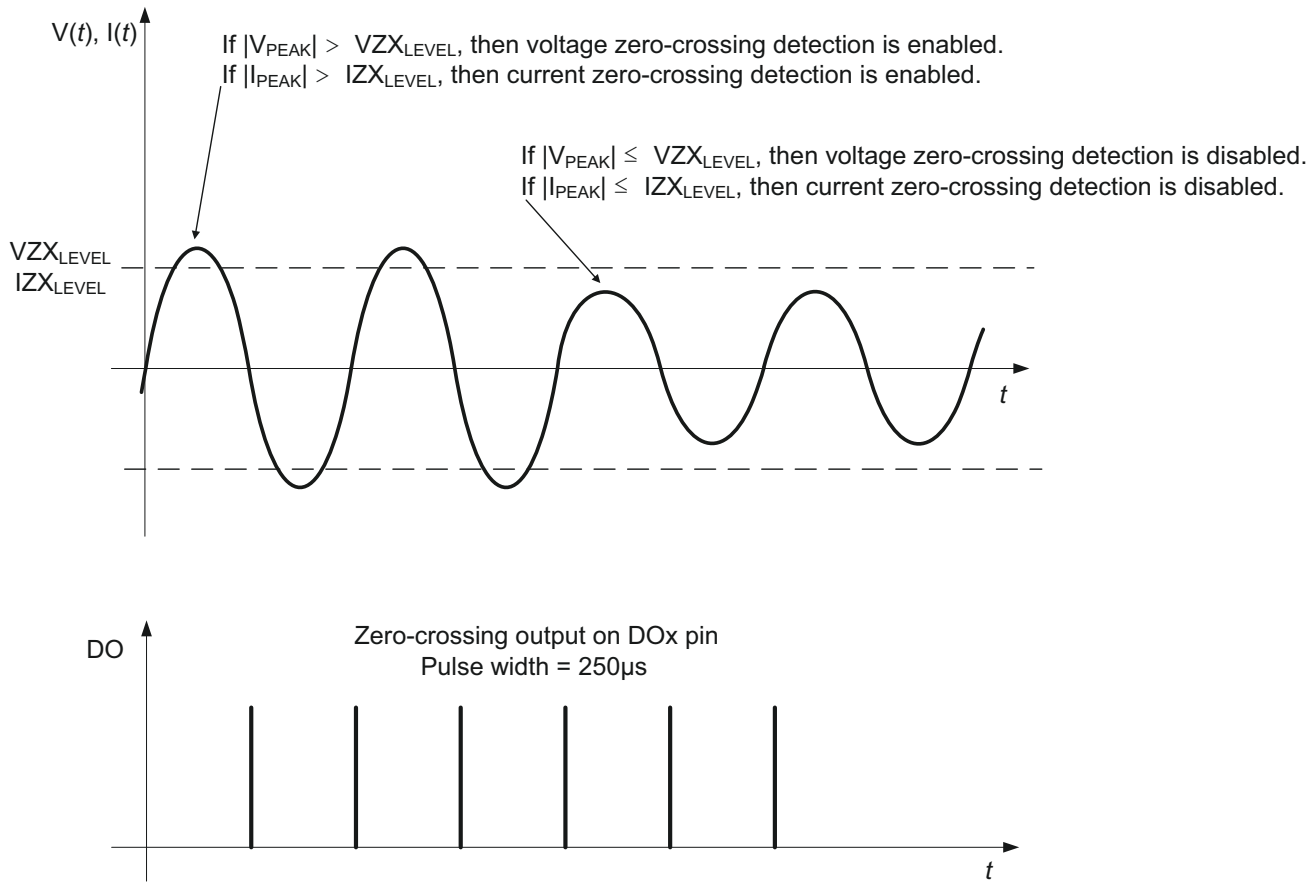


Figure 9. Zero-crossing Level and Zero-crossing Output on DO

5.4 Line Frequency Measurement

If the Automatic Frequency Calculation (AFC) bit in the *Config2* register is set, the line frequency measurement on the voltage channel will be enabled. The line frequency measurement is based on a number of voltage channel zero crossings. This number is 100 by default and configurable through the ZX_{NUM} register (see section *6.6.56* on page 51). The *Epsilon* register will be updated automatically with the line frequency information. The Frequency Update (FUP) bit in the *Status0* interrupt status register is set when the frequency calculation is completed. When the line frequency is 50Hz and the ZX_{NUM} register is 100, the *Epsilon* register is updated every one second with a resolution of less than 0.1%. A larger zero-crossing number in the ZX_{NUM} register will increase line frequency measurement resolution and period. Note that the CS5490 line frequency measurement function does not support the line frequency out of the range of 40Hz to 75Hz.

The *Epsilon* register is also used to set the gain of the 90° phase shift filter used in the quadrature power calculation. The value in the *Epsilon* register is the ratio of the line frequency to the output word rate (OWR). For 50Hz line frequency and 4000Hz OWR, *Epsilon* is 50/4000 (0.0125) (the default). For 60Hz line frequency, it is 60/4000 (0.015).

5.5 Energy Pulse Generation

The CS5490 provides an independent energy pulse generation (EPG) block in order to output active, reactive, and apparent energy pulses on the digital output pin (DO). The energy pulse frequency is proportional to the magnitude of the power. The energy pulse output is commonly used as the test output of a power meter. The host microcontroller can also use the energy pulses to easily accumulate the energy. Refer to Figure 10.

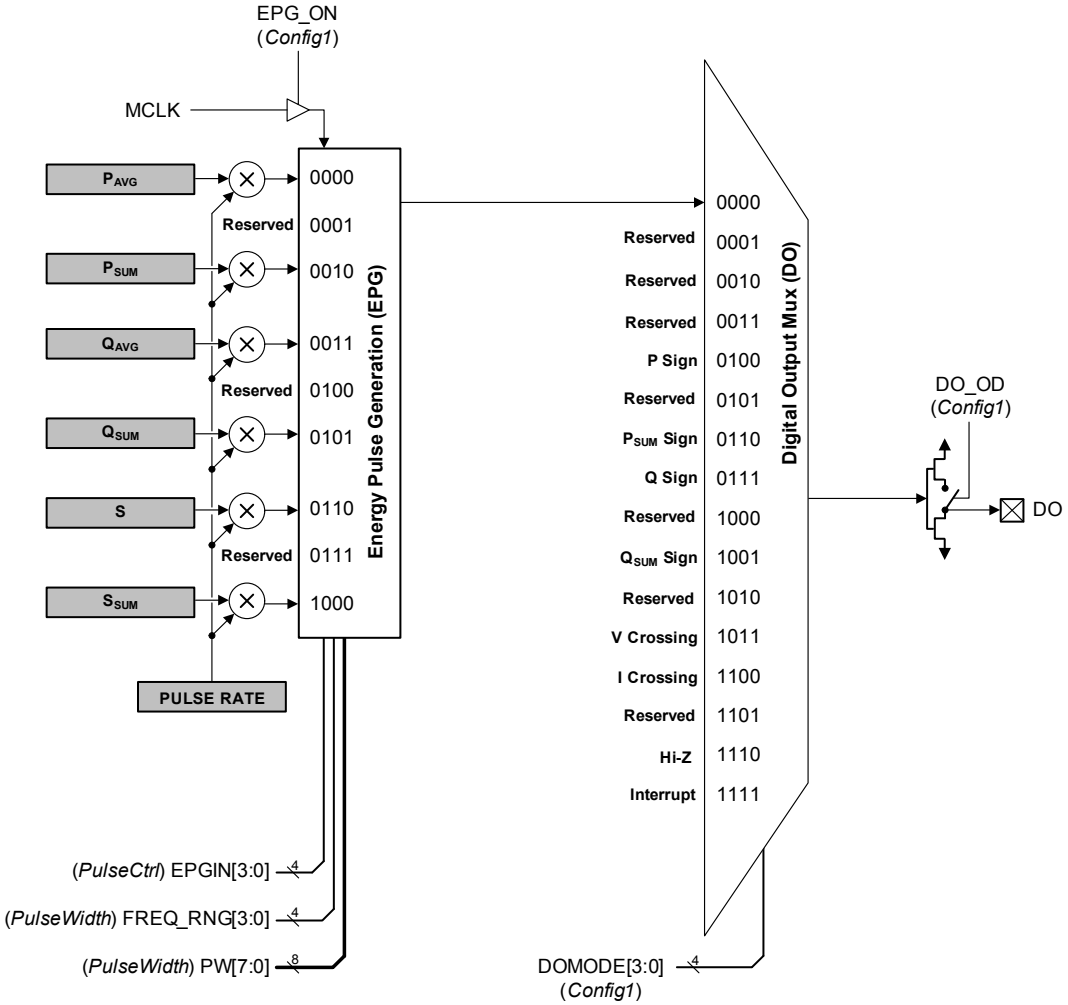


Figure 10. Energy Pulse Generation and Digital Output Control

After reset, the energy pulse generation block is disabled (DOMODE[3:0] = Hi-Z). To output a desired energy pulse to a DO pin, it is necessary to follow the steps below:

1. Write to register *PulseWidth* (page 0, address 8) to select the energy pulse width and pulse frequency range.
2. Write to register *PulseRate* (page 18, address 28) to select the energy pulse rate.
3. Write to register *PulseCtrl* (page 0, address 9) to select the input to the energy pulse generation block.
4. Write '1' to bit EPG_ON of register *Config1* (page 0, address 1) to enable the energy pulse generation block.
5. Wait at least 0.1s.
6. Write bits DOMODE[3:0] of register *Config1* to select DO to output pulses from the energy pulse generation block.
7. Send DSP instruction (0xD5) to begin continuous conversion.

5.5.1 Pulse Rate

Before configuring the *PulseRate* register, the full-scale pulse rate needs to be calculated, and the frequency range needs to be specified through FREQ_RNG[3:0] bits in the *PulseWidth* register. For example, if a meter has the meter constant of 1000imp/kWh, a maximum voltage (U_{MAX}) of 240V, and a maximum current (I_{MAX}) of 100A, the maximum pulse rate is:

$$[1000 \times (240 \times 100 / 1000)] / 3600 = 6.6667\,\text{Hz}.$$

Assume the meter is calibrated with U_{MAX} and I_{MAX}, and the *Scale* register contains the default value of 0.6. After gain calibration, the power register value will be 0.36, which represents 240 x 100 = 24kW or 6.6667Hz pulse output rate. The full-scale pulse rate is:

$$F_{out} = 6.6667 / 0.36 = 18.5185\,\text{Hz}.$$

Refer to section *6.6.6 Pulse Output Width (PulseWidth) – Page 0, Address 8* on page 36. The FREQ_RNG[3:0] bits should be set to b[0110].

The CS5490 pulse generation block behaves as follows:

- The pulse rate generated by full-scale (1.0 decimal) power register is

$$F_{OUT} = (PulseRate \times 2000)/2^{FREQ\_RNG}$$

- The *PulseRate* register value is

$$PulseRate = (F_{OUT} \times 2^{FREQ\_RNG})/2000$$
$$= (18.5186 \times 64)/2000$$
$$= 0.5925952$$
$$= 0x4BDA29$$

5.5.2 Pulse Width

The *PulseWidth* register defines the Active-low time of each energy pulse:

$$\text{Active-low} = 250\mu s + (PulseWidth/64000).$$

By default, the *PulseWidth* register value is 1, and the Active-low time of each energy pulse is 265.6µs. Note that the pulse width should never exceed the pulse period.

5.6 Voltage Sag, Voltage Swell, and Overcurrent Detection

Voltage sag detection is used to determine when the voltage falls below a predetermined level for a specified interval of time (duration). Voltage swell and overcurrent detection determine when the voltage or current rises above a predetermined level for the duration.

The duration is set by the value in the $VSag_{DUR}$, $VSwell_{DUR}$, and $IOver_{DUR}$ registers. Setting any of these to zero (default) disables the detect feature for the given channel. The value is in output word rate (OWR) samples. The predetermined level is set by the values in the $VSag_{LEVEL}$, $VSwell_{LEVEL}$, and $IOver_{LEVEL}$ registers.

For each enabled input channel, the measured value is rectified and compared to the associated level register. Over the duration window, the number of samples above and below the level are counted. If the number of samples below the level exceeds the number of samples above, a *Status0* register bit VSAG is set, indicating a sag condition. If the number of samples above the level exceeds the number of samples below, a *Status0* register bit VSWELL or IOVER is set, indicating a swell or overcurrent condition (see Figure 11).

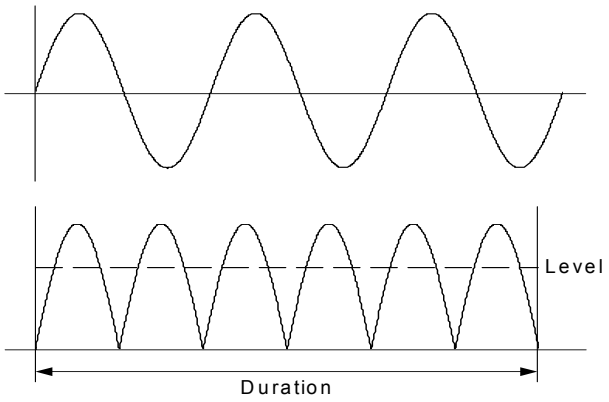


Figure 11. Sag, Swell, & Overcurrent Detect

5.7 Phase Sequence Detection

Polyphase meters using multiple CS5490 devices may be configured to sense the succession of voltage zero-crossings and determine which phase order is in service. The phase sequence detection within CS5490 involves counting the number of OWR samples from a starting point to the next voltage zero-crossing rising edge or falling for each phase. By comparing the count for each phase, the phase sequence can be easily determined: the smallest count is first, and the largest count is last.

The phase sequence detection and control (*PSDC*) register provides the count control, zero-crossing direction and count results. Writing '0' to bit DONE and '10110' to bits CODE[4:0] of the *PSDC* register followed by a falling edge on the RX pin will initiate the phase sequence detection circuit. The RX pin must be held low for a minimum of 500ns. When the device is in UART mode, it is recommended that a 0xFF command be written to all parts to start the phase sequence detection. Multiple CS5490 devices in a polyphase meter must receive the register writing and the RX falling edge at the same time so that all CS5490 devices starts to count simultaneously. Bit DIR of *PSDC* register specifies the direction of the next zero crossing at which the count stops. If bit DIR is '0', the count stops at the next negative-to-positive zero crossing. If bit DIR is '1', the count stops at the next positive-to-negative zero crossing. When the count stops, the DONE bit will be set by the CS5490, and then the count result of each phase may be read from bits PSCNT[6:0] of the PSDC register.

If the PSCNT[6:0] bits are equal to 0x00, 0x7F or greater than 0x64 (for 50Hz) or 0x50 (for 60Hz), then a measurement error has occurred, and the measurement results should be disregarded. This could happen when the voltage input signal amplitude is lower than the amplitude specified in the VZX_{LEVEL} register.

To determine the phase order, the PSCNT[6:0] bit counts from each CS5490 are sorted in ascending order. Figure 12 and Figure 13 illustrate how phase sequence detection is performed.

Phase sequences A, B, and C for the default rising edge transition are illustrated in Figure 12. The PSCNT[6:0] bits from the CS5490 on phase A will have the lowest count, followed by the PSCNT[6:0] bits from the CS5490 on phase B with the middle count, and the PSCNT[6:0] bits from the CS5490 on phase C with the highest count.

Phase sequences C, B, and A for rising edge transition are illustrated in Figure 13. The PSCNT[6:0] bits from the CS5490 on phase C will have the lowest count, followed by the PSCNT[6:0] bits from the CS5490 on phase B with the middle count, and the PSCNT[6:0] bits from the CS5490 on phase A with the highest count.

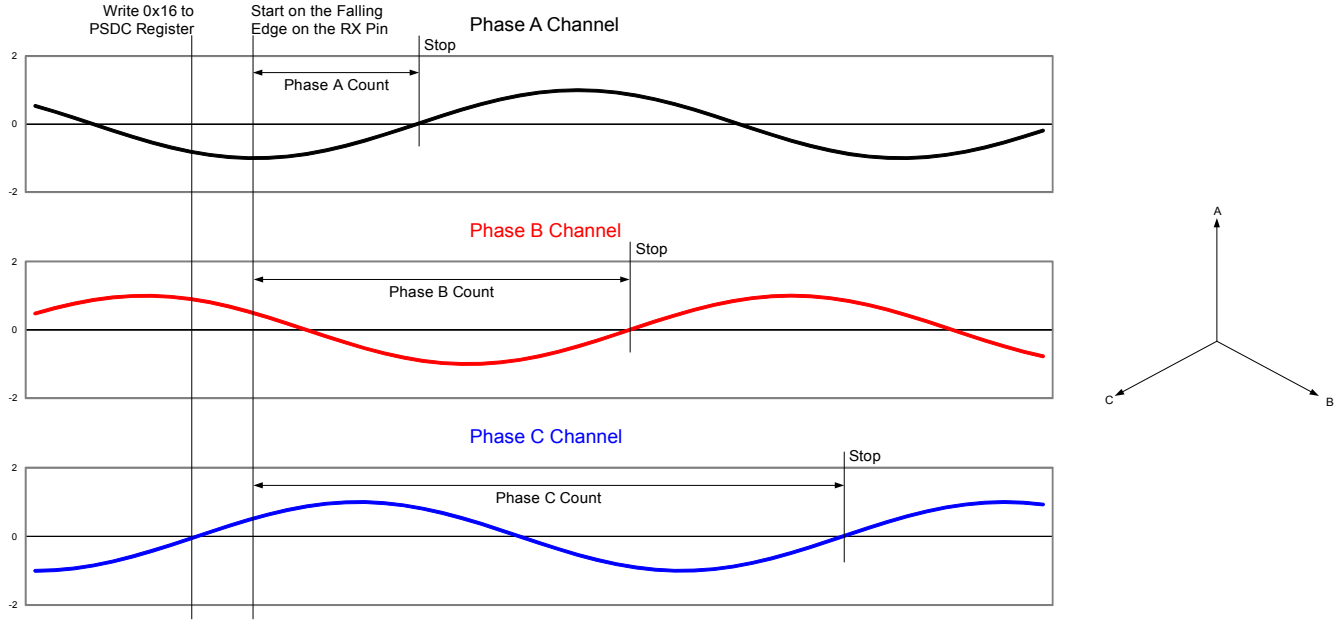


Figure 12. Phase Sequence A, B, C for Rising Edge Transition

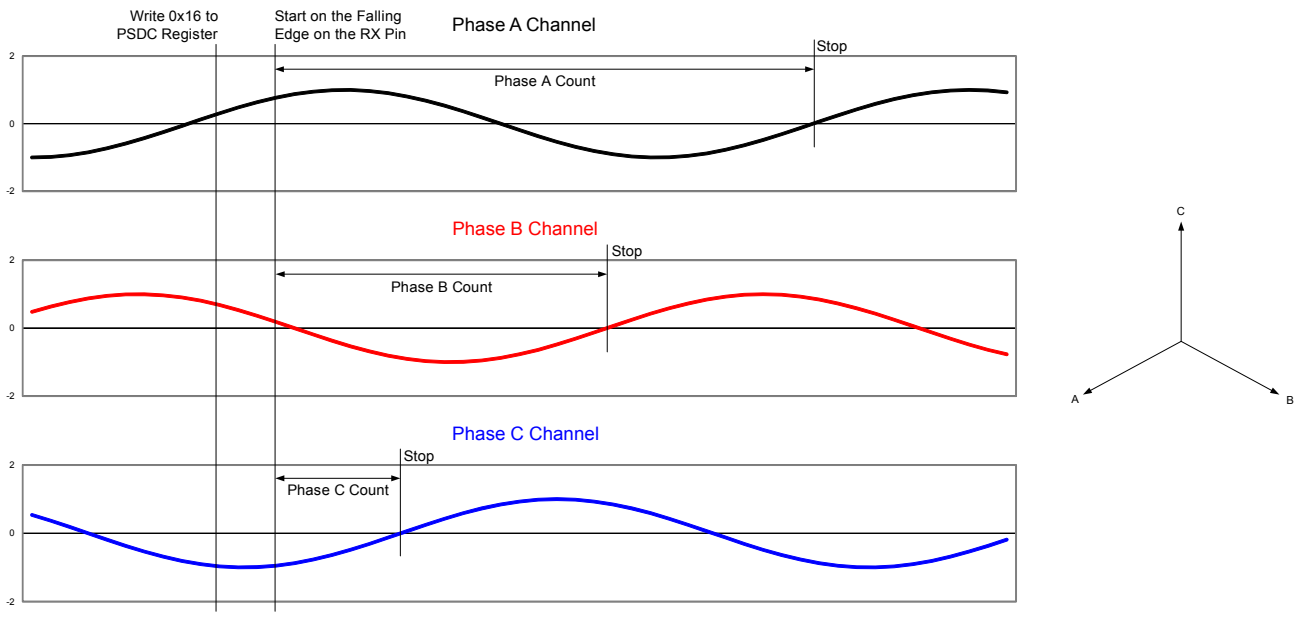


Figure 13. Phase Sequence C, B, A for Rising Edge Transition

5.8 Temperature Measurement

The CS5490 has an internal temperature sensor, which is designed to measure temperature and optionally compensate for temperature drift of the voltage reference. Temperature measurements are stored in the temperature register (*T*), which, by default, is configured to a range of ±128 °C.

The application program can change the scale and range of the temperature (*T*) register by changing the temperature gain (T_{GAIN}) register and temperature offset (T_{OFF}) register.

The temperature (*T*) register updates every 2240 output word rate (OWR) samples. The *Status0* register bit TUP indicates when *T* is updated.

5.9 Anti-creep

The anti-creep (no-load threshold) is used to determine if a no-load condition is detected. The $|P_{Sum}|$ and $|Q_{Sum}|$ are compared to the value in the no-load threshold ($Load_{Min}$) register. If both $|P_{Sum}|$ and $|Q_{Sum}|$ are less than this threshold, then P_{Sum} and Q_{Sum} are forced to zero. If S_{Sum} is less than the value in $Load_{Min}$ register, then S_{Sum} is forced to zero.

5.10 Register Protection

To prevent the critical configuration and calibration registers from unintended changes, the CS5490 provides two enhanced register protection mechanisms: write protection and automatic checksum calculation.

5.10.1 Write Protection

Setting the DSP_LCK[4:0] bits in the *RegLock* register to 0x16 enables the CS5490 DSP lockable registers to be write-protected from the calculation engine. Setting the DSP_LCK[4:0] bits to 0x09 disables the write-protection mode.

Setting the HOST_LCK[4:0] bits in the *RegLock* register to 0x16 enables the CS5490 HOST lockable registers to be write-protected from the serial interface. Setting the HOST_LCK[4:0] bits to 0x09 disables the write-protection mode.

For registers that are DSP lockable, HOST lockable, or both, refer to sections *6.2 Hardware Registers Summary (Page 0)* on page 26, *6.3 Software Registers Summary (Page 16)* on page 28, and *6.4 Software Registers Summary (Page 17)* on page 30.

5.10.2 Register Checksum

All the configuration and calibration registers are protected by checksum, if enabled. Refer to sections *6.2 Hardware Registers Summary (Page 0)* on page 26, *6.3 Software Registers Summary (Page 16)* on page 28, and *6.4 Software Registers Summary (Page 17)* on page 30. The checksum for all registers marked with an asterisk symbol (*) is computed at the rate of OWR. The checksum result is stored in the *RegChk* register. After the CS5490 has been fully configured and loaded with the calibrations, the host microcontroller should keep a copy of the checksum (*RegChk_Copy*) in its memory. In normal operation, the host microcontroller can read the *RegChk* register and compare it with the saved copy of the *RegChk* register. If the two values mismatch, a reload of configurations and calibrations into the CS5490 is necessary.

The automatic checksum computation can be disabled by setting the REG_CSUM_OFF bit in the *Config2* register.

6. HOST COMMANDS AND REGISTERS

6.1 Host Commands

The first byte sent to the CS5490 RX pin contains the host command. Four types of host commands are required to read and write registers and instruct the calculation engine. The two most significant bits (MSBs) of the host command defines the function to be performed. The following table depicts the types of commands.

Table 2. Command Format

Function	Binary Value	Note
Register Read	0 0 A_5 A_4 A_3 A_2 A_1 A_0	$A_{[5:0]}$ specifies the register address.
Register Write	0 1 A_5 A_4 A_3 A_2 A_1 A_0	
Page Select	1 0 P_5 P_4 P_3 P_2 P_1 P_0	$P_{[5:0]}$ specifies the page.
Instruction	1 1 C_5 C_4 C_3 C_2 C_1 C_0	$C_{[5:0]}$ specifies the instruction.

6.1.1 Memory Access Commands

The CS5490 memory has 12-bit addresses and is organized as P_5 P_4 P_3 P_2 P_1 P_0 A_5 A_4 A_3 A_2 A_1 A_0 in 64 pages of 64 addresses each. The higher 6 bits specify the page number. The lower 6 bits specify the address within the selected page.

6.1.1.1 Page Select

A page select command is designated by setting the two MSBs of the command to binary '10'. The page select command provides the CS5490 with the page number of the register to access. Register read and write commands access 1 of 64 registers within a specified page. Subsequent register reads and writes can be performed once the page has been selected.

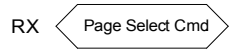


Figure 14. Byte Sequence for Page Select

6.1.1.2 Register Read

A register read is designated by setting the two MSBs of the command to binary '00'. The lower 6 bits of the read register command are the lower 6 bits of the 12-bit register address. After the register read command has been received, the CS5490 will send 3 bytes of register data onto the TX pin.

Figure 15. Byte Sequence for Register Read

6.1.1.3 Register Write

A register write command is designated by setting the two MSBs of the command to binary '01'. The lower 6 bits of the register write command are the lower 6 bits of the 12-bit register address. A register write command must be followed by 3 bytes of data.

Figure 16. Byte Sequence for Register Write

6.1.2 Instructions

An instruction command is designated by setting the two MSBs of the command to binary '11'. An instruction command will interrupt any process currently running and initiate a new process in the CS5490.

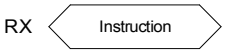


Figure 17. Byte Sequence for Instructions

These new processes include calibration, power control, and soft reset. The following table depicts the types of instructions. Note that when the CS5490 is in continuous conversion mode, an unexpected or invalid instruction command could cause the device to stop continuous conversion and enter an unexpected operation mode. The host processor should keep monitoring the CS5490 operation status and react accordingly.

Table 3. Instruction Format

Function	Binary Value	Note
Controls	0 **C_4 C_3 C_2 C_1 C_0** **0** 00001 - Software Reset **0** 00010 - Standby **0** 00011 - Wakeup **0** 10100 - Single Conv. **0** 10101 - Continuous Conv. **0** 11000 - Halt Conv.	$C_{[5]}$ specifies the instruction type: 0 = Controls 1 = Calibrations
Calibration	1 **C_4 C_3** C_2 C_1 C_0 **1** 00 $C_2C_1C_0$ DC Offset **1** 10 $C_2C_1C_0$ AC Offset* **1** 11 $C_2C_1C_0$ Gain ***AC offset calibration valid only for current channel.**	For calibration, $C_{[4:3]}$ specifies the type of calibration.
	1 C_4 C_3 **C_2 C_1 C_0** **1** C_4C_3 0 0 1 I **1** C_4C_3 0 1 0 V **1** C_4C_3 1 1 0 I & V	For calibration, $C_{[2:0]}$ specifies the channel(s).

6.1.3 Checksum

To improve the communication reliability on the serial interface, the CS5490 provides a checksum mechanism on transmitted and received signals. Checksum is disabled by default but can be enabled by setting the appropriate bit in the *SerialCtrl* register. When enabled, both host and CS5490 are expected to send one additional checksum byte after the normal command byte and applicable 3-byte register data have been transmitted.

The checksum is calculated by subtracting each transmit byte from 0xFF. Any overflow is truncated and the result wraps. The CS5490 executes the command only if the checksum transmitted by the host matches the checksum calculated locally. Otherwise, it sets a status bit (RX_CSUM_ERR in *Status0* register), ignores the command, and clears the serial interface in preparation for the next transmission.

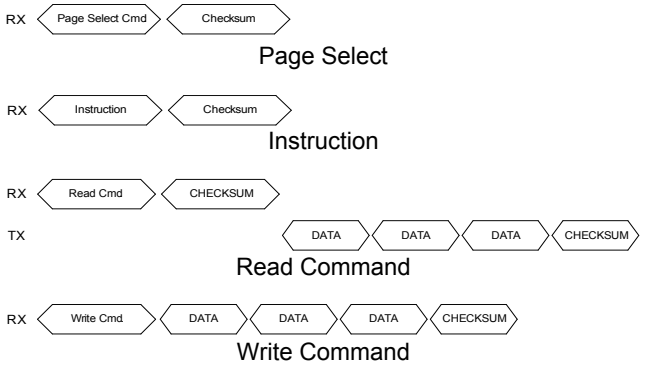


Figure 18. Byte Sequence for Checksum

6.1.4 Serial Time Out

In case a transaction from the host is not completed (for example, a data byte is missing in a register write), a time out circuit will reset the interface after 128 ms. This will require that each byte be sent from the host within 128 ms of the previous byte.

6.2 Hardware Registers Summary (Page 0)

Address[2]	RA[5:0]	Name	Description[1]	DSP[3]	HOST[3]	Default
0*	00 0000	Config0	Configuration 0	Y	Y	0x C0 2000
1*	00 0001	Config1	Configuration 1	Y	Y	0x 00 EEEE
2	00 0010	-	Reserved			-
3*	00 0011	Mask	Interrupt Mask	Y	Y	0x 00 0000
4	00 0100	-	Reserved	-		-
5*	00 0101	PC	Phase Compensation Control	Y	Y	0x 00 0000
6	00 0110	-	Reserved	-		-
7*	00 0111	SerialCtrl	UART Control	Y	Y	0x 02 004D
8*	00 1000	PulseWidth	Energy Pulse Width	Y	Y	0x 00 0001
9*	00 1001	PulseCtrl	Energy Pulse Control	Y	Y	0x 00 0000
10	00 1010	-	Reserved	-		-
11	00 1011	-	Reserved	-		-
12	00 1100	-	Reserved	-		-
13	00 1101	-	Reserved			-
14	00 1110	-	Reserved	-		-
15	00 1111	-	Reserved	-		-
16	01 0000	-	Reserved	-		-
17	01 0001	-	Reserved	-		-
18	01 0010	-	Reserved	-		-
19	01 0011	-	Reserved	-		-
20	01 0100	-	Reserved	-		-
21	01 0101	-	Reserved	-		-
22	01 0110	-	Reserved	-		-
23	01 0111	Status0	Interrupt Status	N	N	0x 80 0000
24	01 1000	Status1	Chip Status 1	N	N	0x 80 1800
25	01 1001	Status2	Chip Status 2	N	N	0x 00 0000
26	01 1010	-	Reserved	-		-
27	01 1011	-	Reserved	-		-
28	01 1100	-	Reserved	-		-
29	01 1101	-	Reserved	-		-
30	01 1110	-	Reserved	-		-
31	01 1111	-	Reserved	-		-
32	10 0000	-	Reserved	-		-
33	10 0001	-	Reserved	-		-
34*	10 0010	RegLock	Register Lock Control	N	N	0x 00 0000
35	10 0011	-	Reserved	-		-
36	10 0100	V_{PEAK}	Peak Voltage	N	Y	0x 00 0000
37	10 0101	I_{PEAK}	Peak Current	N	Y	0x 00 0000
38	10 0110	-	Reserved	-		-
39	10 0111	-	Reserved	-		-
40	10 1000	-	Reserved	-		-
41	10 1001	-	Reserved	-		-
42	10 1010	-	Reserved	-		-
43	10 1011	-	Reserved	-		-
44	10 1100	-	Reserved	-		-
45	10 1101	-	Reserved	-		-
46	10 1110	-	Reserved	-		-
47	10 1111	-	Reserved	-		-
48	11 0000	PSDC	Phase Sequence Detection & Control	N	Y	0x 00 0000
49	11 0001	-	Reserved	-		-
50	11 0010	-	Reserved	-		-
51	11 0011	-	Reserved	-		-
52	11 0100	-	Reserved	-		-

53	11 0101	-	Reserved	-		-
54	11 0110	-	Reserved	-		-
55	11 0111	ZX_{NUM}	Num. Zero Crosses used for Line Freq.	Y	Y	0x00 0064
56	11 1000	-	Reserved	-		-
57	11 1001	-	Reserved	-		-
58	11 1010	-	Reserved	-		-
59	11 1011	-	Reserved	-		-
60	11 1100	-	Reserved	-		-
61	11 1101	-	Reserved	-		-
62	11 1110	-	Reserved	-		-
63	11 1111	-	Reserved	-		-

Notes: (1) Warning: *Do not* write to unpublished or reserved register locations.

(2) * Registers with checksum protection.

(3) Registers that can be set to write protect from DSP and/or HOST.

6.3 Software Registers Summary (Page 16)

Address[2]	RA[5:0]	Name	Description[1]	DSP[3]	HOST[3]	Default
0*	00 0000	Config2	Configuration 2	Y	Y	0x 10 0200
1	00 0001	RegChk	Register Checksum	N	Y	0x 00 0000
2	00 0010	I	I Instantaneous Current	N	Y	0x 00 0000
3	00 0011	V	V Instantaneous Voltage	N	Y	0x 00 0000
4	00 0100	P	Instantaneous Power	N	Y	0x 00 0000
5	00 0101	P_{AVG}	Active Power	N	Y	0x 00 0000
6	00 0110	I_{RMS}	I RMS Current	N	Y	0x 00 0000
7	00 0111	V_{RMS}	V RMS Voltage	N	Y	0x 00 0000
8	00 1000	-	Reserved			-
9	00 1001	-	Reserved			-
10	00 1010	-	Reserved			-
11	00 1011	-	Reserved			-
12	00 1100	-	Reserved			-
13	00 1101	-	Reserved			-
14	00 1110	Q_{AVG}	Reactive Power	N	Y	0x 00 0000
15	00 1111	Q	Instantaneous Reactive Power	N	Y	0x 00 0000
16	01 0000	-	Reserved			-
17	01 0001	-	Reserved			-
18	01 0010	-	Reserved			-
19	01 0011	-	Reserved			-
20	01 0100	S	Apparent Power	N	Y	0x 00 0000
21	01 0101	PF	Power Factor	N	Y	0x 00 0000
22	01 0110	-	Reserved			-
23	01 0111	-	Reserved			-
24	01 1000	-	Reserved			-
25	01 1001	-	Reserved			-
26	01 1010	-	Reserved			-
27	01 1011	T	Temperature	N	Y	0x 00 0000
28	01 1100	-	Reserved			-
29	01 1101	P_{SUM}	Total Active Power	N	Y	0x 00 0000
30	01 1110	S_{SUM}	Total Apparent Power	N	Y	0x 00 0000
31	01 1111	Q_{SUM}	Total Reactive Power	N	Y	0x 00 0000
32*	10 0000	I_{DCOFF}	I DC Offset	Y	Y	0x 00 0000
33*	10 0001	I_{GAIN}	I Gain	Y	Y	0x 40 0000
34*	10 0010	V_{DCOFF}	V DC Offset	Y	Y	0x 00 0000
35*	10 0011	V_{GAIN}	V Gain	Y	Y	0x 40 0000
36*	10 0100	P_{OFF}	Instantaneous Power Offset			0x 00 0000
37*	10 0101	I_{ACOFF}	I AC Offset	Y	Y	0x 00 0000
38*	10 0110	-	Reserved			-
39*	10 0111	-	Reserved			-
40*	10 1000	-	Reserved			-
41*	10 1001	-	Reserved			-
42*	10 1010	-	Reserved			-
43*	10 1011	-	Reserved			-
44*	10 1100	-	Reserved			-
45*	10 1101	-	Reserved			-
46	10 1110	-	Reserved			-
47	10 1111	-	Reserved			-
48	11 0000	-	Reserved			-
49	11 0001	Epsilon	Ratio of Line to Sample Frequency	N	Y	0x 01 999A
50*	11 0010	-	Reserved			-
51**	11 0011	SampleCount	Sample Count	N	Y	0x 00 0FA0
52	11 0100	-	Reserved			-

53	11 0101	-	Reserved			-
54*	11 0110	T_{GAIN}	Temperature Gain	Y	Y	0x 06 B716
55*	11 0111	T_{OFF}	Temperature Offset	Y	Y	0x D5 3998
56*	11 1000	-	Reserved			-
57	11 1001	T_{SETTLE}	Filter Settling Time to Conv. Startup	Y	Y	0x 00 001E
58*	11 1010	$Load_{MIN}$	No Load Threshold	Y	Y	0x 00 0000
59*	11 1011	-	Reserved			-
60*	11 1100	SYS_{GAIN}	System Gain	N	Y	0x 50 0000
61	11 1101	Time	System Time (in samples)	N	Y	0x 00 0000
62	11 1110	-	Reserved			-
63	11 1111	-	Reserved			-

Notes:

(1) Warning: *Do not* write to unpublished or reserved register locations.

(2) * Registers with checksum protection.

** When setting the AVG_MODE bit (AVG_MODE = '1') in the *Config2* register, the device will use the Line-cycle Synchronized Averaging mode and the *CycleCount* register will be included in the checksum. Otherwise the *SampleCount* register will be included.

(3) Registers that can be set to write protect from DSP and/or HOST.

6.4 Software Registers Summary (Page 17)

Address[2]	RA[5:0]	Name	Description[1]	DSP[3]	HOST[3]	Default
0*	00 0000	$VSag_{DUR}$	V Sag Duration	Y	Y	0x 00 0000
1*	00 0001	$VSag_{Level}$	V Sag Level	Y	Y	0x 00 0000
2	00 0010	-	Reserved			-
3	00 0011	-	Reserved			-
4*	00 0100	$IOver_{DUR}$	I Overcurrent Duration	Y	Y	0x 00 0000
5*	00 0101	$IOver_{LEVEL}$	I Overcurrent Level	Y	Y	0x 7F FFFF
6	00 0110	-	Reserved			-
7	00 0111	-	Reserved			-
8*	00 1000	-	Reserved			-
9*	00 1001	-	Reserved			-
10	00 1010	-	Reserved			-
11	00 1011	-	Reserved			-
12*	00 1100	-	Reserved			-
13*	00 1101	-	Reserved			-
14	00 1110	-	Reserved			-
15	00 1111	-	Reserved			-
16	01 0000	-	Reserved			-
17	01 0001	-	Reserved			-
18	01 0010	-	Reserved			-
19	01 0011	-	Reserved			-
20	01 0100	-	Reserved			-
21	01 0101	-	Reserved			-
22	01 0110	-	Reserved			-
23	01 0111	-	Reserved			-
24	01 1000	-	Reserved			-
25	01 1001	-	Reserved			-
26	01 1010	-	Reserved			-
27	01 1011	-	Reserved			-
28	01 1100	-	Reserved			-
29	01 1101	-	Reserved			-
30	01 1110	-	Reserved			-
31	01 1111	-	Reserved			-

Notes: (1) Warning: *Do not* write to unpublished or reserved register locations.

(2) * Registers with checksum protection.

(3) Registers that can be set to write protect from DSP and/or HOST.

6.5 Software Registers Summary (Page 18)

Address[2]	RA[5:0]	Name	Description[1]	DSP[3]	HOST[3]	Default
24*	01 1000	IZX_{LEVEL}	I-channel Zero-crossing Threshold	Y	Y	0x 10 0000
25	01 1001	-	Reserved			-
26	01 1010	-	Reserved			-
27	01 1011	-	Reserved			-
28*	01 1100	PulseRate	Energy Pulse Rate	Y	Y	0x 80 0000
29	01 1101	-	Reserved			-
30	01 1110	-	Reserved			-
31	01 1111	-	Reserved			-
32	10 0000	-	Reserved			-
33	10 0001	-	Reserved			-
34	10 0010	-	Reserved			-
35	10 0011	-	Reserved			-
36	10 0100	-	Reserved			-
37	10 0101	-	Reserved			-
38	10 0110	-	Reserved			-
39	10 0111	-	Reserved			-
40	10 1000	-	Reserved			-
41	10 1001	-	Reserved			-
42	10 1010	-	Reserved			-
43*	10 1011	INT_{GAIN}	Rogowski Coil Integrator Gain	Y	Y	0x 14 3958
44	10 1100	-	Reserved			-
45	10 1101	-	Reserved			-
46*	10 1110	$VSwell_{DUR}$	V Swell Duration	Y	Y	0x 00 0000
47*	10 1111	$VSwell_{LEVEL}$	V Swell Level	Y	Y	0x 7F FFFF
48	11 0000	-	Reserved			-
49	11 0001	-	Reserved			-
50*	11 0010	-	Reserved			-
51*	11 0011	-	Reserved			-
52	11 0100	-	Reserved			-
53	11 0101	-	Reserved			-
54	11 0110	-	Reserved			-
55	11 0111	-	Reserved			-
56	11 1000	-	Reserved			-
57	11 1001	-	Reserved			-
58*	11 1010	VZX_{LEVEL}	V-channel Zero-crossing Threshold	Y	Y	0x 10 0000
59	11 1011	-	Reserved			-
60	11 1100	-	Reserved			-
61	11 1101	-	Reserved			-
62**	11 1110	CycleCount	Line Cycle Count	N	Y	0x 00 0064
63*	11 1111	Scale	Scale Value for I-channel Gain Calibration	Y	Y	0x 4C CCCC

Notes:

(1) Warning: *Do not* write to unpublished or reserved register locations.

(2) * Registers with checksum protection.

** When setting the AVG_MODE bit (AVG_MODE = '1') in the *Config2* register, the device will use the Line-cycle Synchronized Averaging mode and the *CycleCount* register will be included in the checksum. Otherwise the *SampleCount* register will be included.

(3) Registers that can be set to write protect from DSP and/or HOST.

6.6 Register Descriptions

21. “Default” = bit states after power-on or reset
22. DO NOT write a “1” to any unpublished register bit or to a bit published as “0”.
23. DO NOT write a “0” to any bit published as “1”.
24. DO NOT write to any unpublished register address.

6.6.1 Configuration 0 (Config0) – Page 0, Address 0

23	22	21	20	19	18	17	16
1	1	0	0	-	-	-	-
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
-	0	1	-	-	-	-	INT_POL
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	IPGA[1]	IPGA[0]	-	NO_OSC	0	0

Default = 0xC0 2000

[23:9] Reserved.

INT_POL Interrupt Polarity.
0 = Active low (Default)
1 = Active high

[7:6] Reserved.

IPGA[1:0] Select PGA gain for I channel.
00 = gain (Default)
10 = 50x gain

[3] Reserved.

NO_OSC Disable crystal oscillator (making XIN a logic-level input).
0 = Crystal oscillator enabled (Default)
1 = Crystal oscillator disabled

6.6.2 Configuration 1 (Config1) – Page 0, Address 1

23	22	21	20	19	18	17	16
0	0	0	EPG_ON	0	0	0	DO_OD
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
1	1	1	0	1	1	1	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	1	1	0	DOMODE[3]	DOMODE[2]	DOMODE[1]	DOMODE[0]

Default = 0x00 EEEE

[23:21] Reserved.

EPG_ON Enable EPG block.
0 = Disable energy pulse generation block (Default)
1 = Enable energy pulse generation block

[19:17] Reserved.

DO_OD Allow the DO pin to be an open-drain output.
0 = Normal output (Default)
1 = Open-drain output

[15:4] Reserved.

DOMODE[3:0] Output control for DO pin.
0000 = Energy pulse generation (EPG) block output
0001 = Reserved
0010 = Reserved
0011 = Reserved
0100 = P sign
0101 = Reserved
0110 = P_{SUM} sign
0111 = Q sign
1000 = Reserved
1001 = Q_{SUM} sign
1010 = Reserved
1011 = V zero-crossing
1100 = I zero-crossing
1101 = Reserved
1110 = Hi-Z, pin not driven (Default)
1111 = Interrupt

6.6.3 Configuration 2 (Config2) – Page 16, Address 0

23	22	21	20	19	18	17	16
-	POS	-	1	-	0	0	-
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
-	APCM	-	ZX_LPF	AVG_MODE	REG_CSUM_OFF	AFC	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	IFLT[1]	IFLT[0]	VFLT[1]	VFLT[0]	IIR_OFF

Default = 0x10 0200

[23] Reserved.

POS Positive energy only. Suppress negative values in P_{AVG}. If a negative value is calculated, a zero result will be stored.
0 = Positive and negative energy (Default)
1 = Positive energy only

[21:15] Reserved.

APCM Selects the apparent power calculation method.
0 = V_{RMS} x I_{RMS} (Default)
1 = SQRT(P_{AVG}^2 + Q_{AVG}^2)

[13] Reserved.

ZX_LPF Enable LPF in zero-cross detect.
0 = LPF disabled (Default)
1 = LPF enabled

AVG_MODE Select averaging mode for low-rate calculations.
0 = Use *SampleCount* (Default)
1 = Use *CycleCount*

REG_CSUM_OFF Disable checksum on critical registers.
0 = Enable checksum on critical registers (Default)
1 = Disable checksum on critical registers

AFC Enables automatic line frequency measurement which sets *Epsilon* every time a new line frequency measurement completes. *Epsilon* is used to control the gain of 90° phase shift integrator used in quadrature power calculations.
0 = Disable automatic line frequency measurement
1 = Enable automatic line frequency measurement (Default)

[8:5] Reserved.

IFLT[1:0] Filter enable for current channel.
00 = No filter (Default)
01 = High-pass filter (HPF) on current channel
10 = Phase-matching filter (PMF) on current channel
11 = Rogowski coil integrator (INT) on current channel

VFLT[1:0] Filter enable for voltage channel.
00 = No filter (Default)
01 = High-pass filter (HPF) on voltage channel
10 = Phase-matching filter (PMF) on voltage channel
11 = Reserved

IIR_OFF[0] Bypass IIR filter.
0 = Do not bypass IIR filter (Default)
1 = Bypass IIR filter

6.6.4 Phase Compensation (PC) – Page 0, Address 5

23	22	21	20	19	18	17	16
-	-	CPCC[1]	CPCC[0]	-	-	-	-
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
-	-	-	-	-	-	-	FPCC[8]
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FPCC[7]	FPCC[6]	FPCC[5]	FPCC[4]	FPCC[3]	FPCC[2]	FPCC[1]	FPCC[0]

Default = 0x00 0000

[23:22] Reserved.

CPCC[1:0] Coarse phase compensation control for I & V.
00 = No extra delay
01 = 1 OWR delay in current channel
10 = 1 OWR delay in voltage channel
11 = 2 OWR delay in voltage channel

[19:9] Reserved.

FPCC[8:0] Fine phase compensation control for I & V.
Sets a delay in current, relative to voltage.
Resolution: 0.008789° at 50Hz and 0.010547° at 60Hz (OWR = 4000)

6.6.5 UART Control (SerialCtrl) – Page 0, Address 7

23	22	21	20	19	18	17	16
-	-	-	-	-	RX_PU_OFF	RX_CSUM_OFF	-
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BR[15]	BR[14]	BR[13]	BR[12]	BR[11]	BR[10]	BR[9]	BR[8]
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BR[7]	BR[6]	BR[5]	BR[4]	BR[3]	BR[2]	BR[1]	BR[0]

Default = 0x02 004D

[23:19] Reserved.

RX_PU_OFF Disable the pull-up resistor on the RX input pin.
0 = Pull-up resistor enabled (Default)
1 = Pull-up resistor disabled

RX_CSUM_OFF Disable the checksum on serial port data.
0 = Enable checksum
1 = Disable checksum (Default)

[16] Reserved.

BR[15:0] Baud rate (serial bit rate).
BR[15:0] = Baud Rate x 524288 / MCLK

6.6.6 Pulse Output Width (PulseWidth) – Page 0, Address 8

23	22	21	20	19	18	17	16
-	-	-	-	FREQ_RNG[3]	FREQ_RNG[2]	FREQ_RNG[1]	FREQ_RNG[0]
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PW[15]	PW[14]	PW[13]	PW[12]	PW[11]	PW[10]	PW[9]	PW[8]
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PW[7]	PW[6]	PW[5]	PW[4]	PW[3]	PW[2]	PW[1]	PW[0]

Default = 0x00 0001 (265.6 µs at OWR = 4 kHz)

PulseWidth sets the energy pulse frequency range and the duration of energy pulses.

The actual pulse duration is 250 µs plus the contents of *PulseWidth* divided by 64,000. *PulseWidth* is an integer in the range of 1 to 65,535.

[23:20] Reserved.

FREQ_RNG[19:16] Energy pulse (*PulseRate*) frequency range for 0.1% resolution.
- 0000 = Freq. range: 2 kHz – 0.238 Hz (Default)
- 0001 = Freq. range: 1 kHz – 0.1192 Hz
- 0010 = Freq. range: 500 Hz – 0.0596 Hz
- 0011 = Freq. range: 250 Hz – 0.0298 Hz
- 0100 = Freq. range: 125 Hz – 0.0149 Hz
- 0101 = Freq. range: 62.5 Hz – 0.00745 Hz
- 0110 = Freq. range: 31.25 Hz – 0.003725 Hz
- 0111 = Freq. range: 15.625 Hz – 0.0018626 Hz
- 1000 = Freq. range: 7.8125 Hz – 0.000931323 Hz
- 1001 = Freq. range: 3.90625 Hz – 0.000465661 Hz
- 1010 = Reserved
- ...
- 1111 = Reserved

PW[15:0] Energy Pulse Width.

6.6.7 Pulse Output Rate (PulseRate) – Page 18, Address 28

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default= 0x80 0000

PulseRate sets the full-scale frequency for the energy pulse output.

For a 4 kHz OWR rate, the maximum pulse rate is 2 kHz. It is a two's complement value in the range of $-1 \leq \text{value} < 1$, with the binary point to the left of the MSB.

Refer to section *5.5 Energy Pulse Generation* on page 19 for more information.

6.6.8 Pulse Output Control (PulseCtrl) – Page 0, Address 9

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	EPGIN[3]	EPGIN[2]	EPGIN[1]	EPGIN[0]

Default = 0x00 0000

This register controls the input to the energy pulse generation (EPG) block.

[23:4] Reserved.

EPGIN[3:0] Selects the input to the energy pulse generation (EPG) block.
0000 = P_{AVG} (Default)
0001 = Reserved
0010 = P_{SUM}
0011 = Q_{AVG}
0100 = Reserved
0101 = Q_{SUM}
0110 = S
0111 = Reserved
1000 = S_{SUM}
1001 = Unused
...
1111 = Unused

6.6.9 Register Lock Control (RegLock) – Page 0, Address 34

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
-	-	-	DSP_LCK[4]	DSP_LCK[3]	DSP_LCK[2]	DSP_LCK[1]	DSP_LCK[0]
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	HOST_LCK[4]	HOST_LCK[3]	HOST_LCK[2]	HOST_LCK[1]	HOST_LCK[0]

Default = 0x00 0000

[23:13] Reserved.

DSP_LCK[12:8] DSP_LCK[4:0] = 0x16 sets the DSP lockable registers to be write protected from the CS5490 internal calculation engine. Writing 0x09 unlocks the registers.

[7:5] Reserved.

HOST_LCK[4:0] HOST_LCK[4:0] = 0x16 sets all the registers except *RegLock*, *Status0*, *Status1*, and *Status2* to be write protected from the serial interface. Writing 0x09 unlocks the registers.

6.6.10 Phase Sequence Detection and Control (PSDC) – Page 0, Address 48

23	22	21	20	19	18	17	16
DONE	PSCNT[6]	PSCNT[5]	PSCNT[4]	PSCNT[3]	PSCNT[2]	PSCNT[1]	PSCNT[0]
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
-	-	-	-	-	-	-	-
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	DIR	CODE[4]	CODE[3]	CODE[2]	CODE[1]	CODE[0]

Default = 0x00 0000

DONE — Indicates valid count values reside in PSCNT[6:0].
0 = Invalid values in PSCNT[6:0]. (Default)
1 = Valid values in PSCNT[6:0].

PSCNT[6:0] — Registers the number of OWR samples from the start time to the time when the next zero crossing is detected.

[15:6] — Reserved.

DIR — Set the zero-crossing edge direction which will stop PSCNT count.
0 = Stop count at negative to positive zero-crossing - Rising Edge. (Default)
1 = Stop count at positive to negative zero-crossing - Falling Edge.

CODE[4:0] — Write 10110 to this location to enable the phase sequence detection.

6.6.11 Checksum of Critical Registers (RegChk) – Page 16, Address 1

MSB															**LSB**
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Default = 0x00 0000

This register contains the checksum of critical registers.

6.6.12 Interrupt Status (Status0) – Page 0, Address 23

23	22	21	20	19	18	17	16
DRDY	CRDY	WOF	-	-	MIPS	-	VSWELL
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
-	POR	-	IOR	-	VOR	-	IOC
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	VSAG	TUP	FUP	IC	RX_CSUM_ERR	-	RX_TO

Default = 0x 00 0000

The *Status0* register indicates a variety of conditions within the chip.

Writing a one to a *Status0* register bit will clear that bit. Writing a zero to any bit has no effect.

DRDY — Data Ready. During conversion, this bit indicates that low-rate results have been updated. It indicates completion of other host instruction and the reset sequence.

CRDY — Conversion Ready. Indicates that sample rate (output word rate) results have been updated.

WOF — Watchdog timer overflow.

[20:19] — Reserved.

MIPS — MIPS overflow.
Sets when the calculation engine has not completed processing a sample before the next one arrives.

[17] — Reserved.

VSWELL — Voltage channel swell event detected.

[15] — Reserved.

POR — Power out of range. Sets when the measured power would cause the *P* register to overflow.

[13] — Reserved.

IOR — Current out of range. Set when the measured current would cause the *I* register to overflow.

[11] — Reserved.

VOR — Voltage out of range. Set when the measured voltage would cause the *V* register to overflow.

[7] — Reserved.

IOC — I Overcurrent.

[9] — Reserved.

VSAG — Voltage channel sag event detected.

TUP — Temperature updated. Indicates when the Temperature register (*T*) has been updated.

FUP — Frequency updated. Indicates the *Epsilon* register has been updated.

IC — Invalid command has been received.

RX_CSUM_ERR — Received data checksum error. Sets to one automatically if checksum error is detected on serial port received data.

RX_TO — SDI/RX time out. Sets to one automatically when SDI/RX time out occurs.

6.6.13 Interrupt Mask (Mask) – Page 0, Address 3

23	22	21	20	19	18	17	16
DRDY	CRDY	WOF	-	-	MIPS	0	VSWELL
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	POR	0	IOR	0	VOR	0	IOC
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	VSAG	TUP	FUP	IC	RX_CSUM_ERR	-	RX_TO

Default = 0x00 0000

The *Mask* register is used to control the activation of the $\overline{\text{INT}}$ pin. Writing a '1' to a *Mask* register bit will allow the corresponding *Status0* register bit to activate the $\overline{\text{INT}}$ pin when set.

[23:0] Enable/disable (mask) interrupts.
0 = Interrupt disabled (Default)
1 = Interrupt enabled

6.6.14 Chip Status 1 (Status1) – Page 0, Address 24

23	22	21	20	19	18	17	16
		-	-	-	-	-	-
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LCOM[7]	LCOM[6]	LCOM[5]	LCOM[4]	LCOM[3]	LCOM[2]	LCOM[1]	LCOM[0]
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	-	TOD	VOD	-	IOD

Default = 0x00 0000

This register indicates a variety of conditions within the chip.

[23:16] Reserved.

LCOM[15:8] Indicates the value of the last serial command executed.

[7:4] Reserved.

TOD Modulator oscillation has been detected in the temperature ADC.

VOD Modulator oscillation has been detected in the voltage ADC.

[1] Reserved.

IOD Modulator oscillation has been detected in the current ADC.

6.6.15 Chip Status 2 (Status2) – Page 0, Address 25

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
-	-	-	-	-	-	-	-
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	QSUM_SIGN	-	Q_SIGN	PSUM_SIGN	-	P_SIGN

Default = 0x00 0000

This register indicates a variety of conditions within the chip.

[23:6] Reserved.

QSUM_SIGN Indicates the sign of the value contained in Q_{SUM}.
0 = positive value
1 = negative value

[4] Reserved.

Q_SIGN Indicates the sign of the value contained in Q_{AVG}.
0 = positive value
1 = negative value

PSUM_SIGN Indicates the sign of the value contained in P_{SUM}.
0 = positive value
1 = negative value

[1] Reserved.

P_SIGN Indicates the sign of the value contained in P_{AVG}.
0 = positive value
1 = negative value

6.6.16 Line to Sample Frequency Ratio (Epsilon) – Page 16, Address 49

MSB															**LSB**
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x01 999A (0.0125 or 50Hz/4.0kHz)

Epsilon is the ratio of the input line frequency to the output word rate (OWR).

It can either be written by the application program or calculated automatically from the line frequency (from the voltage channel input) using the AFC bit in the *Config2* register. It is a two's complement value in the range of $-1.0 \leq \text{value} < 1.0$, with the binary point to the right of the MSB. Negative values are not used.

6.6.17 No Load Threshold ($Load_{MIN}$) – Page 16, Address 58

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

$Load_{MIN}$ is used to set the no-load threshold for the anti-creep function.

When the magnitudes of P_{SUM} and Q_{SUM} are less than $Load_{MIN}$, P_{SUM} and Q_{SUM} are forced to zero. When the magnitude of S_{SUM} is less than $Load_{MIN}$, S_{SUM} is forced to zero.

$Load_{MIN}$ is a two's complement value in the range of $-1.0 \leq \text{value} < 1.0$, with the binary point to the right of the MSB. Negative values are not used.

6.6.18 Sample Count (SampleCount) – Page 16, Address 51

MSB															LSB
0	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x00 0FA0 (4000)

Determines the number of output word rate (OWR) samples to use in calculating low-rate results. *SampleCount* (*N*) is an integer in the range of 100 to 8,388,607. Values less than 100 should not be used.

6.6.19 Cycle Count (CycleCount) – Page 18, Address 62

MSB															LSB
0	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x00 0064 (100)

Determines the number of half-line cycles to use in calculating low-rate results when the CS5490 is in Line-cycle Synchronized Averaging mode.

CycleCount is an integer in the range of 1 to 8,388,607. Zero should not be used.

6.6.20 Filter Settling Time for Conversion Startup (T_{SETTLE}) – Page 16, Address 57

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x00 001E (30)

Sets the number of output word rate (OWR) samples that will be used to allow filters to settle at the beginning of Conversion and Calibration commands.

This is an integer in the range of 0 to 16,777,215 samples.

6.6.21 System Gain (Sys_{GAIN}) – Page 16, Address 60

MSB															LSB
$-(2^1)$	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default = 0x50 0000 (1.25)

System Gain (Sys_{GAIN}) is applied to all channels.

By default, Sys_{GAIN} = 1.25, but can be finely adjusted to compensate for voltage reference error. It is a two's complement value in the range of -2.0 ≤ value < 2.0, with the binary point to the right of the second MSB. Values should be kept within 5% of 1.25.

6.6.22 Rogowski Coil Integrator Gain (Int_{GAIN}) – Page 18, Address 43

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x14 3958

Gain for the Rogowski coil integrator. This must be programmed accordingly for 50 Hz and 60 Hz (0.158 for 50 Hz, 0.1875 for 60 Hz).

This is a two's complement value in the range of -1.0 ≤ value ≤ 1.0, with the binary point to the right of the MSB. Negative values are not used.

6.6.23 System Time (Time) – Page 16, Address 61

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x00 0000

System Time (*Time*) is measured in output word rate (OWR) samples.

This is an unsigned integer in the range of 0 to 16,777,215 samples. At OWR = 4.0 kHz, OWR will overflow every 1 hour, 9 minutes, 54 seconds. *Time* can be used by the application to manage real-time events.

6.6.24 Voltage Sag Duration ($VSag_{DUR}$) – Page 17, Address 0

MSB															LSB
0	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x00 0000

Voltage sag duration, $VSag_{DUR}$, determines the count of output word rate (OWR) samples utilized to determine a sag event.

These are integers in the range of 0 to 8,388,607 samples. A value of zero disables the feature.

6.6.25 Voltage Sag Level ($VSag_{LEVEL}$) – Page 17, Address 1

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

Voltage sag level, $VSag_{LEVEL}$, establishes an input level below which a sag event is triggered.

This is a two's complement value in the range of $-1.0 \leq \text{value} < 1.0$, with the binary point to the right of the MSB. Negative values are not used.

6.6.26 Current Overcurrent Duration ($IOver_{DUR}$) – Page 17, Address 4

MSB															LSB
0	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x00 0000

Overcurrent duration, $IOver_{DUR}$, determines the count of output word rate (OWR) samples utilized to determine an overcurrent event.

These are integers in the range of 0 to 8,388,607 samples. A value of zero disables the feature.

6.6.27 Current Overcurrent Level ($IOver_{LEVEL}$) – Page 17, Address 5

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x7F FFFF

Overcurrent level, $IOver_{LEVEL}$, establishes an input level above which an overcurrent event is triggered.

This is a two's complement value in the range of $-1.0 \leq \text{value} < 1.0$, with the binary point to the right of the MSB. Negative values are not used.

6.6.28 Voltage Swell Duration ($VSwell_{DUR}$) – Page 18, Address 46

MSB															LSB
0	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x00 0000

Voltage swell duration, $VSwell_{DUR}$, determines the count of output word rate (OWR) samples used to determine a swell event.

These are integers in the range of 0 to 8,388,607 samples. A value of zero disables the feature.

6.6.29 Voltage Swell Level ($VSwell_{LEVEL}$) – Page 18, Address 47

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x7F FFFF

Voltage swell level, $VSwell_{LEVEL}$, establishes an input level above which a swell event is triggered.

This is a two's complement value in the range of $-1.0 \leq value < 1.0$, with the binary point to the right of the MSB. Negative values are not used.

6.6.30 Instantaneous Current (I) – Page 16, Address 2

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

I contains instantaneous current measurements for current channel.

This is a two's complement value in the range of $-1.0 \leq value < 1.0$, with the binary point to the right of the MSB.

6.6.31 Instantaneous Voltage (V) – Page 16, Address 3

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

V contains instantaneous voltage measurements for voltage channel.

This is a two's complement value in the range of $-1.0 \leq value < 1.0$, with the binary point to the right of the MSB.

6.6.32 Instantaneous Active Power (P) – Page 16, Address 4

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

P contains instantaneous power measurements for current and voltage channels.

Values in registers *I* and *V* are multiplied to generate this value. This is a two's complement value in the range of $-1.0 \leq value < 1.0$, with the binary point to the right of the MSB.

6.6.33 Active Power (P_{AVG}) – Page 16, Address 5

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

Instantaneous power is averaged over each low-rate interval (*SampleCount* samples) and then added with power offset (P_{OFF}) to compute active power (P_{AVG}).

This is a two's complement value in the range of $-1.0 \leq \text{value} < 1.0$, with the binary point to the right of the MSB.

6.6.34 RMS Current (I_{RMS}) – Page 16, Address 6

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Default = 0x00 0000

I_{RMS} contains the root mean square (RMS) values of *I*, calculated during each low-rate interval.

This is an unsigned value in the range of $0 \leq \text{value} < 1.0$, with the binary point to the left of the MSB.

6.6.35 RMS Voltage (V_{RMS}) – Page 16, Address 7

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Default = 0x00 0000

V_{RMS} contains the root mean square (RMS) value of *V*, calculated during each low-rate interval.

This is an unsigned value in the range of $0 \leq \text{value} < 1.0$, with the binary point to the left of the MSB.

6.6.36 Reactive Power (Q_{Avg}) – Page 16, Address 14

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

Reactive power (Q_{AVG}) is *Q* averaged over each low-rate interval (*SampleCount* samples) and corrected by Q_{OFF}.

This is a two's complement value in the range of $-1.0 \leq \text{value} < 1.0$, with the binary point to the right of the MSB.

6.6.37 Instantaneous Quadrature Power (Q) – Page 16, Address 15

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

Instantaneous quadrature power, *Q*, the product of *V* shifted 90° and *I*.

This is a two's complement value in the range of -1.0 ≤ value < 1.0, with the binary point to the right of the MSB.

6.6.38 Peak Current (I_{PEAK}) – Page 0, Address 37

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

Peak current (I_{PEAK}) contains the value of the instantaneous current 1 sample with the greatest magnitude detected during the last low-rate interval.

This is a two's complement value in the range of -1.0 ≤ value < 1.0, with the binary point to the right of the MSB.

6.6.39 Peak Voltage (V_{PEAK}) – Page 0, Address 36

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

Peak voltage (V_{PEAK}) contains the value of the instantaneous voltage sample with the greatest magnitude detected during the last low-rate interval.

This is a two's complement value in the range of -1.0 ≤ value < 1.0, with the binary point to the right of the MSB.

6.6.40 Apparent Power (S) – Page 16, Address 20

MSB															LSB
0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

Apparent power 1 (*S*) is the product of V_{RMS} and I_{RMS} or SQRT(P_{AVG}^2 + Q_{AVG}^2).

This is an unsigned value in the range of 0 ≤ value < 1.0, with the binary point to the right of the MSB.

6.6.41 Power Factor (PF) – Page 16, Address 21

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

Power factor (*PF*) is calculated by dividing active power (P_{AVG}) by apparent power (*S*).

The sign is determined by the active power (P_{AVG}) sign.

This is a two's complement value in the range of -1.0 ≤ value < 1.0, with the binary point to the right of the MSB.

6.6.42 Temperature (T) – Page 16, Address 27

MSB															LSB
$-(2^7)$	2^6	2^5	2^4	2^3	2^2	2^1	2^0	.....	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Default = 0

T contains results from the on-chip temperature measurement.

By default, *T* uses the Celsius scale and is a two's complement value in the range of -128.0 ≤ value < 128.0 (°C), with the binary point to the right of bit 16.

T can be rescaled by the application using the T_{GAIN} and T_{OFF} registers.

6.6.43 Total Active Power (P_{SUM}) – Page 16, Address 29

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0

$P_{SUM} = P_{AVG}$

This is a two's complement value in the range of -1.0 ≤ value < 1.0, with the binary point to the right of the MSB.

6.6.44 Total Apparent Power (S_{SUM}) – Page 16, Address 30

MSB															LSB
0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0

$S_{SUM} = S$

This is an unsigned value in the range of 0≤value<1.0, with the binary point to the right of the MSB.

6.6.45 Total Reactive Power (Q_{SUM}) – Page 16, Address 31

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0

$Q_{SUM} = Q_{AVG}$

This is a two's complement value in the range of -1.0 ≤ value < 1.0, with the binary point to the right of the MSB.

6.6.46 DC Offset for Current (I_{DCOFF}) – Page 16, Address 32

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0

DC offset registers I_{DCOFF} are initialized to zero on reset. During DC offset calibration, selected registers are written with the inverse of the DC offset measured. The application program can also write the DC offset register values. This is a two's complement value in the range of -1.0 ≤ value < 1.0, with the binary point to the right of the MSB.

6.6.47 DC Offset for Voltage (V_{DCOFF}) – Page 16, Address 34

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0

DC offset registers V_{DCOFF} are initialized to zero on reset. During DC offset calibration, selected registers are written with the inverse of the DC offset measured. The application program can also write the DC offset register values. It is a two's complement value in the range of -1.0 ≤ value < 1.0, with the binary point to the right of the MSB.

6.6.48 Gain for Current (I_{GAIN}) – Page 16, Address 33

MSB															LSB
2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default = 1.0

Gain register I_{GAIN} is initialized to 1.0 on reset. During gain calibration, the I_{GAIN} register is written with the multiplicative inverse of the gain measured. This is an unsigned fixed-point value in the range of 0 ≤ value < 4.0, with the binary point to the right of the second MSB.

6.6.49 Gain for Voltage (V_{GAIN}) – Page 16, Address 35

MSB															LSB
2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default = 1.0

Gain register V_{GAIN} is initialized to 1.0 on reset. During gain calibration, the V_{GAIN} register is written with the multiplicative inverse of the gain measured. This is an unsigned fixed-point value in the range of $0 \le \text{value} < 4.0$, with the binary point to the right of the second MSB.

6.6.50 Average Active Power Offset (P_{OFF}) – Page 16, Address 36

MSB															LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0

Average Active Power Offset (P_{OFF}) is added to the averaged active power to yield P_{AVG} register results. It can be used to reduce systematic energy errors. This is a two's complement value in the range of $-1.0 \le \text{value} < 1.0$, with the binary point to the right of the MSB.

6.6.51 Average Reactive Power Offset (Q_{OFF}) – Page 16, Address 38

MSB															LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x00 0000

Average Reactive Power Offset (Q_{OFF}) is added to the averaged active power to yield Q_{AVG} register results. It can be used to reduce systematic energy errors. It is a two's complement value in the range of $-1.0 \le \text{value} < 1.0$, with the binary point to the right of the MSB.

6.6.52 AC Offset for Current (I_{ACOFF}) – Page 16, Address 37

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Default = 0

AC offset register I_{ACOFF} is initialized to zero on reset. It is used to reduce systematic errors in the RMS results. This is an unsigned value in the range of $0 \le \text{value} < 1.0$, with the binary point to the left of the MSB.

6.6.53 Temperature Gain (T_{GAIN}) – Page 16, Address 54

MSB															LSB
2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	.....	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Default = 0x 06 B716

Register T_{GAIN} is used to scale the Temperature register (T), and is an unsigned fixed-point value in the range of $0.0 \le \text{value} < 256.0$, with the binary point to the right of bit 16.

Register T can be rescaled by the application using the T_{GAIN} and T_{OFF} registers. Refer to section *7.3 Temperature Sensor Calibration* on page 54 for more information.

6.6.54 Temperature Offset (T_{OFF}) – Page 16, Address 55

MSB															LSB
$-(2^7)$	2^6	2^5	2^4	2^3	2^2	2^1	2^0	.....	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Default = 0xD5 3998

Register T_{OFF} is used to offset the Temperature register (T), and is a two's complement value in the range of -128.0≤value<128.0 (°C), with the binary point to the right of bit 16.

Register T can be rescaled by the application using the T_{GAIN} and T_{OFF} registers. Refer to section *7.3 Temperature Sensor Calibration* on page 54 for more information.

6.6.55 Calibration Scale (Scale) – Page18, Address 63

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x4C CCCC (0.6)

The *Scale* register is used in the gain calibration to set the level of calibrated results of I-channel RMS. During gain calibration, the I_{RMS} results register is divided into the *Scale* register. The quotient is put into the I_{GAIN} register. It is a two's complement value in the range of -1.0 ≤ value < 1.0, with the binary point to the right of the MSB. Negative values are not used.

6.6.56 Zero-crossing Number (ZX_{NUM}) – Page 0, Address 55

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x00 0064 (100)

ZX_{NUM} is the number of zero crossings used for line frequency measurement. It is an integer in the range of 1 to 8,388,607. Zero should not be used.

6.6.57 V-channel Zero-crossing Threshold (VZX_{LEVEL}) – Page 18, Address 58

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x10 0000 (0.125)

VZX_{LEVEL} is the level that the peak instantaneous voltage must exceed for the zero-crossing detection to function. This is a two's complement value in the range of -1.0≤value<1.0, with the binary point to the right of the MSB. Negative values are not used.

6.6.58 I-channel Zero-crossing Threshold (IZX_{LEVEL}) – Page 18, Address 24

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x10 0000 (0.125)

IZX_{LEVEL} is the level that the peak instantaneous current must exceed for the zero-crossing detection to function. This is a two's complement value in the range of -1.0≤value<1.0, with the binary point to the right of the MSB. Negative values are not used.

7. SYSTEM CALIBRATION

Component tolerances, residual ADC offset, and system noise require a meter that needs to be calibrated before it meets a specific accuracy requirement. The CS5490 provides an on-chip calibration algorithm to operate the system calibration quickly and easily. Benefiting from the excellent linearity and low noise level of the CS5490, a CS5490 meter normally only needs one calibration at a single load point to achieve accurate measurements over the full load range.

7.1 Calibration in General

The CS5490 provides DC offset and gain calibration that can be applied to the instantaneous voltage and current measurements and AC offset calibration, which can only be applied to the current RMS calculation.

Since the voltage and current channels have independent offset and gain registers, offset and gain calibration can be performed on any channel independently.

The data flow of the calibration is shown in Figure 19.

Note that in Figure 19 the AC offset registers and gain registers affect the output results differently than the DC offset registers. The DC offset and gain values are applied to the voltage/current signals early in the signal path; the DC offset register and gain register values affect all CS5490 results. This is not true for the AC offset correction. The AC offset registers only affect the results of the RMS current calculation.

The CS5490 must be operating in its active state and ready to accept valid commands. Refer to section *6.1.2 Instructions* on page 24 for different calibration commands. The value in the *SampleCount* register determines the number (*N*) of output word rate (OWR) samples that are averaged during a calibration. The calibration procedure takes the time of $N + T_{SETTLE}$ OWR samples. As *N* is increased, the calibration takes more time, but the accuracy of the calibration results tends to increase.

The DRDY bit in the *Status0* register will be set at the completion of calibration commands. If an overflow occurs during calibration, other *Status0* bits may be set as well.

7.1.1 Offset Calibration

During offset calibrations, no line voltage or current should be applied to the meter; the differential signal on voltage inputs VIN± or current inputs IIN± of the CS5490 should be 0 volts.

7.1.1.1 DC Offset Calibration

The DC offset calibration command measures and averages DC values read on specified voltage or current channels at zero input and stores the inverse result in the associated offset registers. This DC offset will be added to instantaneous measurements in subsequent conversions, removing the offset.

The gain register for the channel being calibrated should be set to 1.0 prior to performing DC offset calibration.

DC offset calibration is not required if the high-pass filter is enabled on that channel because the DC component will be removed by the high-pass filter.

7.1.1.2 AC Offset Calibration

The AC offset calibration applies only to the current channel. It measures the residual RMS values on the current channel at zero input and stores the squared

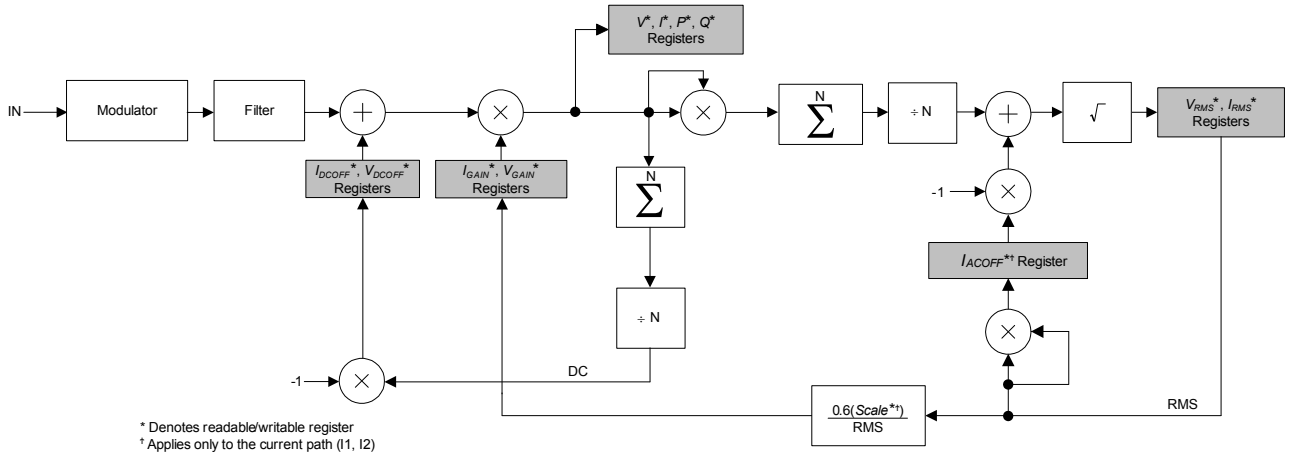


Figure 19. Calibration Data Flow

result in the AC offset register. This AC offset will be subtracted from RMS measurements in subsequent conversions, removing the AC offset on the current channel.

The AC offset register for the channel being calibrated should first be cleared prior to performing the calibration. The high-pass filter should be enabled if AC offset calibration is used. It is recommended that T_{SETTLE} be set to 2000 ms before performing an AC offset calibration. Note that the AC offset register holds the square of the RMS value measured during calibration. Therefore, it can hold a maximum RMS noise of $\sqrt{0xFFFFFF}$. This is the maximum RMS noise that AC offset correction can remove.

7.1.2 Gain Calibration

Prior to executing the gain calibration command, gain registers for any path to be calibrated (V_{GAIN}, I_{GAIN}) should be set to '1.0,' and T_{SETTLE} should be set to 2000 ms. For gain calibration, a reference signal must be applied to the meter. During gain calibration, the voltage RMS result register (V_{RMS}) is divided into '0.6,' and the current RMS result register (I_{RMS}) is divided into the *Scale* register. The quotient is put into the associated gain register. The gain calibration algorithm attempts to adjust the gain register (V_{GAIN}, I_{GAIN}) such that the voltage RMS result register (V_{RMS}) equals '0.6,' and the current RMS result register (I_{RMS}) equals the *Scale* register.

Note that for the gain calibration, there are limitations on choosing the reference level and the *Scale* register value. Using a reference or a scale that is too large or too small can cause register overflow during calibration or later during normal operation. Either condition can set *Status* register bits IOR and VOR. The maximum value that the gain register can attain is '4.' Using inappropriate reference levels or scale values may also cause the CS5490 to attempt to set the gain register higher than '4.' Therefore, the gain calibration result will be invalid.

The *Scale* register is '0.6' by default. The maximum voltage (U_{MAX} Volts) and current (I_{MAX} Amps) of the meter should be used as the reference signal level if the *Scale* register is '0.6.' After gain calibration, '0.6' of the V_{RMS} (I_{RMS}) registers represents U_{MAX} Volts (I_{MAX} Amps) for the line voltage (load current); '0.36' of the P_{AVG}, Q_{AVG}, or S register represents $U_{MAX} \times I_{MAX}$ Watts, Vars, or VAs for the active, reactive, or apparent power.

If the calibration is performed with U_{MAX} Volts and I_{CAL} Amps and $I_{CAL} < I_{MAX}$, the *Scale* register needs to be scaled down to $0.6 \times I_{CAL} / I_{MAX}$ before performing gain calibration. After gain calibration, '0.6' of the V_{RMS} register represents U_{MAX} Volts, $0.6 \times I_{CAL} / I_{MAX}$ of the I_{RMS} register represents I_{CAL} Amps, and $0.36 \times I_{CAL} / I_{MAX}$ of the P_{AVG}, Q_{AVG}, or S register represents $U_{MAX} \times I_{CAL}$ Watts, Vars, or VAs.

7.1.3 Calibration Order

1) If the HPF option is enabled, then any DC component that may be present in the selected signal channel will be removed, and a DC offset calibration is not required. However, if the HPF option is disabled, the DC offset calibration should be performed.

   When using high-pass filters, it is recommended that the DC offset register for the corresponding channel be set to 0. Before performing DC offset calibration, the DC offset register should be set to 0, and the corresponding gain register should be set to 1.

2) If there is an AC offset in the I_{RMS} calculation, the AC offset calibration should be performed on the current channel. Before performing AC offset calibration, the AC offset register should be set to 0.

3) Perform the gain calibration.

4) If an AC offset calibration was performed (step 2), then the AC offset may need to be adjusted to compensate for the change in gain (step 3). This can be accomplished by restoring zero to the AC offset register and then performing an AC offset calibration. The adjustment could also be done by multiplying the AC offset register value that was calculated in step 2 by the gain calculated in step 3 and updating the AC offset register with the product.

7.2 Phase Compensation

A phase compensation mechanism is provided to adjust for meter-to-meter variation in signal path delays.
Phase offset between a voltage channel and its corresponding current channel can be calculated by using the power factor (*PF*) register after a conversion.

1) Apply a reference voltage and current with a lagging power factor to the meter. The reference current waveform should lag the voltage with a 60° phase shift.

2) Start continuous conversion.

3) Accumulate multiple readings of the *PF* register.

4) Calculate the average power factor, PF_{avg}.

5) Calculate phase offset = $\arccos(PF_{avg}) - 60°$.

6) If the phase offset is negative, then the delay should be added only to the current channel. Otherwise, add more delay to the voltage channel than to the current channel to compensate for a positive phase offset.

Once the phase offset is known, the CPCC and FPCC bits for that channel are calculated and programmed in the *PC* register.

CPCC bits are used if either

- The phase offset is more than 1 output word rate (OWR) sample.
- More delay is needed on the voltage channel.

The compensation resolution is 0.008789° at 50Hz and 0.010547° at 60Hz at an OWR of 4000Hz.

7.3 Temperature Sensor Calibration

Temperature sensor calibration involves the adjustment of two parameters: temperature gain (T_{GAIN}) and temperature offset (T_{OFF}). Before calibration, T_{GAIN} must be set to 1.0 (0x 01 0000), and T_{OFF} must be set to 0.0 (0x 00 0000).

7.3.1 Temperature Offset and Gain Calibration

To obtain the optimal temperature offset (T_{OFF}) register value and temperature (T_{GAIN}) register value, it is necessary to measure the temperature (T) register at a minimum of two points (T1 and T2) across the meter operating temperature range. The two temperature points must be far enough apart to yield reasonable accuracy, for example 25°C and 85°C. Obtain a linear fit of these points ($y = m \cdot x + b$), where the slope (m) and intercept (b) can be obtained.

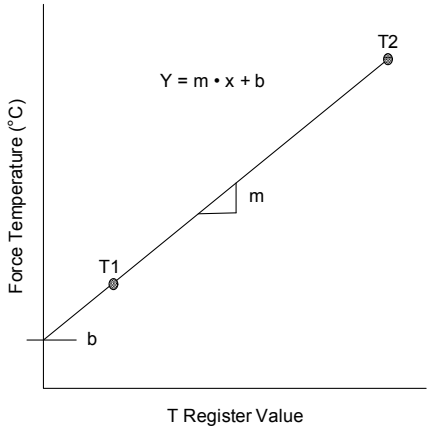


Figure 20. T Register vs. Force Temp

T_{OFF} and T_{GAIN} are calculated using the equations below:

$$T_{OFF} = \frac{b}{m}$$

$$T_{GAIN} = m$$

8. BASIC APPLICATION CIRCUITS

The CS5490 is configured to measure power in a single-phase, two-wire single voltage and current system, as illustrated in Figure 21. In this diagram, a current transformer (CT) is used to sense the line load current, and a resistive voltage divider is used to sense the line voltage.

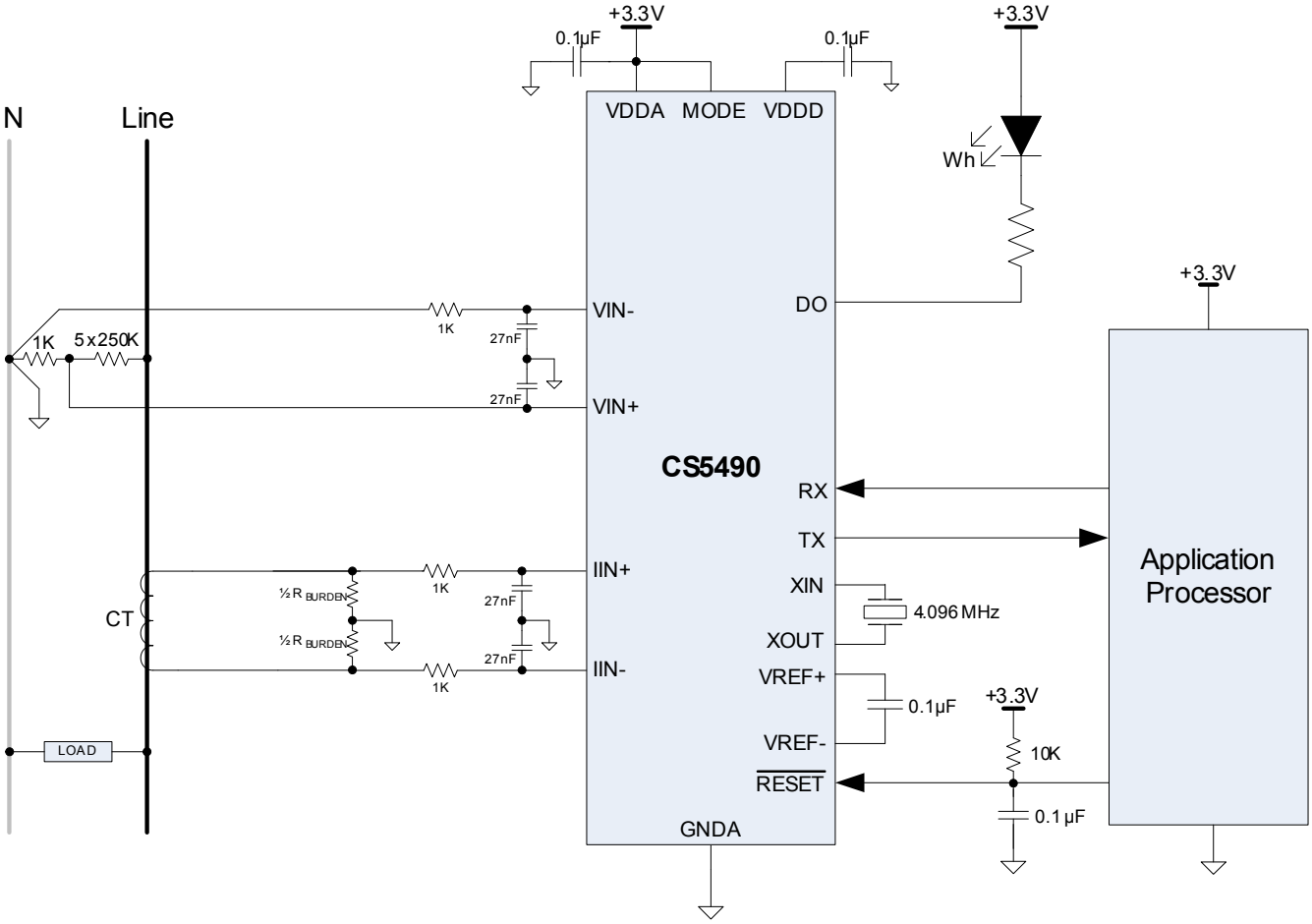
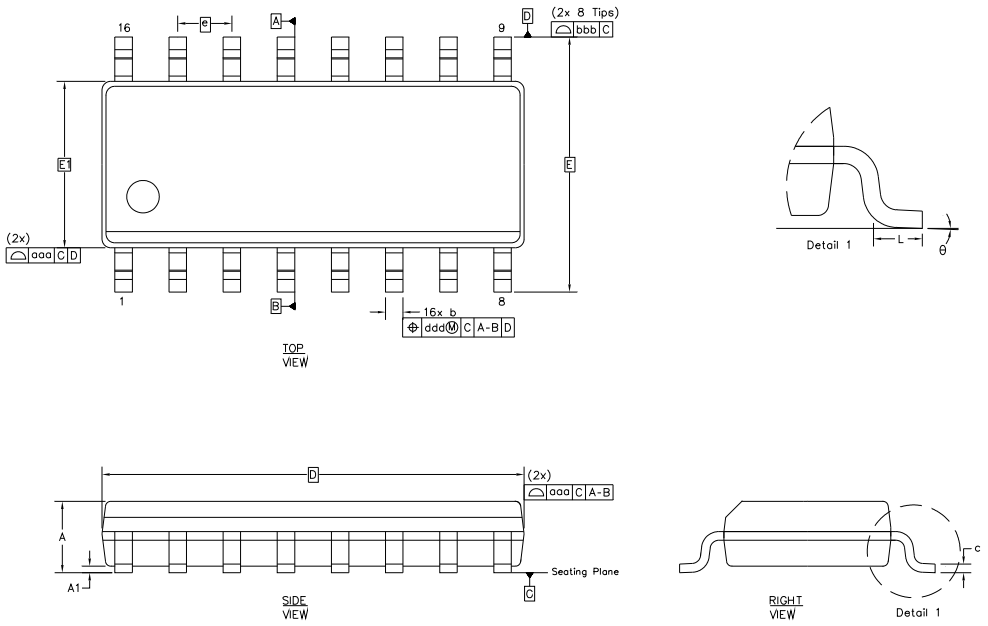


Figure 21. Typical Connection Diagram *(Single-phase, Two-wire, Power Meter)*

9. PACKAGE DIMENSIONS

16 SOIC (150 MIL BODY) PACKAGE DRAWING



	mm			inch		
Dimension	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	- -	- -	1.75	- -	- -	0.069
A1	0.10	- -	0.25	0.004	- -	0.010
b	0.31	- -	0.51	0.012	- -	0.020
c	0.10	- -	0.25	0.004	- -	0.010
D	9.90 BSC			0.390 BSC		
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.05 BSC		
L	0.40	- -	1.27	0.016	- -	0.050
Θ	0°	- -	8°	0°	- -	8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ddd	0.25			0.010		

Notes:

1. Controlling dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M.
3. This drawing conforms to JEDEC outline MS-012, variation AC for standard 16 SOIC narrow body.
4. Recommended reflow profile is per JEDEC/IPC J-STD-020.

10. ORDERING INFORMATION

Ordering Number	Container	Temperature	Package
CS5490-ISZ	Bulk	-40 to +85 °C	16-pin SOIC, Lead (Pb) Free
CS5490-ISZR	Tape & Reel		

11. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Part Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5490-ISZ	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

12. REVISION HISTORY

Revision	Date	Changes
PP1	APR 2012	Preliminary release.
F1	APR 2012	Edited for content and clarity.
F2	JUN 2012	Updated ordering information.
F3	MAR 2013	Clarified context.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com