CS5530

24-bit ADC with Ultra-low-noise Amplifier

Features

- Chopper-stabilized Instrumentation Amplifier, 64X
  - 12 nV/√Hz @ 0.1 Hz (No 1/f noise)
  - 1200 pA Input Current
- Digital Gain Scaling up to 40x
- Delta-sigma Analog-to-digital Converter
  - Linearity Error: 0.0015% FS
  - Noise Free Resolution: Up to 19 bits
- Scalable V_{REF} Input: Up to Analog Supply
- Simple Three-wire Serial Interface
  - SPI™ and Microwire™ Compatible
  - Schmitt-trigger on Serial Clock (SCLK)
- Onboard Offset and Gain Calibration Registers
- Selectable Word Rates: 6.25 to 3,840 Sps
- Selectable 50 or 60 Hz Rejection
- Power Supply Configurations
  - VA+ = +5 V; VA- = 0 V; VD+ = +3 V to +5 V
  - VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V to +5 V
  - VA+ = +3 V; VA- = -3 V; VD+ = +3 V

General Description

The CS5530 is a highly integrated ΔΣ Analog-to-Digital Converter (ADC) which uses charge-balance techniques to achieve 24-bit performance. The ADC is optimized for measuring low-level unipolar or bipolar signals in weigh scale, process control, scientific, and medical applications.

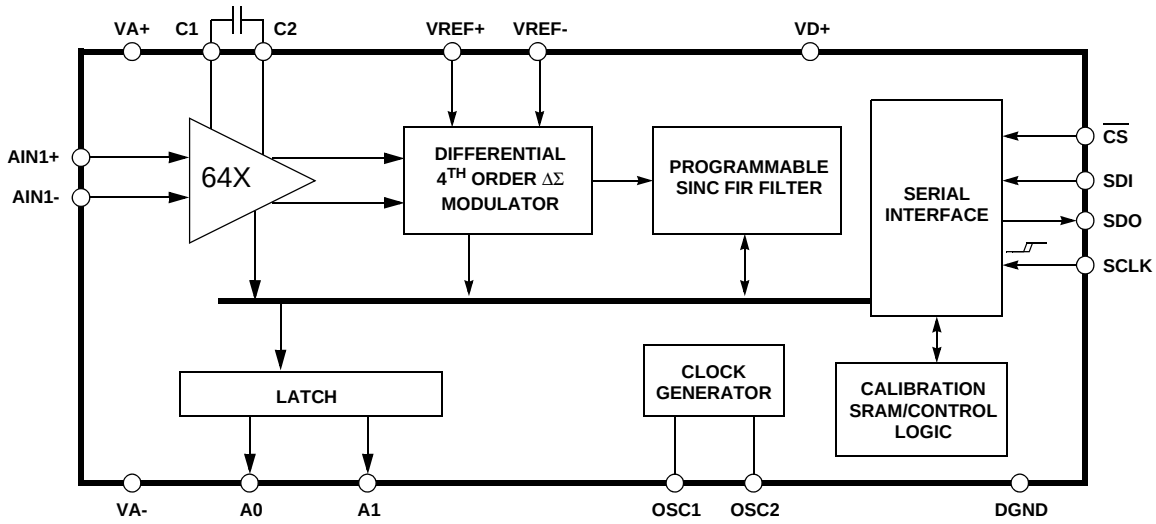
To accommodate these applications, the ADC includes a very-low-noise, chopper-stabilized instrumentation amplifier (12 nV/√Hz @ 0.1 Hz) with a gain of 64X. This device also includes a fourth-order ΔΣ modulator followed by a digital filter which provides twenty selectable output word rates of 6.25, 7.5, 12.5, 15, 25, 30, 50, 60, 100, 120, 200, 240, 400, 480, 800, 960, 1600, 1920, 3200, and 3840 Sps (MCLK = 4.9152 MHz).

To ease communication between the ADC and a microcontroller, the converter includes a simple three-wire serial interface which is SPI and Microwire compatible with a Schmitt-trigger input on the serial clock (SCLK).

High dynamic range, programmable output rates, and flexible power supply options make this device an ideal solution for weigh scale and process control applications.

ORDERING INFORMATION

See page 35.



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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARCTERISTICS

(VA+, VD+ = 5 V ±5%; VREF+ = 5 V; VA-, VREF-, DGND = 0 V; MCLK = 4.9152 MHz;
OWR (Output Word Rate) = 60 Sps; Bipolar Mode)
(See Notes 1 and 2.)

Parameter	CS5530-CS			Unit
	Min	Typ	Max	
Accuracy				
Linearity Error	-	±0.0015	±0.003	%FS
No Missing Codes	24	-	-	Bits
Bipolar Offset	-	±16	±32	LSB_{24}
Unipolar Offset	-	±32	±64	LSB_{24}
Offset Drift (Notes 3 and 4)	-	10	-	nV/°C
Bipolar full-scale Error	-	±8	±31	ppm
Unipolar full-scale Error	-	±16	±62	ppm
full-scale Drift (Note 4)	-	2	-	ppm/°C

Notes:
1. Applies after system calibration at any temperature within -40 °C to +85 °C.
2. Specifications guaranteed by design, characterization, and/or test. LSB is 24 bits.
3. This specification applies to the device only and does not include any effects by external parasitic thermocouples.
4. Drift over specified temperature range after calibration at power-up at 25 °C.

ANALOG CHARACTERISTICS (Continued)

(See Notes 1 and 2.)

Parameter		Min	Typ	Max	Unit
Analog Input					
Common Mode + Signal on AIN+ or AIN-	Bipolar/Unipolar Mode	(VA-) + 1.6	-	(VA+) - 1.6	V
CVF Current on AIN+ or AIN-		-	1200	-	pA
Input Current Noise		-	1	-	pA/√Hz
Open Circuit Detect Current		100	300	-	nA
Common Mode Rejection	DC 50, 60 Hz	- -	130 120	- -	dB dB
Input Capacitance		-	10	-	pF
Voltage Reference Input					
Range	(VREF+) - (VREF-)	1	2.5	(VA+)-(VA-)	V
CVF Current	(Note 5, 6)	-	50	-	nA
Common Mode Rejection	DC 50, 60 Hz	- -	120 120	- -	dB dB
Input Capacitance		11	-	22	pF
System Calibration Specifications					
Full-scale Calibration Range	Bipolar/Unipolar Mode	3	-	110	%FS
Offset Calibration Range	Bipolar Mode	-100	-	100	%FS
Offset Calibration Range	Unipolar Mode	-90	-	90	%FS

Notes: 5. See the section of the data sheet which discusses input models.

6. Input current on VREF+ or VREF- may increase to 250 nA if operated within 50 mV of VA+ or VA-. This is due to the rough charge buffer being saturated under these conditions.

ANALOG CHARACTERISTICS (Continued)

(See Notes 1 and 2.)

Parameter			CS5530-CS Min	CS5530-CS Typ	CS5530-CS Max	Unit
Power Supplies						
DC Power Supply Currents (Normal Mode)	I_{A+}, I_{A-}		-	6	8	mA
	I_{D+}		-	0.6	1.0	mA
Power Consumption	Normal Mode	(Note 7)	-	35	45	mW
	Standby		-	5	-	mW
	Sleep		-	500	-	µW
Power Supply Rejection		(Note 8)				
	DC Positive Supplies		-	115	-	dB
	DC Negative Supply		-	115	-	dB

7. All outputs unloaded. All input CMOS levels.
8. Tested with 100 mV change on VA+ or VA-.

TYPICAL NOISE-FREE RESOLUTION (BITS) (See Notes 9 and 10)

Output Word Rate (Sps)	-3 dB Filter Frequency (Hz)	Noise-free Bits	Noise (nV_{rms})
7.5	1.94	19	17
15	3.88	19	24
30	7.75	18	34
60	15.5	18	48
120	31	17	68
240	62	16	115
480	122	16	163
960	230	15	229
1,920	390	15	344
3,840	780	13	1390

9. Noise Free Resolution listed is for Bipolar operation, and is calculated as LOG((Input Span)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. For Unipolar operation, the input span is 1/2 as large, so one bit is lost. The input span is calculated in the analog input span section of the data sheet. The Noise Free Resolution table is computed with a value of 1.0 in the gain register. Values other than 1.0 will scale the noise, and change the Noise Free Resolution accordingly.
10. “Noise Free Resolution” is not the same as “Effective Resolution”. Effective Resolution is based on the RMS noise value, while Noise Free Resolution is based on a peak-to-peak noise value specified as 6.6 times the RMS noise value. Effective Resolution is calculated as LOG((Input Span)/(RMS Noise))/LOG(2).

Specifications are subject to change without notice.

5 V DIGITAL CHARACTERISTICS

(VA+, VD+ = 5 V ±5%; VA-, DGND = 0 V; See Notes 2 and 11.)

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	All Pins Except SCLK SCLK	V_{IH}	0.6 VD+ (VD+) - 0.45	- -	VD+ VD+	V
Low-Level Input Voltage	All Pins Except SCLK SCLK	V_{IL}	0.0 0.0	-	0.8 0.6	V
High-Level Output Voltage	A0 and A1, I_{out} = -1.0 mA SDO, I_{out} = -5.0 mA	V_{OH}	(VA+) - 1.0 (VD+) - 1.0	-	-	V
Low-Level Output Voltage	A0 and A1, I_{out} = 1.0 mA SDO, I_{out} = 5.0 mA	V_{OL}	-	-	(VA-) + 0.4 0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
SDO 3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

3 V DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+ = 5V ±5%; VD+ = 3.0V±10%; VA-, DGND = 0V; See Notes 2 and 11.)

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	All Pins Except SCLK SCLK	V_{IH}	0.6 VD+ (VD+) - 0.45	-	VD+ VD+	V
Low-Level Input Voltage	All Pins Except SCLK SCLK	V_{IL}	0.0 0.0	-	0.8 0.6	V
High-Level Output Voltage	A0 and A1, I_{out} = -1.0 mA SDO, I_{out} = -5.0 mA	V_{OH}	(VA+) - 1.0 (VD+) - 1.0	-	-	V
Low-Level Output Voltage	A0 and A1, I_{out} = 1.0 mA SDO, I_{out} = 5.0 mA	V_{OL}	-	-	(VA-) + 0.4 0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
SDO 3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

11. All measurements performed under static conditions.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Unit
Modulator Sampling Rate	f_s	MCLK/16	Sps
Filter Settling Time to 1/2 LSB (full-scale Step Input)			
Single Conversion mode (Notes 12, 13, and 14)	t_s	$1/OWR_{SC}$	s
Continuous Conversion mode, OWR < 3200 Sps	t_s	$5/OWR_{sinc5} + 3/OWR$	s
Continuous Conversion mode, OWR ≥ 3200 Sps	t_s	5/OWR	s

12. The ADCs use a $Sinc^5$ filter for the 3200 Sps and 3840 Sps output word rate (OWR) and a $Sinc^5$ filter followed by a $Sinc^3$ filter for the other OWRs. OWR_{sinc5} refers to the 3200 Sps (FRS = 1) or 3840 Sps (FRS = 0) word rate associated with the $Sinc^5$ filter.
13. The single conversion mode only outputs fully settled conversions. See Table 1 for more details about single conversion mode timing. OWR_{SC} is used here to designate the different conversion time associated with single conversions.
14. The continuous conversion mode outputs every conversion. This means that the filter's settling time with a full-scale step input in the continuous conversion mode is dictated by the OWR.

ABSOLUTE MAXIMUM RATINGS

(DGND = 0 V; See Note 15.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 16 and 17)					
Positive Digital		VD+	-0.3	-	+6.0	V
Positive Analog		VA+	-0.3	-	+6.0	V
Negative Analog		VA-	+0.3	-	-3.75	V
Input Current, Any Pin Except Supplies	(Notes 18 and 19)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Power Dissipation	(Note 20)	PDN	-	-	500	mW
Analog Input Voltage	VREF pins	V_{INR}	(VA-) -0.3	-	(VA+) + 0.3	V
	AIN Pins	V_{INA}	(VA-) -0.3	-	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 15. All voltages with respect to ground.

16. VA+ and VA- must satisfy {(VA+) - (VA-)} ≤ +6.6 V.
17. VD+ and VA- must satisfy {(VD+) - (VA-)} ≤ +7.5 V.
18. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.
19. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.
20. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

(VA+ = 2.5 V or 5 V ±5%; VA- = -2.5V±5% or 0 V; VD+ = 3.0 V ±10% or 5 V ±5%;DGND = 0 V; Levels: Logic 0 = 0 V, Logic 1 = VD+; C_L = 50 pF; See Figures 1 and 2.)

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency (Note 21) External Clock or Crystal Oscillator	MCLK	1	4.9152	5	MHz
Master Clock Duty Cycle		40	-	60	%
Rise Times (Note 22) Any Digital Input Except SCLK SCLK Any Digital Output	t_{rise}	 - - -	 - - 50	 1.0 100 -	 µs µs ns
Fall Times (Note 22) Any Digital Input Except SCLK SCLK Any Digital Output	t_{fall}	 - - -	 - - 50	 1.0 100 -	 µs µs ns
Start-up					
Oscillator Start-up Time XTAL = 4.9152 MHz (Note 23)	t_{ost}	-	20	-	ms
Serial Port Timing					
Serial Clock Frequency	SCLK	0	-	2	MHz
Serial Clock Pulse Width High Pulse Width Low	t_1 t_2	250 250	- -	- -	ns ns
SDI Write Timing					
$\overline{CS}$ Enable to Valid Latch Clock	t_3	50	-	-	ns
Data Set-up Time prior to SCLK rising	t_4	50	-	-	ns
Data Hold Time After SCLK Rising	t_5	100	-	-	ns
SCLK Falling Prior to $\overline{CS}$ Disable	t_6	100	-	-	ns
SDO Read Timing					
$\overline{CS}$ to Data Valid	t_7	-	-	150	ns
SCLK Falling to New Data Bit	t_8	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z	t_9	-	-	150	ns

Notes: 21. Device parameters are specified with a 4.9152 MHz clock.

22. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

23. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

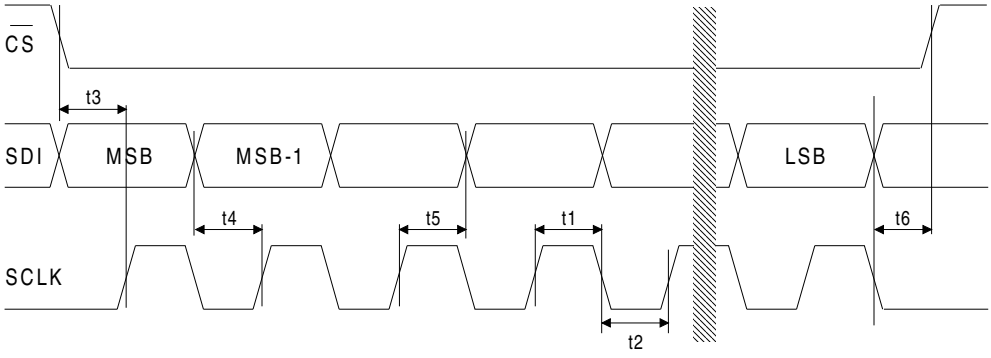


Figure 1. SDI Write Timing (Not to Scale)

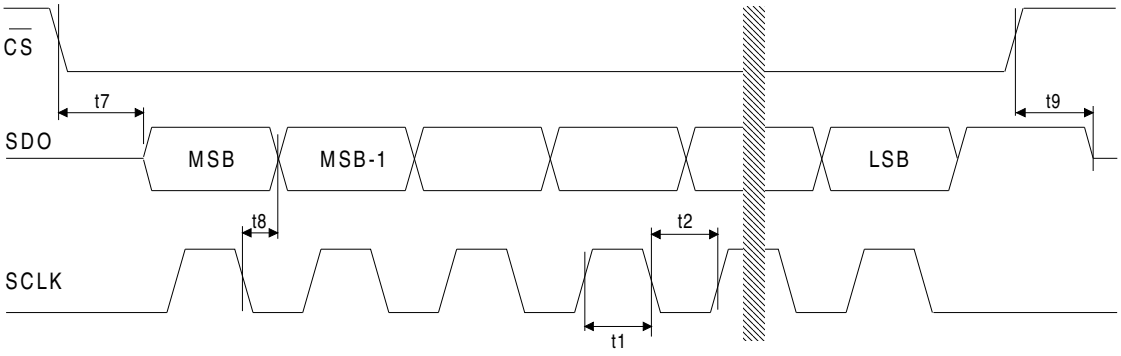


Figure 2. SDO Read Timing (Not to Scale)

2. GENERAL DESCRIPTION

The CS5530 is a ΔΣ Analog-to-Digital Converter (ADC) which uses charge-balance techniques to achieve 24-bit performance. The ADC is optimized for measuring low-level unipolar or bipolar signals in weigh scale, process control, scientific, and medical applications.

To accommodate these applications, the ADC includes a very-low-noise, chopper-stabilized instrumentation amplifier (12 nV/√Hz @ 0.1 Hz) with a gain of 64X. This ADC also includes a fourth-order ΔΣ modulator followed by a digital filter which provides twenty selectable output word rates of 6.25, 7.5, 12.5, 15, 25, 30, 50, 60, 100, 120, 200, 240, 400, 480, 800, 960, 1600, 1920, 3200, and 3840 samples per second (MCLK = 4.9152 MHz).

To ease communication between the ADCs and a micro-controller, the converters include a simple three-wire serial interface which is SPI and Microwire compatible with a Schmitt-trigger input on the serial clock (SCLK).

2.1 Analog Input

Figure 3 illustrates a block diagram of the CS5530. The front end includes a chopper-stabilized instrumentation amplifier with a gain of 64X.

The amplifier is chopper-stabilized and operates with a chop clock frequency of MCLK/128. The CVF (sampling) current into the instrumentation amplifier is typically 1200 pA over -40°C to +85°C (MCLK=4.9152 MHz). The common-mode plus signal range of the instrumentation amplifier is (VA-) + 1.6 V to (VA+) - 1.6 V.

Figure 4 illustrates the input model for the 64X amplifier.

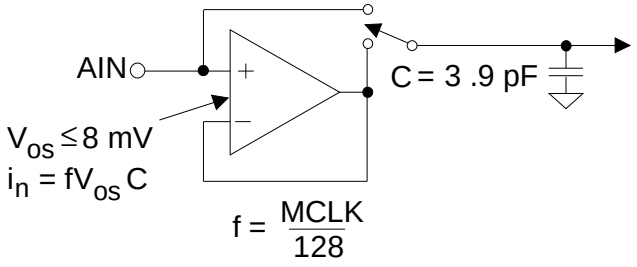


Figure 4. Input Model for AIN+ and AIN- Pins

Note: The C = 3.9 pF capacitor is for input current modeling only. For physical input capacitance see 'Input Capacitance' specification under *Analog Characteristics*.

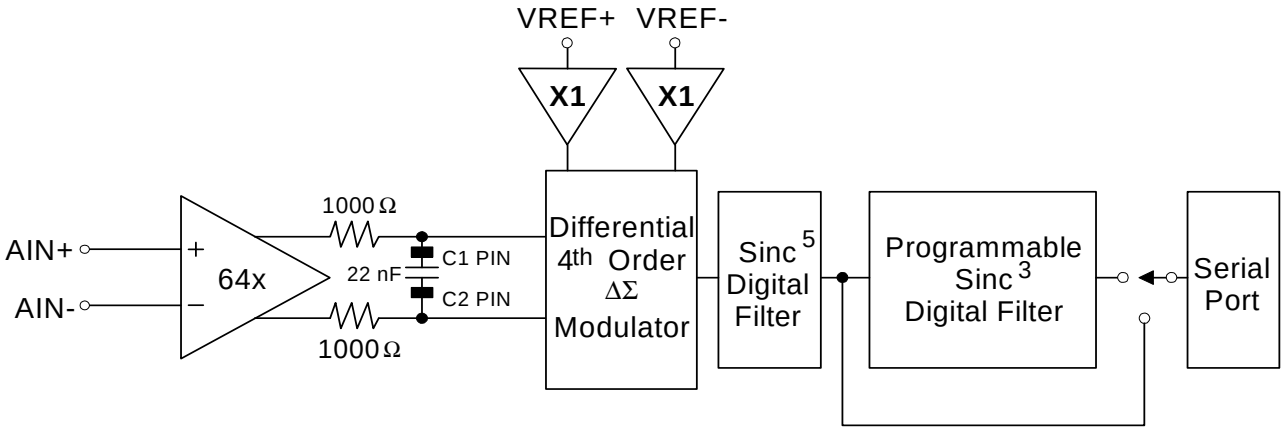


Figure 3. Front End Configuration

2.1.1 Analog Input Span

The full-scale input signal that the converter can digitize is a function of the reference voltage connected between the VREF+ and VREF- pins. The full-scale input span of the converter is
((VREF+) – (VREF-))/(64Y), where 64 is the gain of the amplifier and Y is 2 for VRS = 0, or Y is 1 for VRS = 1. VRS is the Voltage Reference Select bit, and must be set according to the differential voltage applied to the VREF+ and VREF- pins on the part. See section 2.3.4 for more details.

With a 2.5 V reference, the full-scale biploar input range is equal to ±2.5/64, or about ±39 mV. Note that these input ranges assume the calibration registers are set to their default values (i.e. Gain = 1.0 and Offset = 0.0). The gain setting in the Gain Register can be altered to map the digital codes of the converter to set full scales from 1 mV to 40 mV.

2.1.2 Voltage Noise Density Performance

Figure 5 illustrates the measured voltage noise density versus frequency from 0.025 Hz to 10 Hz. The device was powered with ±2.5 V supplies, using 30 Sps OWR, bipolar mode, and with the input short bit enabled.

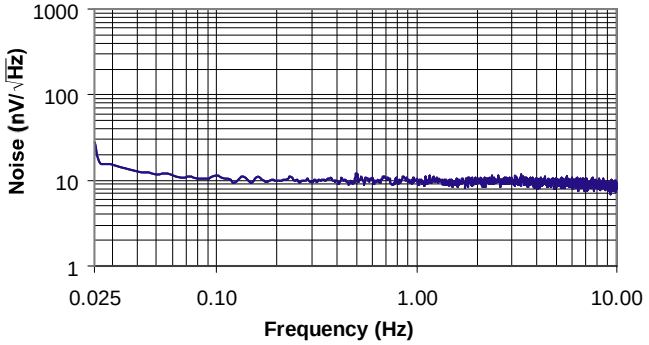


Figure 5. Measured Voltage Noise Density, 64x

2.1.3 No Offset DAC

An offset DAC was not included in the CS5530 because the high dynamic range of the converter eliminates the need for one. The offset register can be manipulated by the user to mimic the function of a DAC if desired.

2.2 Overview of ADC Register Structure and Operating Modes

The CS5530 ADC has an on-chip controller, which includes a number of user-accessible registers. The registers are used to hold offset and gain calibration results, configure the chip's operating modes, hold conversion instructions, and to store conversion data words. Figure 6 depicts a block diagram of the on-chip controller's internal registers.

The converter has 32-bit registers to function as the offset and the gain calibration registers. These registers hold calibration results. The contents of these registers can be read or written by the user. This allows calibration data to be off-loaded into an external EEPROM. The user can also manipulate the contents of these registers to modify the offset or the gain slope of the converter.

The converter includes a 32-bit configuration register which is used for setting options such as the power down modes, resetting the converter, shorting the analog input, enabling logic outputs, and other user options.

The following pages document how to initialize the converter and perform offset and gain calibrations. Each of the bits of the configuration register is described. Also the *Command Register Quick Reference* can be used to decode all valid commands (the first 8-bits into the serial port).

2.2.1 System Initialization

The CS5530 provide no power-on-reset function. To initialize the ADC, the user must perform a software reset via the configuration register. Before accessing the configuration register, the user must insure serial port synchronization by using the Serial Port Initialization sequence. This sequence resets the serial port to the command mode and is accomplished by transmitting at least 15 SYNC1 command bytes (0xFF hexadecimal), followed by one SYNC0 command (0xFE hexadecimal). Note that this sequence can be initiated at anytime to reinitialize the serial port. To complete the system

initialization sequence, the user must also perform a system reset sequence which is as follows: Write a logic 1 into the RS bit of the configuration register. This will reset the calibration registers and other logic (but not the serial port). A valid reset will set the RV bit in the configuration register to a logic 1. After writing the RS bit to a logic 1, wait 8 master clock cycles, then write the RS bit back to logic 0. Note that the other bits in the configuration register cannot be written on this write cycle as they are being held in reset until RS is set back to logic 0. While this involves writing an entire word into the configuration register to casue the RS bit to go to logic 0, the RV bit is a read only bit, therefore a write to the configuration register will not overwrite the RV bit. After clearing the RS bit back to logic 0, read the configuration register to check the state of the RV bit as this indicates that a valid reset occurred. Reading the configuration register clears the RV bit back to logic 0.

Completing the reset cycle initializes the on-chip registers to the following states:

Configuration Register:	00000000(H)
Offset Register:	00000000(H)
Gain Register	01000000(H)

After the configuration register has been read to clear the RV bit, the register can then be written to set the other function bits or other registers can be written or read.

Once the system initialization or reset is completed, the on-chip controller is initialized into command mode where it waits for a valid command (the first 8-bits written into the serial port are shifted into the command register). Once a valid command is received and decoded, the byte instructs the converter to either acquire data from or transfer data to an internal register, or perform a conversion or a calibration. The *Command Register Descriptions* section lists all valid commands.

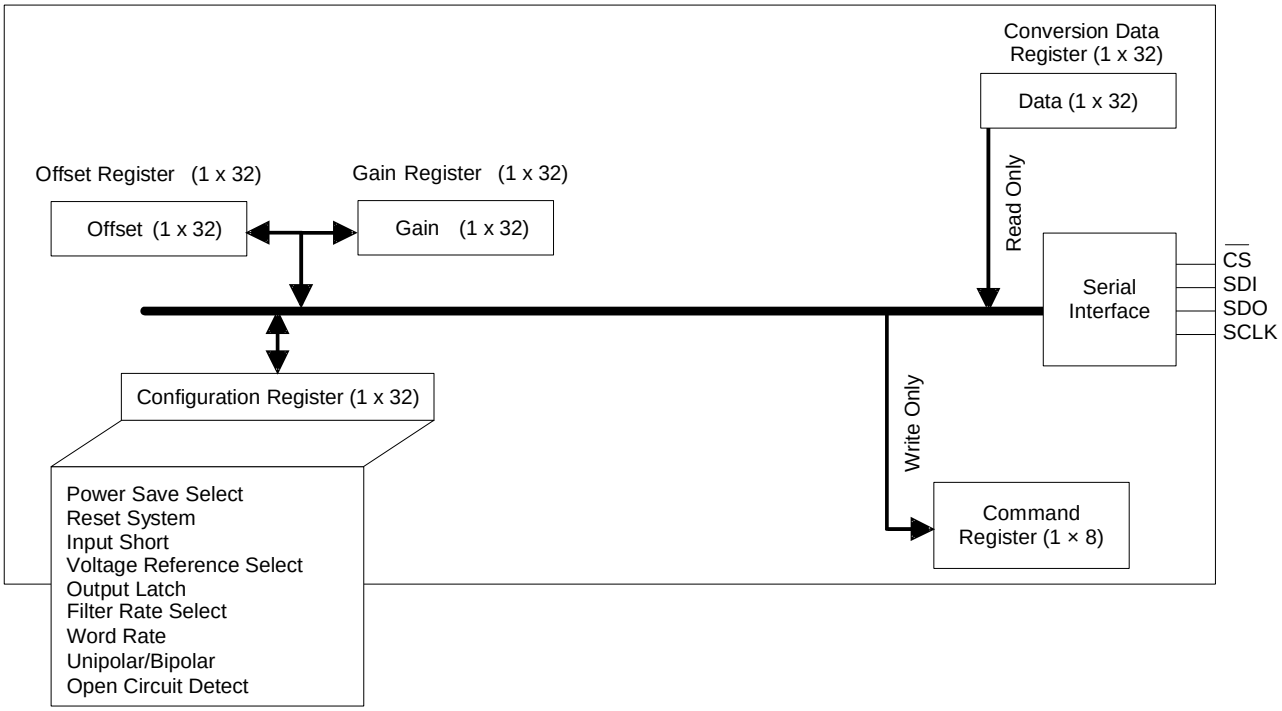


Figure 6. CS5530 Register Diagram

2.2.2 Command Register Descriptions

READ/$\overline{\text{WRITE}}$ OFFSET REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	R/$\overline{W}$	0	0	1

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write offset register.

1 Read offset register.

READ/$\overline{\text{WRITE}}$ GAIN REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	R/$\overline{W}$	0	1	0

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write gain register.

1 Read gain register.

READ/$\overline{\text{WRITE}}$ CONFIGURATION REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	R/$\overline{W}$	0	1	1

Function: These commands are used to read from or write to the configuration register.

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write configuration register.

1 Read configuration register.

PERFORM CONVERSION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	0	0	0	0	0	0

MC (Multiple Conversions)

0 Perform a single conversion.

1 Perform continuous conversions.

PERFORM SYSTEM OFFSET CALIBRATION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	1

PERFORM SYSTEM GAIN CALIBRATION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	1	0

SYNC1

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Function: Part of the serial port re-initialization sequence.

SYNC0

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	0

Function: *End of the serial port re-initialization sequence.*

NULL

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Function: *This command is used to clear a port flag and keep the converter in the continuous conversion mode.*

2.2.3 Serial Port Interface

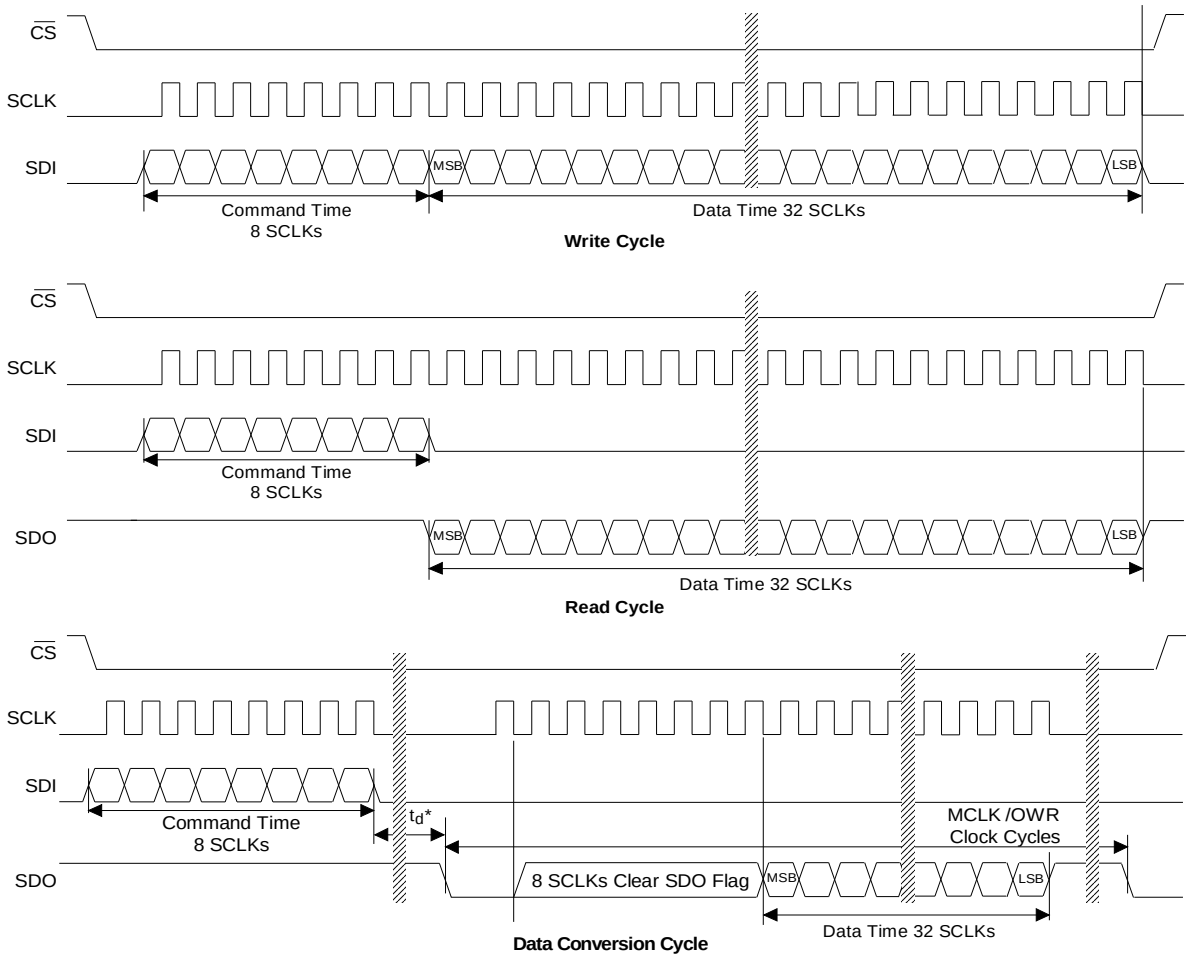
The CS5530's serial interface consists of four control lines: $\overline{CS}$, SDI, SDO, SCLK. Figure 7 details the command and data word timing.

$\overline{CS}$, Chip Select, is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied low, the port can function as a three wire interface.

SDI, Serial Data In, is the data signal used to transfer data to the converters.

SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1.

SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held low (logic 0) before SCLK transitions can be recognized by the port logic. To accommodate optoisolators SCLK is designed with a Schmitt-trigger input to allow an optoisolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an optoisolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.



* td is the time it takes the ADC to perform a conversion. See the Single Conversion and Continuous Conversion sections of the data sheet for more details about conversion timing.

Figure 7. Command and Data Word Timing

2.2.4 Reading/Writing On-Chip Registers

The CS5530's offset, gain, and configuration registers are readable and writable while the conversion data register is read only.

As shown in Figure 7, to write to a particular register the user must transmit the appropriate write command and then follow that command by 32 bits of data. For example, to write 0x80000000 (hexadecimal) to the gain register, the user would first transmit the command byte 0x02 (hexadecimal) followed by the data 0x80000000 (hexadecimal). Similarly, to read a particular register the user must transmit the appropriate read command and then acquire the 32 bits of data. Once a register is written to or read from, the serial port returns to the command mode.

2.3 Configuration Register

To ease the architectural design and simplify the serial interface, the configuration register is thirty-two bits long, however, only fifteen of the thirty two bits are used. The following sections detail the bits in the configuration register.

2.3.1 Power Consumption

The CS5530 accommodates three power consumption modes: normal, standby, and sleep. The default mode, "normal mode", is entered after power is applied. In this mode, the CS5530 typically consumes 35 mW. The other two modes are referred to as the power save modes. They power down most of the analog portion of the chip and stop filter convolutions. The power save modes are entered whenever the power down (PDW) bit of the configuration register is set to logic 1. The particular power save mode entered depends on state of the PSS (Power Save Select) bit. If PSS is logic 0, the converter enters the standby mode reducing the power consumption to 4 mW. The standby mode leaves the oscillator and the on-chip bias generator for the analog portion of the chip active. This allows the converter to quickly return to the normal mode once PDW is set back to a logic 0. If PSS and PDW are both set to logic 1, the sleep mode is entered reducing the consumed power to around 500 µW. Since this sleep mode disables the oscillator, approximately a 20 ms oscillator start-up delay period is required before returning to the normal mode. If an external clock is used, there will be no delay.

2.3.2 System Reset Sequence

The reset system (RS) bit permits the user to perform a system reset. A system reset can be initiated at any time by writing a logic 1 to the RS bit in the configuration register. After the RS bit has been set, the internal logic of the chip will be initialized to a reset state. The reset valid (RV) bit is set indicating that the internal logic was properly reset. The RV bit is cleared after the configuration register is read. The on-chip registers are initialized to the following default states:

Configuration Register:	00000000(H)
Offset Register:	00000000(H)
Gain Register	01000000(H)

After reset, the RS bit should be written back to logic 0 to complete the reset cycle. The ADC will return to the command mode where it waits for a valid command. Also, the RS bit is the only bit in the configuration register that can be set when initiating a reset (i.e. a second write command is needed to set other bits in the Configuration Register after the RS bit has been cleared).

2.3.3 Input Short

The input short bit allows the user to internally ground the inputs of the ADC. This is a useful function because it allows the user to easily test the grounded input performance of the ADC and eliminate the noise effects due to the external system components.

2.3.4 Voltage Reference Select

The voltage reference select (VRS) bit selects the size of the sampling capacitor used to sample the voltage reference. The bit should be set based upon

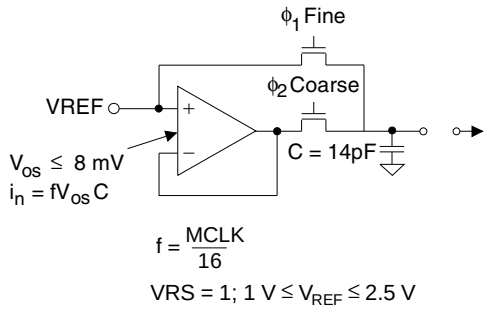


Figure 8. Input Reference Model when VRS = 1

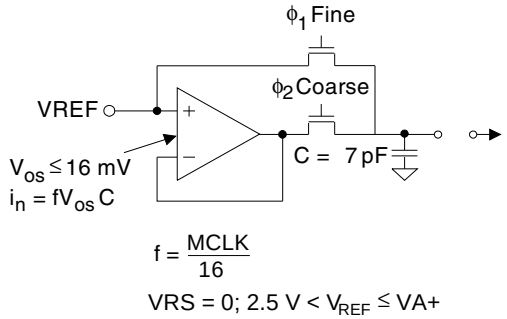


Figure 9. Input Reference Model when VRS = 0

the magnitude of the reference voltage to achieve optimal performance. Figures 8 and 9 model the effects on the reference's input impedance and input current for each VRS setting. As the models show, the reference includes a coarse/fine charge buffer which reduces the dynamic current demand of the external reference.

The reference's input buffer is designed to accommodate rail-to-rail (common-mode plus signal) input voltages. The differential voltage between the VREF+ and VREF- can be any voltage from 1.0 V up to the analog supply (depending on how VRS is configured), however, the VREF+ cannot go above VA+ and the VREF- pin can not go below VA-. Note that the power supplies to the chip should be established before the reference voltage.

2.3.5 Output Latch Pins

The A1-A0 pins of the ADC mimic the D24-D23 bits of the configuration register. A1-A0 can be used to control external multiplexers and other logic functions outside the converter. The A1-A0 outputs can sink or source at least 1 mA, but it is recommended to limit drive currents to less than 20 µA to reduce self-heating of the chip. These outputs are powered from VA+ and VA-. Their output voltage will be limited to the VA+ voltage for a logic 1 and VA- for a logic 0. Note that if the latch bits are used to modify the analog input signal the user should delay performing a conversion until he knows the effects of the A0/A1 bits are fully settled.

2.3.6 Filter Rate Select

The Filter Rate Select bit (FRS) modifies the output word rates of the converter to allow either 50 Hz or 60 Hz rejection when operating from a 4.9152 MHz crystal. If FRS is cleared to logic 0, the word rates and corresponding filter characteristics can be selected using the Configuration Register. Rates can be 7.5, 15, 30, 60, 120, 240, 480, 960, 1920, or 3840 Sps when using a 4.9152 MHz clock. If FRS is set to logic 1, the word rates and corresponding filter characteristics scale by a factor of 5/6, making the selectable word rates 6.25, 12.5, 25, 50, 100, 200, 400, 800, 1600, and 3200 Sps when using a 4.9152 MHz clock. When using other clock frequencies, these selectable word rates will scale linearly with the clock frequency that is used.

2.3.7 Word Rate Select

The Word Rate Select bits (WR3-WR0) allow slection of the output word rate of the converter as depicted in the Configuration Register Descriptions. The word rate chosen by the WR3-WR0 bits is modified by the setting of the FRS bit as presented in the previous paragraph.

2.3.8 Unipolar/Bipolar Select

The UP/$\overline{BP}$ Select bit sets the converter to measure either a unipolar or bipolar input span.

2.3.9 Open Circuit Detect

When the OCD bit is set it activates a current source as a means to test for open thermocouples.

2.3.10 Configuration Register Description

D31(MSB)	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
PSS	PDW	RS	RV	IS	NU	VRS	A1	A0	NU	NU	NU	FRS	NU	NU	NU
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
NU	WR3	WR2	WR1	WR0	UP/$\overline{BP}$	OCD	NU	NU	NU	NU	NU	NU	NU	NU	NU

PSS (Power Save Select)[31]

0 Standby Mode (Oscillator active, allows quick power-up).

1 Sleep Mode (Oscillator inactive).

PDW (Power Down Mode)[30]

0 Normal Mode

1 Activate the power save select mode.

RS (Reset System)[29]

0 Normal Operation.

1 Activate a Reset cycle. See System Reset Sequence in the datasheet text.

RV (Reset Valid)[28]

0 Normal Operation

1 System was reset. This bit is read only. Bit is cleared to logic zero after the configuration register is read.

IS (Input Short)[27]

0 Normal Input

1 All signal input pairs for each channel are disconnected from the pins and shorted internally.

NU (Not Used)[26]

0 Must always be logic 0. Reserved for future upgrades.

VRS (Voltage Reference Select)[25]

0 $2.5\ V < V_{REF} \leq [(VA+) - (VA-)]$

1 $1\ V \leq V_{REF} \leq 2.5V$

A1-A0 (Output Latch bits)[24:23]

The latch bits (A1 and A0) will be set to the logic state of these bits when the Configuration register is written. Note that these logic outputs are powered from VA+ and VA-.

00 A1 = 0, A0 = 0

01 A1 = 0, A0 = 1

10 A1 = 1, A0 = 0

11 A1 = 1, A0 = 1

NU (Not Used)[22:20]

0 Must always be logic 0. Reserved for future upgrades.

Filter Rate Select, FRS[19]

0 Use the default output word rates.

1 Scale all output word rates and their corresponding filter characteristics by a factor of 5/6.

NU (Not Used)[18:15]

0 Must always be logic 0. Reserved for future upgrades.

WR3-WR0 (Word Rate) [14:11]

The listed Word Rates are for continuous conversion mode using a 4.9152 MHz clock. All word rates will scale linearly with the clock frequency used. The very first conversion using continuous conversion mode will last longer, as will conversions done with the single conversion mode. See the section on Performing Conversions and Tables 1 and 2 for more details.

Bit	WR (FRS = 0)	WR (FRS = 1)
0000	120 Sps	100 Sps
0001	60 Sps	50 Sps
0010	30 Sps	25 Sps
0011	15 Sps	12.5 Sps
0100	7.5 Sps	6.25 Sps
1000	3840 Sps	3200 Sps
1001	1920 Sps	1600 Sps
1010	960 Sps	800 Sps
1011	480 Sps	400 Sps
1100	240 Sps	200 Sps

All other combinations are not used.

U/$\overline{B}$ (Unipolar / $\overline{Bipolar}$) [10]

0 Select Bipolar mode.

1 Select Unipolar mode.

OCD (Open Circuit Detect Bit) [9]

When set, this bit activates a 300 nA current source on the input channel (AIN+) selected by the channel select bits. Note that the 300nA current source is rated at 25°C. This feature is particularly useful in thermocouple applications when the user wants to drive a suspected open thermocouple lead to a supply rail.

0 Normal mode.

1 Activate current source.

NU (Not Used) [8:0]

0 Must always be logic 0. Reserved for future upgrades.

2.4 Calibration

Calibration is used to set the zero and gain slope of the ADC's transfer function. The CS5530 provides system calibration.

Note: After the ADC is reset, it is functional and can perform measurements without being calibrated (remember that the VRS bit in the configuration register must be properly configured). If the converter is operated without calibraton, the converter will utilize the initialized values of the on-chip registers (Offset = 0.0; Gain = 1.0) to calculate output words. Any initial offset and gain errors in the internal circuitry of the chip will remain.

2.4.1 Calibration Registers

The CS5530 converter has an offset register that is used to set the zero point of the converter's transfer function. As shown in *Offset Register* section, one LSB in the offset register is 1.835007966 X 2^{-24} proportion of the input span (bipolar span is 2 times the unipolar span, gain register = 1.000...000 decimal). The MSB in the offset register determines if the offset to be trimmed is positive or negative (0 positive, 1 negative). Note that the magnitude of the offset that is trimmed from the input is mapped through the gain register. The converter can typically trim ±100 percent of the input span. As shown in the *Gain Register* section, the gain register spans from 0 to (64 - 2^{-24}). The decimal equivalent meaning of the gain register is

$$D = b_{D29}2^5 + b_{D28}2^4 + b_{D27}2^3 + \ldots + b_{D0}2^{-24}) = \sum_{i=0}^{29} b_{Di}2^{(-24+i)}$$

where the binary numbers have a value of either zero or one (b_{D29} is the binary value of bit D29). While gain register settings of up to 64 - 2^{-24} are available, the gain register should never be set to values above 40.

2.4.2 Gain Register

Decimal Point

MSB	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
NU	NU	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**LSB**
2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{22}	2^{-23}	2^{-24}
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The gain register span is from 0 to (64-2^{-24}). After Reset D24 is 1, all other bits are '0'.

2.4.3 Offset Register

MSB	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Sign	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**LSB**
2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	NU	NU	NU	NU	NU	NU	NU	NU
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

One LSB represents 1.835007966 X 2^{-24} proportion of the input span (bipolar span is 2 times unipolar span).
Offset and data word bits align by MSB. After reset, all bits are '0'.
The offset register is stored as a 32-bit, two's complement number, where the last 8 bits are all 0.

2.4.4 Performing Calibrations

To perform a calibration, the user must send a command byte with its MSB=1, and the appropriate calibration bits (CC2-CC0) set to choose the type of calibration to be performed. The calibration will be performed using the filter rate, and siganl span (unipolar or bipolar) as set in the configuration register. The length of time it takes to do a calibration is slightly less than the amount of time it takes to do a single conversion (see Table 1 for single conversion timing). Offset calibration takes 608 clock cycles less than a single conversion when FRS = 0, and 729 clock cycles less when FRS = 1. Gain calibration takes 128 clock cycles less than a single conversion when FRS = 0, and 153 clock cycles less when FRS = 1.

Once a calibration cycle is complete, SDO falls and the results are automatically stored in either the gain or offset register. SDO will remain low until the next command word is begun. If additional calibrations are performed while referencing the same calibration registers, the last calibration results will replace the effects from the previous calibration. Only one calibration is performed with each command byte.

2.4.5 System Calibration

For the system calibration functions, the user must supply the converter input calibration signals which represent ground and full-scale. When a system offset calibration is performed, a ground referenced signal must be applied to the converter. Figure 10 illustrates system offset calibration.

As shown in Figure 11, the user must input a signal representing the positive full-scale point to perform a system gain calibration. In either case, the calibration signals must be within the specified calibration limits for each specific calibration step (refer to the *System Calibration Specifications*).

2.4.6 Calibration Tips

Calibration steps are performed at the output word rate selected by the WR3-WR0 bits of the configuration register. To minimize the effects of peak-to-peak noise on the accuracy of calibration the converter should be calibrated using the slowest word rate that is acceptable. It is recommended that word rates of 240 Sps and higher not be used for calibration.) To minimize digital noise near the device, the user should wait for each calibration step to be completed before reading or writing to the serial port. Reading the calibration registers and averaging multiple calibrations together can produce a more accurate calibration result. Note that accessing the ADC's serial port before a calibration has finished may result in the loss of synchronization between the microcontroller and the ADC, and may prematurely halt the calibration cycle.

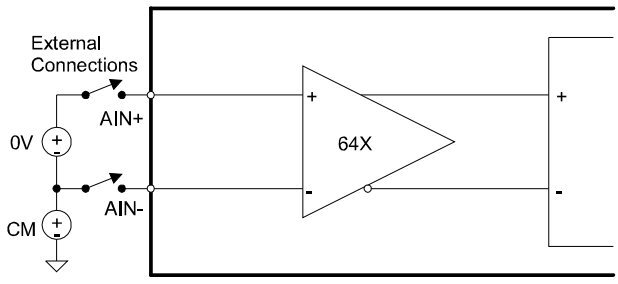


Figure 10. System Calibration of Offset

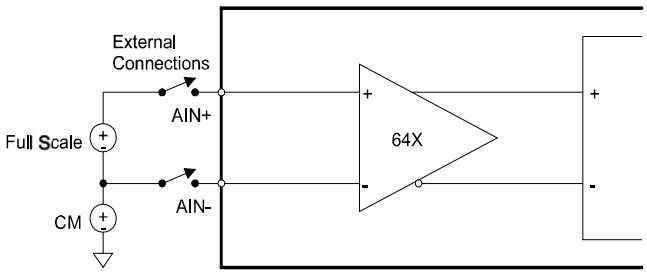


Figure 11. System Calibration of Gain

For maximum accuracy, calibrations should be performed for both offset and gain.

When the device is used without calibration, the uncalibrated gain accuracy is about ±1 percent. Note that the gain from the offset register to the output is 1.83007966 decimal, not 1. If a user wants to adjust the calibration coefficients externally, they will need to divide the information to be written to the offset register by the scale factor of 1.83007966. (This discussion assumes that the gain register is 1.000...000 decimal. The offset register is also multiplied by the gain register before being applied to the output conversion words).

2.4.7 Limitations in Calibration Range

System calibration can be limited by signal headroom in the analog signal path inside the chip as discussed under the *Analog Input* section of this data sheet. For gain calibration, the full-scale input signal can be reduced to 3% of the nominal full-scale value. At this point, the gain register is approximately equal to 33.33 (decimal). While the gain register can hold numbers all the way up to $64 - 2^{-24}$, gain register settings above a decimal value of 40 should not be used. With the converter's intrinsic gain error, this minimum full-scale input signal may be higher or lower. In defining the minimum full-scale Calibration Range (FSCR) under *Analog Characteristics*, margin is retained to accommodate the intrinsic gain error. Inversely, the input full-scale signal can be increased to a point in which the modulator reaches its 1's density limit of 86 percent, which under nominal conditions occurs when the full-scale input signal is 1.1 times the nominal full-scale value. With the chip's intrinsic gain error, this maximum full-scale input signal maybe higher or lower. In defining the maximum FSCR, margin is again incorporated to accommodate the intrinsic gain error.

2.5 Performing Conversions

The CS5530 offers two distinctly different conversion modes. The paragraphs that follow detail the differences in the conversion modes.

2.5.1 Single Conversion Mode

When the user transmits the perform single conversion command, a single, fully settled conversion is performed using the word rate and polarity selections set in the configuration register. Once the command byte is transmitted, the serial port enters data mode where it waits until the conversion is complete. When the conversion data is available, SDO falls to logic 0 to act as a flag to indicate that the data is available. Forty SCLKs are then needed to read the conversion data word. The first 8 SCLKs are used to clear the SDO flag. During the first 8 SCLKs, SDI must be logic 0. The last 32 SCLKs are needed to read the conversion result. Note that the user is forced to read the conversion in single conversion mode as the serial port will remain in data mode until SCLK transitions 40 times. After reading the data, the serial port returns to the command mode, where it waits for a new command to be issued. The single conversion mode will take longer than conversions performed in the continuous conversion mode. The number of clock cycles a single conversion takes for each Output Word Rate (OWR) setting is listed in Table 1. The ± 8 (FRS = 0) or ± 10 (FRS = 1) clock ambiguity is due to internal synchronization between the SCLK input and the oscillator.

Note: In the single conversion mode, more than one conversion is actually performed, but only the final, fully settled result is output to the conversion data register.

Table 1. Conversion Timing for Single Mode

(WR3-WR0)	Clock Cycles	
	FRS = 0	FRS = 1
0000	171448 ± 8	205738 ± 10
0001	335288 ± 8	402346 ± 10
0010	662968 ± 8	795562 ± 10
0011	1318328 ± 8	1581994 ± 10
0100	2629048 ± 8	3154858 ± 10
1000	7592 ± 8	9110 ± 10
1001	17848 ± 8	21418 ± 10
1010	28088 ± 8	33706 ± 10
1011	48568 ± 8	58282 ± 10
1100	89528 ± 8	107434 ± 10

2.5.2 Continuous Conversion Mode

When the user transmits the perform continuous conversion command, the converter begins continuous conversions using the word rate and polarity selections set in the configuration register. Once the command byte is transmitted, the serial port enters data mode where it waits until a conversion is complete. After the conversion is done, SDO falls to logic 0 to act as a flag to indicate that the data is available. Forty SCLKs are then needed to read the conversion. The first 8 SCLKs are used to clear the SDO flag. The last 32 SCLKs are needed to read the conversion result. If '00000000' is provided to SDI during the first 8 SCLKs when the SDO flag is cleared, the converter remains in this conversion mode and continues to convert using the same word rate and polarity information. In continuous conversion mode, not every conversion word needs to be read. The user needs only to read the conversion words required for the application as SDO rises and falls to indicate the availability of new conversion data. Note that if a conversion is not read before the next conversion data becomes available, it will be lost and replaced by the new conversion data. To exit this conversion mode, the user must provide '11111111' to the SDI pin during the first 8 SCLKs after SDO falls. If the user decides to exit, 32 SCLKs are required to clock out the last conversion before the converter returns to command mode. The number of clock cycles a continuous conversion takes for each Output Word Setting is listed in Table 2. The first conversion from the part in continuous conversion mode will be longer than the following conversions due to start-up overhead. The ± 8 (FRS = 0) or ± 10 (FRS = 1) clock ambiguity is due to internal synchronization between the SCLK input and the oscillator.

Note: When changing channels, or after performing calibrations and/or single conversions, the user must ignore the first three (for OWRs less than 3200 Sps, MCLK = 4.9152 MHz) or first five (for OWR ≥ 3200 Sps) conversions in continuous conversion mode, as residual filter coefficients must be flushed from the filter before accurate conversions are performed.

Table 2. Conversion Timing for Continuous Mode

FRS	(WR3-WR0)	Clock Cycles (First Conversion)	Clock Cycles (All Other Conversions)
0	0000	89528 ± 8	40960
0	0001	171448 ± 8	81920
0	0010	335288 ± 8	163840
0	0011	662968 ± 8	327680
0	0100	1318328 ± 8	655360
0	1000	2472 ± 8	1280
0	1001	12728 ± 8	2560
0	1010	17848 ± 8	5120
0	1011	28088 ± 8	10240
0	1100	48568 ± 8	20480
1	0000	107434 ± 10	49152
1	0001	205738 ± 10	98304
1	0010	402346 ± 10	196608
1	0011	795562 ± 10	393216
1	0100	1581994 ± 10	786432
1	1000	2966 ± 10	1536
1	1001	15274 ± 10	3072
1	1010	21418 ± 10	6144
1	1011	33706 ± 10	12288
1	1100	58282 ± 10	24576

2.6 Using Multiple ADCs Synchronously

Some applications require synchronous data outputs from multiple ADCs converting different analog channels. Multiple CS5530 devices can be synchronized in a single system by using the following guidelines:

1) All of the ADCs in the system must be operated from the same oscillator source.

2) All of the ADCs in the system must share common SCLK and SDI lines.

3) A software reset must be performed at the same time for all of the ADCs after system power-up (by selecting all of the ADCs using their respective $\overline{CS}$ pins, and writing the reset sequence to all parts, using SDI and SCLK).

4) A start conversion command must be sent to all of the ADCs in the system at the same time. The ± 8 clock cycles of ambiguity for the first conversion (or for a single conversion) will be the same for all ADCs, provided that they were all reset at the same time.

5) Conversions can be obtained by monitoring SDO on only one ADC, (bring $\overline{CS}$ high for all but one part) and reading the data out of each part individually, before the next conversion data words are ready.

An example of a synchronous system using two CS5530 devices is shown in Figure 12.

2.7 Conversion Output Coding

The CS5530 outputs 24-bit data conversion words. To read a conversion word the user must read the conversion data register. The conversion data register is 32 bits long and outputs the conversions MSB first. The last byte of the conversion data register contains an overflow flag bit. The overrange flag (OF) monitors to determine if a valid conversion was performed.

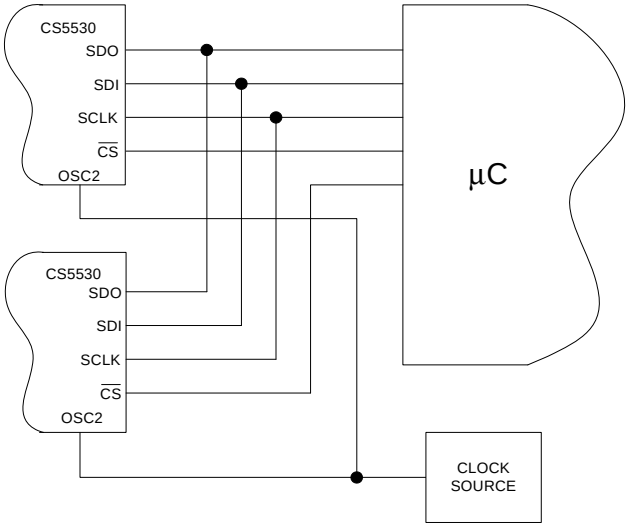


Figure 12. Synchronizing Multiple ADCs

The CS5530 output data conversions in binary format when operating in unipolar mode and in two's complement when operating in bipolar mode. Table 3 shows the code mapping for both unipolar and bipolar modes. VFS in the tables refers to the positive full-scale voltage range of the converter in the specified gain range, and -VFS refers to the negative full-scale voltage range of the converter. The total differential input range (between AIN+ and AIN-) is from 0 to VFS in unipolar mode, and from -VFS to VFS in bipolar mode.

Table 3. Output Coding

Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFFFF	>(VFS-1.5 LSB)	7FFFFF
VFS-1.5 LSB	FFFFFF ------ FFFFFE	VFS-1.5 LSB	7FFFFF ------ 7FFFFE
VFS/2-0.5 LSB	800000 ------ 7FFFFF	-0.5 LSB	000000 ------ FFFFFF
+0.5 LSB	000001 ------ 000000	-VFS+0.5 LSB	800001 ------ 800000
<(+0.5 LSB)	000000	<(-VFS+0.5 LSB)	800000

2.7.1 Conversion Data Output Descriptions

CS5530 (24-BIT CONVERSIONS)

D31(MSB)	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
MSB	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
7	6	5	4	3	2	1	LSB	0	0	0	0	0	OF	0	0

Conversion Data Bits [31:8]

These bits depict the latest output conversion.

OF (Over-range Flag Bit) [2]

0 Bit is clear when over-range condition has not occurred.

1 Bit is set when input signal is more positive than the positive full-scale, more negative than zero (unipolar mode) or when the input is more negative than the negative full-scale (bipolar mode).

Other Bits [7:3], [1:0]

These bits are masked logic zero.

2.8 Digital Filter

The CS5530 has a linear phase digital filter which is programmed to achieve a range of output word rates (OWRs) as stated in the *Configuration Register Description* section. The ADC uses a $Sinc^5$ digital filter to output word rates at 3200 Sps and 3840 Sps (MCLK = 4.9152 MHz). Other output word rates are achieved by using the $Sinc^5$ filter followed by a $Sinc^3$ filter with a programmable decimation rate.Figure 13 shows the magnitude response of the 60 Sps filter, while Figures 14 and 15 show the magnitude and phase response of the filter at 120 Sps. The $Sinc^3$ is active for all output word rates except for the 3200 Sps and 3840 Sps (MCLK = 4.9152 MHz) rate. The Z-transforms of the two filters are shown in Figure 16. For the $Sinc^3$ filter, "D" is the programmable decimation ratio, which is equal to 3840/OWR when FRS = 0 and 3200/OWR when FRS = 1.

The converter's digital filters scale with MCLK. For example, with an output word rate of 120 Sps, the filter's corner frequency is at 31 Hz. If MCLK is increased to 5.0 MHz, the OWR increases by 1.0175 percent and the filter's corner frequency moves to 31.54 Hz. Note that the converter is not specified to run at MCLK clock frequencies greater than 5 MHz.

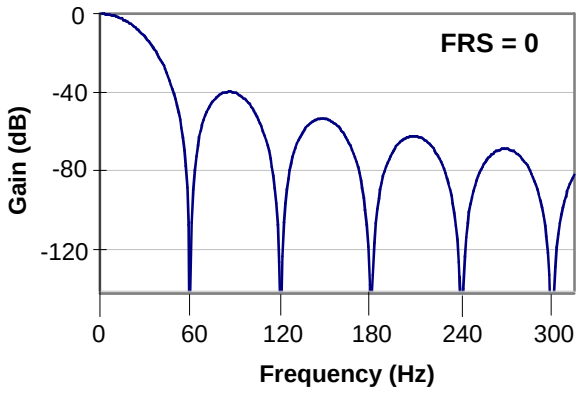


Figure 13. Digital Filter Response (Word Rate = 60 Sps)

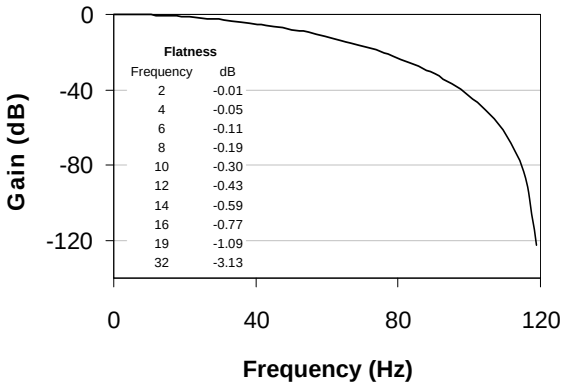


Figure 14. 120 Sps Filter Magnitude Plot to 120 Hz

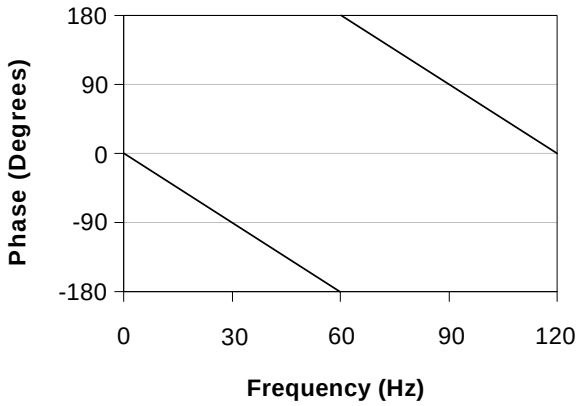


Figure 15. 120 Sps Filter Phase Plot to 120 Hz

$$Sinc^5 = \frac{(1-z^{-80})^5}{(1-z^{-16})^5} \times \frac{(1-z^{-16})^3}{(1-z^{-4})^3} \times \frac{(1-z^{-4})^2}{(1-z^{-2})^2} \times \frac{(1-z^{-2})^3}{(1-z^{-1})^3}$$

$$Sinc^3 = \frac{(1-z^{-D})^3}{(1-z^{-1})^3}$$

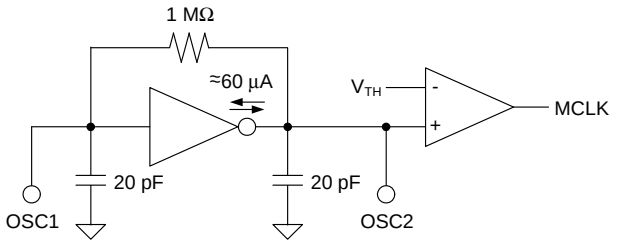
Note: See the text regarding the $Sinc^3$ filter's decimation ratio "D".

Figure 16. Z-Transforms of Digital Filters

2.9 Clock Generator

The CS5530 includes an on-chip inverting amplifier which can be connected with an external crystal to provide the master clock for the chip. Figure 17 illustrates the on-chip oscillator. It includes loading capacitors and a feedback resistor to form a Pierce oscillator configuration. The chips are designed to operate using a 4.9152 MHz crystal; however, other crystals with frequencies between 1 MHz to 5 MHz can be used. One lead of the crystal should be connected to OSC1 and the other to OSC2. Lead lengths should be minimized to reduce stray capacitance. Note that while using the on-chip oscillator, neither OSC1 or OSC2 is capable of directly driving any off chip logic. When the on-chip oscillator is used, the voltage on OSC2 is typically 1/2 V peak-to-peak. This signal is not compatible with external logic unless additional external circuitry is added. The OSC2 output should be used if the on-chip oscillator output is used to drive other circuitry.

The designer can use an external CMOS compatible oscillator to drive OSC2 with a 1 MHz to 5 MHz clock for the ADC. The external clock into OSC2 must overdrive the 60 microampere output of the on-chip amplifier. This will not harm the on-chip circuitry. In this scheme, OSC1 should be left unconnected.



NOTE: 20 pF capacitors are on chip and should not be added externally.

Figure 17. On-chip Oscillator Model

2.10 Power Supply Arrangements

The CS5530 is designed to operate from single or dual analog supplies and a single digital supply. The following power supply connections are possible:

VA+ = +5 V; VA- = 0 V; VD+ = +3 V to +5 V

VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V to +5 V

VA+ = +3 V; VA- = -3 V; VD+ = +3 V

A VA+ supply of +2.5 V, +3.0 V, or +5.0 V should be maintained at ±5% tolerance. A VA- supply of -2.5 V or -3.0 V should be maintained at ±5% tolerance. VD+ can extend from +2.7 V to +5.5 V with the additional restriction that [(VD+) - (VA-) < 7.5 V].

Figure 18 illustrates the CS5530 connected with a single +5.0 V supply to measure differential inputs relative to a common mode of 2.5 V. Figure 19 illustrates the CS5530 connected with ±2.5 V bipolar analog supplies and a +3 V to +5 V digital supply to measure ground referenced bipolar signals. Figures 20 illustrates the CS5532 connected with ±3 V analog supplies and a +3 V digital supply to measure ground referenced bipolar signals.

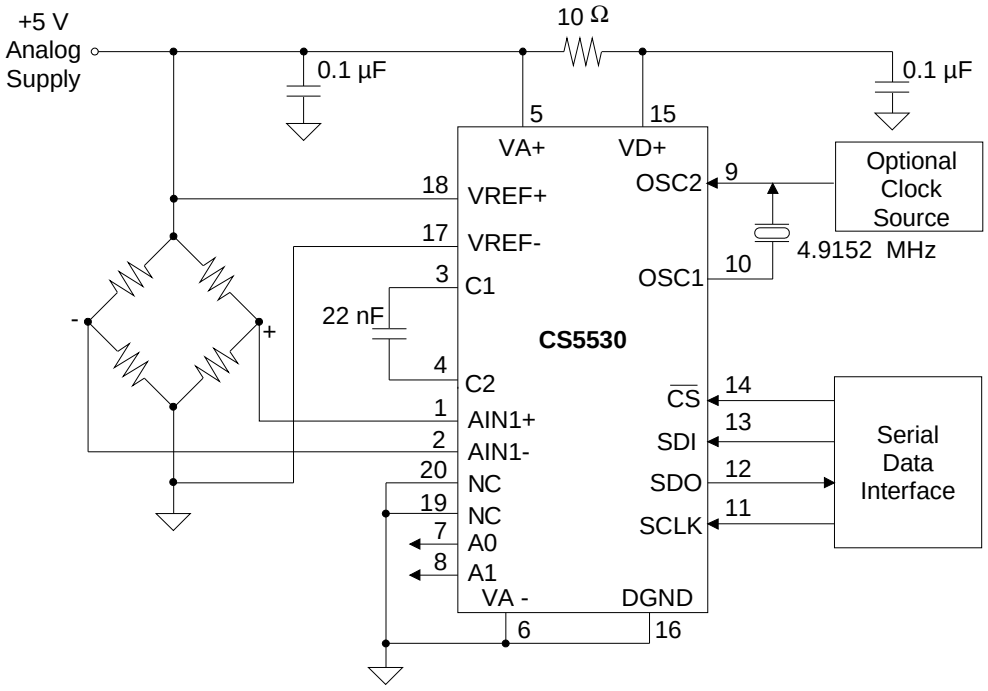


Figure 18. CS5530 Configured with a Single +5 V Supply

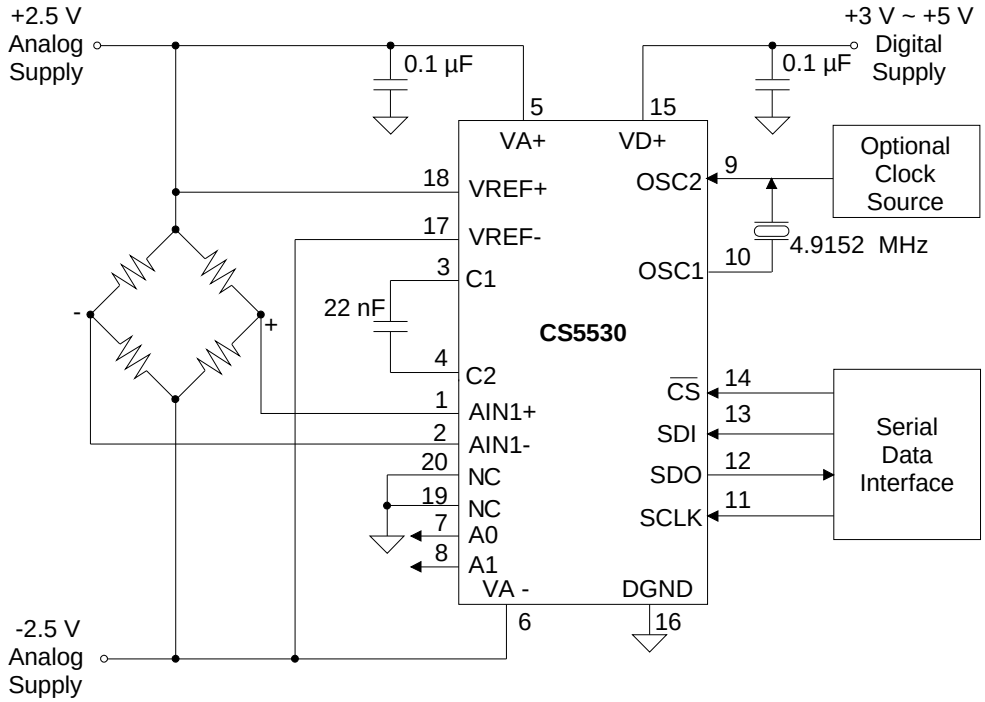


Figure 19. CS5530 Configured with ±2.5 V Analog Supplies

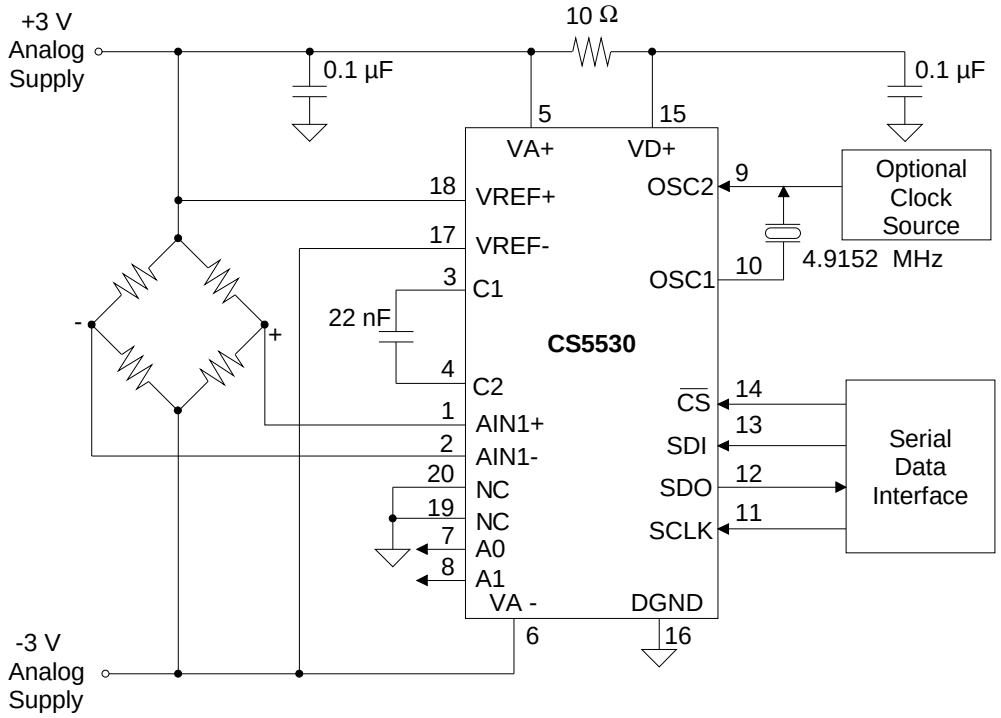


Figure 20. CS5530 Configured with ±3 V Analog Supplies

2.11 Getting Started

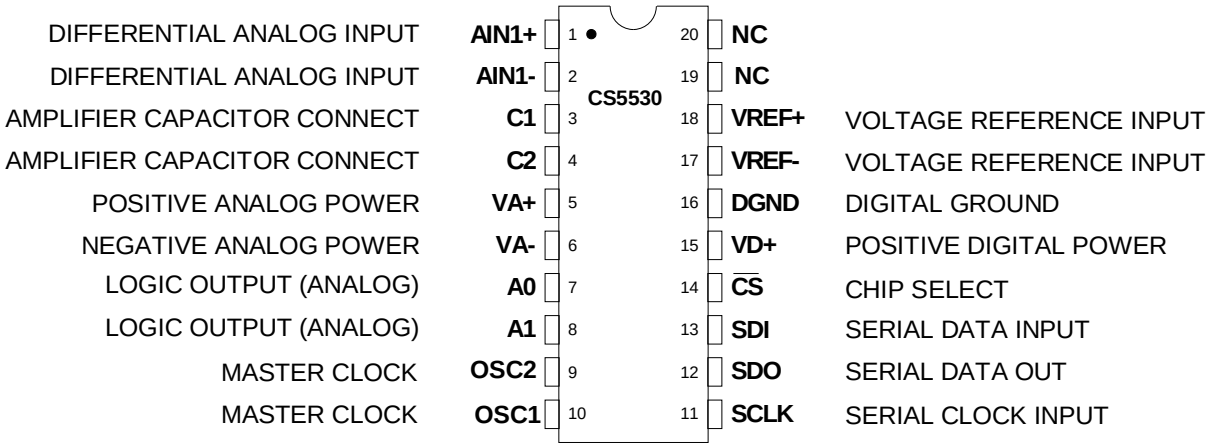
This A/D converter has several features. From a software programmer's prospective, what should be done first? To begin, a 4.9152 MHz or 4.096 MHz crystal takes approximately 20 ms to start. To accommodate for this, it is recommended that a software delay of approximately 20 ms be inserted before the start of the processor's ADC initialization code. Next, since the CS5530 does not provide a power-on-reset function, the user must first initialize the ADC to a known state. This is accomplished by resetting the ADC's serial port with the Serial Port Initialization sequence. This sequence resets the serial port to the command mode and is accomplished by transmitting 15 SYNC1 command bytes (0xFF hexadecimal), followed by one SYNC0 command (0xFE hexadecimal). Once the serial port of the ADC is in the command mode, the user must reset all the internal logic by performing a system reset sequence (see 2.3.2 System Reset Sequence). After the converter is properly reset, the configuration register bits should be configured as appropriate, for example, the voltage reference selection, word rate, signal polarity(unipolar or bipolar) should be configured.

Calibrations or conversions can then be performed as appropriate.

2.12 PCB Layout

For optimal performance, the CS5530 should be placed entirely over an analog ground plane. All grounded pins on the ADC, including the DGND pin, should be connected to the analog ground plane that runs beneath the chip. In a split-plane system, place the analog-digital plane split immediately adjacent to the digital portion of the chip.

3. PIN DESCRIPTIONS



Clock Generator

OSC1; OSC2 – Master Clock

An inverting amplifier inside the chip is connected between these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock (powered relative to VD+) can be supplied into the OSC2 pin to provide the master clock for the device.

Control Pins and Serial Data I/O

$\overline{CS}$ – Chip Select

When active low, the port will recognize SCLK. When high the SDO pin will output a high impedance state. $\overline{CS}$ should be changed when SCLK = 0.

SDI – Serial Data Input

SDI is the input pin of the serial input port. Data will be input at a rate determined by SCLK.

SDO – Serial Data Output

SDO is the serial data output. It will output a high impedance state if $\overline{CS}$ = 1.

SCLK – Serial Clock Input

A clock signal on this pin determines the input/output rate of the data for the SDI/SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.

A0 – Logic Output (Analog), A1 – Logic Output (Analog)

The logic states of A1-A0 mimic the A1-A0 bits in the Configuration Register. Logic Output 0 = VA-, and Logic Output 1 = VA+.

Measurement and Reference Inputs

AIN1+, AIN1- – Differential Analog Input

Differential input pins into the device.

VREF+, VREF- – Voltage Reference Input

Fully differential inputs which establish the voltage reference for the on-chip modulator.

C1, C2 – Amplifier Capacitor Inputs

Connections for the instrumentation amplifier's capacitor.

Power Supply Connections

VA+ – Positive Analog Power

Positive analog supply voltage.

VD+ – Positive Digital Power

Positive digital supply voltage (nominally +3.0 V or +5 V).

VA- – Negative Analog Power

Negative analog supply voltage.

DGND – Digital Ground

Digital Ground.

4. SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two endpoints of the ADC transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

Full-scale Error

The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - 3/2 LSB]. Units are in LSBs.

Unipolar Offset

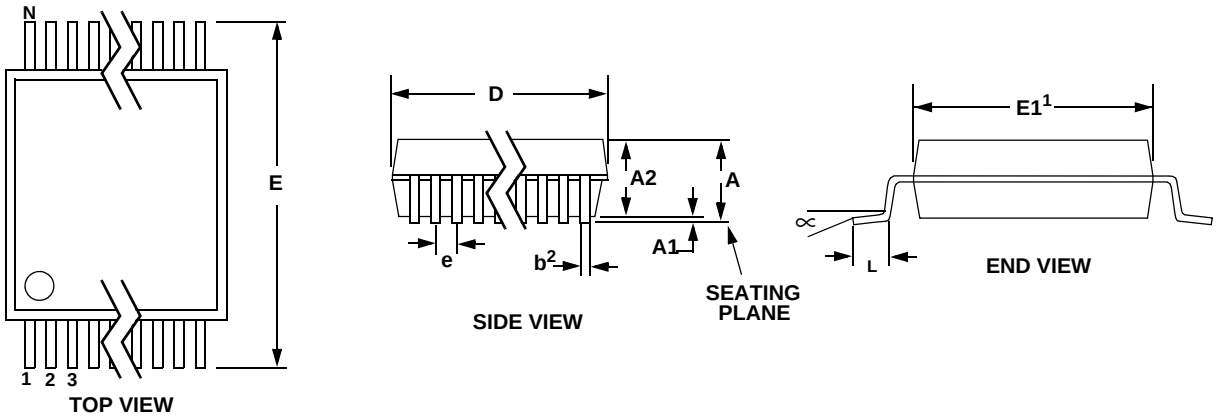
The deviation of the first code transition from the ideal (1/2 LSB above the voltage on the AIN- pin.). When in unipolar mode (U/$\overline{B}$ bit = 1). Units are in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (111...111 to 0$\overline{0}$0...000) from the ideal (1/2 LSB below the voltage on the AIN- pin). When in bipolar mode (U/$\overline{B}$ bit = 0). Units are in LSBs.

5. PACKAGE DRAWINGS

20 PIN SSOP PACKAGE DRAWING



	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	2,3
D	0.272	0.295	6.90	7.50	1
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	1
e	0.024	0.027	0.61	0.69	
L	0.025	0.040	0.63	1.03	
∝	0°	8°	0°	8°	

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

6. ORDERING INFORMATION

Model Number	Bits	Channels	Linearity Error (Max)	Temperature Range	Package
CS5530-IS	24	1	±0.003%	-40°C to +85°C	20-pin 0.2" Plastic SSOP
CS5530-ISZ	24	1	±0.003%	-40°C to +85°C	20-pin 0.2" Plastic SSOP, Lead Free

7. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating	Max Floor Life
CS5530-IS	240 °C	2	365 Days
CS5530-ISZ	260 °C	3	7 Days

Revision History

REVISION	DATE	CHANGES
A1	OCT 2006	Advance Release
A2	NOV 2006	Updated power consumption values.
A3	NOV 2006	Updated noise density plot.
A4	NOV 2006	Updated temperature range specification.
F1	JAN 2007	Corrected input current on p1 to 1200 pA. Changed temp range to -40 to +85.
F2	MAY 2009	Increased input current noise spec. to 1.0 pA / $\sqrt{Hz}$.
F3	NOV 2009	Minor correction to Figure 4. Input Model for AIN+ and AIN- Pins (page 11).

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com