A DIVISION OF CIRRUS LOGIC

CS5542
CS5543

22-Bit, Multi-Channel ΔΣ ADC Chip Set

Features

- Delta-Sigma Architecture:
  - 5th Order Modulator
  - 22-Bit Resolution
- dc Accuracy (f_{BW} = 250Hz):
  - Integral Linearity: ±0.001 % F.S.
  - Differential Linearity: ±0.5 LSBs
  - RMS Noise: 1.1 pA_{RMS}
- Pin Selectable Input Range:
  - ±400 nA to ±2.5 µA Full Scale
- 8-Channel Digital FIR Filter
- Self-calibration of Offset and Gain
- Low Power: 50 mW /ch for 8-ch system

Description

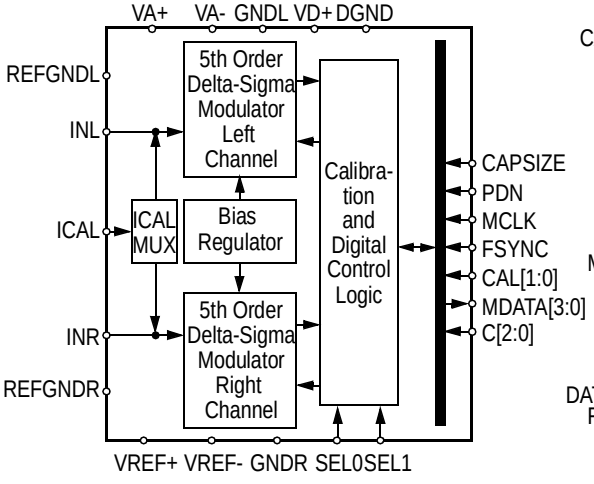
The CS5542 / CS5543 chip set is designed to be a complete current measurement data acquisition system. The CS5542 is a 22-Bit, 2-channel, 5th-order delta sigma modulator. The CS5543 is a monolithic CMOS, 8-channel digital FIR filter designed to be used with up to four CS5542's forming an 8-channel system. The complete system is capable of cascading up to 1024 channels.

The system supports 22-bit measurement resolution with output conversion rates up to 1 kHz per channel. JTAG boundary-scan capability is available to facilitate self-test at the system level.

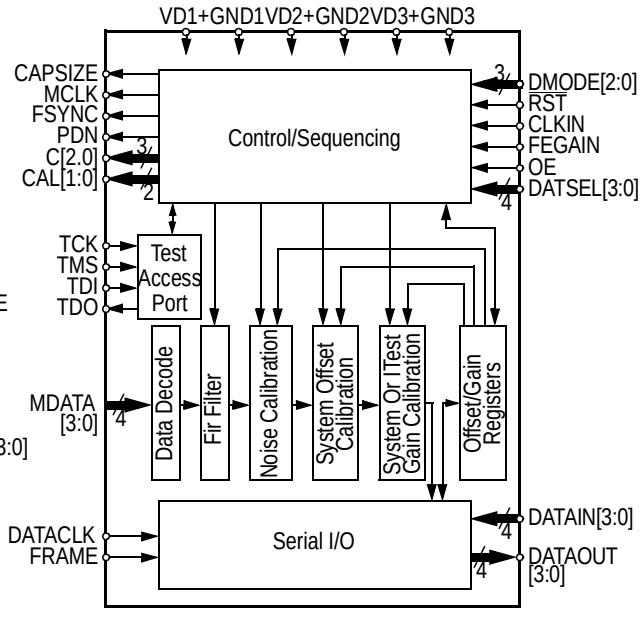
Potential applications for the CS5542/CS5543 system are environmental monitoring, process control systems, color sensing, light measurement, chemical analyzers and photo-diode transducer applications.

ORDERING INFORMATION

CS5542-KL	0 to 70°C	28-pin PLCC
CS5543-KL	0 to 70°C	28-pin PLCC



CS5542



CS5543

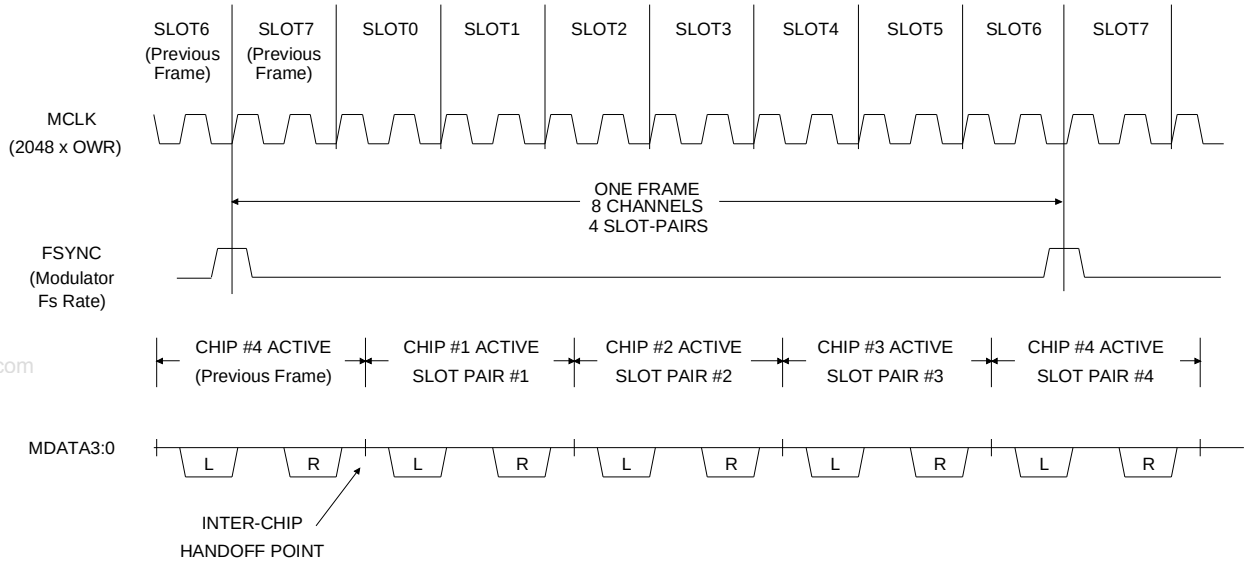
Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Cirrus Logic, Inc.
Crystal Semiconductor Products Division
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

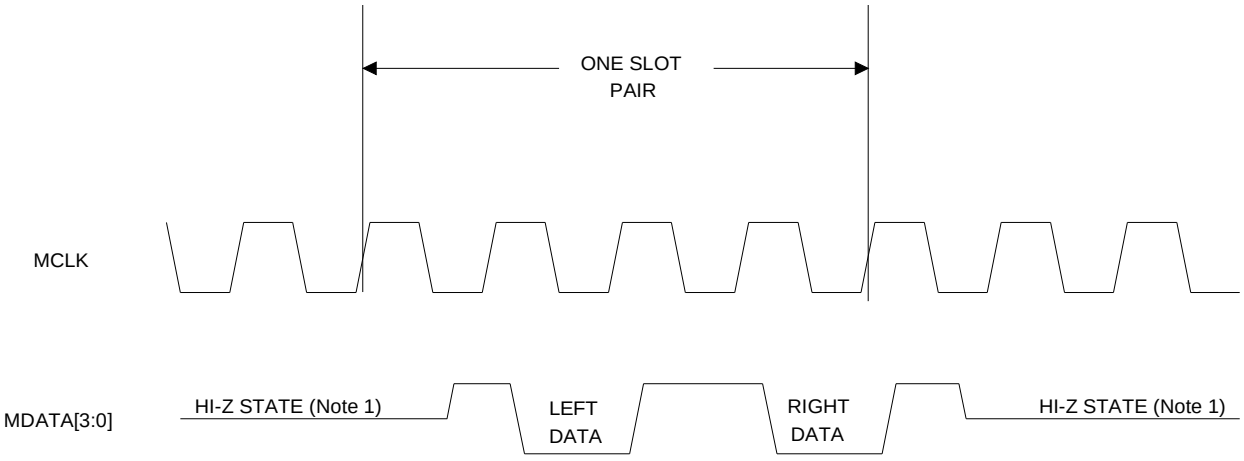
ANALOG CHARACTERISTICS: (T_A = 25° C; VA+, VD+ = 5 V ±5%; VA- = -5 V ±5%; GNDL,GNDR, & DGND= 0V;VREF+ = 4V, VREF- = -4 V; MCLK frequency as noted.)

Parameter			Min	Typ	Max	Units
Specified Temperature Range			0	-	70	°C
Accuracy						
Full Scale Input Current (Bipolar)						
	CAPSIZE=0	(Note 1)	-	400	-	nA
	CAPSIZE=1	(Note 1)	-	2500	-	nA
Dynamic Range						
	CAPSIZE=0	(Note 1)	106	109	-	dB
	CAPSIZE=1	(Note 1)	113	116	-	dB
Differential Nonlinearity	(No Missing Codes)	(Note 2)	22	-	-	Bits
Integral Nonlinearity		(Note 1)	-	-	0.001	%FS
Full Scale Error		(Note 3)	-	-	0.1	%FS
Full Scale Drift		(Note 3)	-	30	-	ppm/°C
System Offset Calibration Range		(Note 4)	-	-	10	%FS
Offset Drift		(Note 1)	-	±0.3	-	LSB/°C
Power Supplies		(Note 5)				
Consumption						
	Active		-	-	80	mW
	Powerdown		-	-	10	mW
50, 60 Hz Power Supply Rejection: VA+ or VA-		(Notes 1, 6)	-	TBD	-	dB
Fullscale Current = 400 nA						
	60 Hz		-	1.85	-	nA/V
	500 Hz		-	13.5	-	nA/V
Fullscale Current = 2500 nA						
	60 Hz		-	1.88	-	nA/V
	500 Hz		-	15.3	-	nA/V

Notes:
1. Full scale current is tested under two conditions: CAPSIZE = 0 (CDAC = 1.6 pF) with MCLK at 1.024 MHz and CAPSIZE = 1 (CDAC = 4.8 pF) with MCLK at 2.048 MHz. Dynamic Range (Signal-to-Noise) is tested with 101 Hz sine wave voltage driven into a 5 MΩ input resistor with a 470 pF capacitor connected from INR or INL to REFGNDR or REFGNDL respectively, to test each modulator. S/N and integral nonlinearity are tested with CAPSIZE = 0 (CDAC = 1.6 pF) with MCLK at 2.048 MHz and CAPSIZE = 1 (CDAC = 4.8 pF) with MCLK at 1.024 MHz.
2. Guaranteed by design or characterization.
3. Specification applies after a complete calibration sequence using the CS5542/CS5543 combination. Drift specification is for the CS5542/CS5543 only and does not include drift due to the input components, the VREF voltage, or a frequency change of CLKIN.
4. Specification applies only to System Offset Calibration using the CS5542/CS5543 chip combination after Input Offset Voltage calibration has been completed with no external offset applied to the input.
5. The VA+ and VA- supplies should be quiet supplies (see data sheet text). Power supply sequence is important. The VA+ and VA- supplies should be applied to the CS5542 prior to or at the same time as the VD+ supply.
6. Power supply rejection is tested with a 100 mVp-p sine wave applied to each supply. See data sheet text for power supply noise requirements.



CS5542 Frame Timing Overview



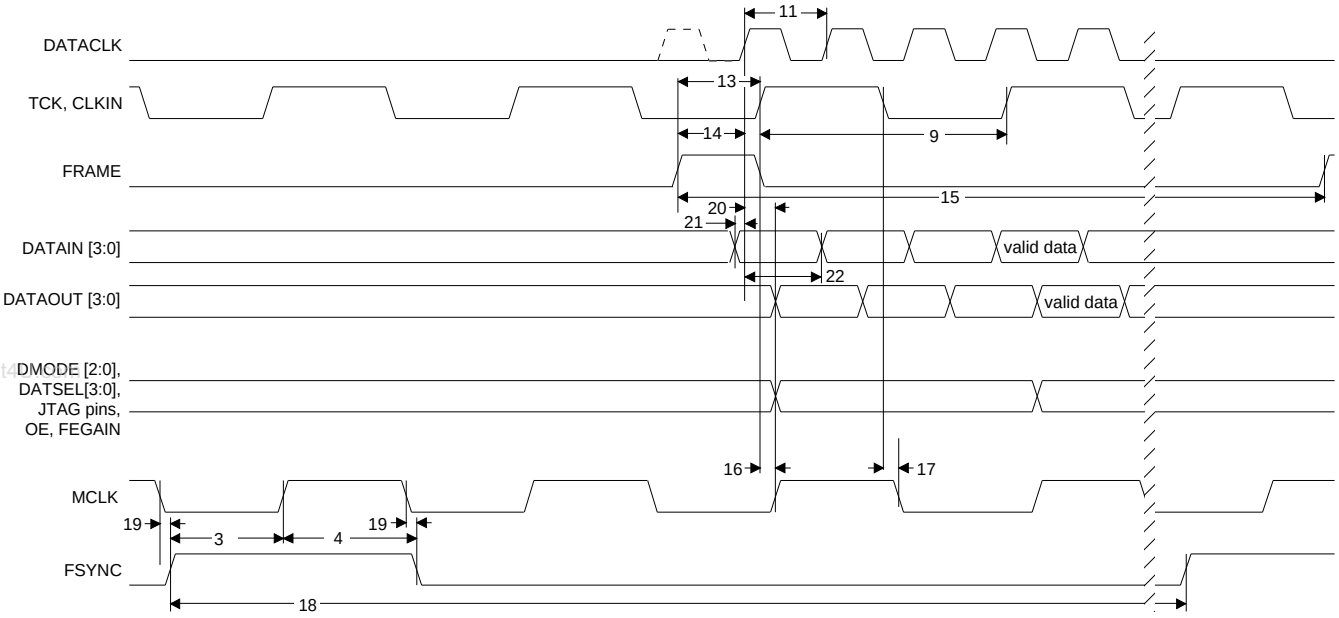
Notes

1 Hi-Z State shown as intermediate level for clarity only. Bus capacitance would normally maintain valid logic one level during Hi-Z until next time slot pair becomes active.

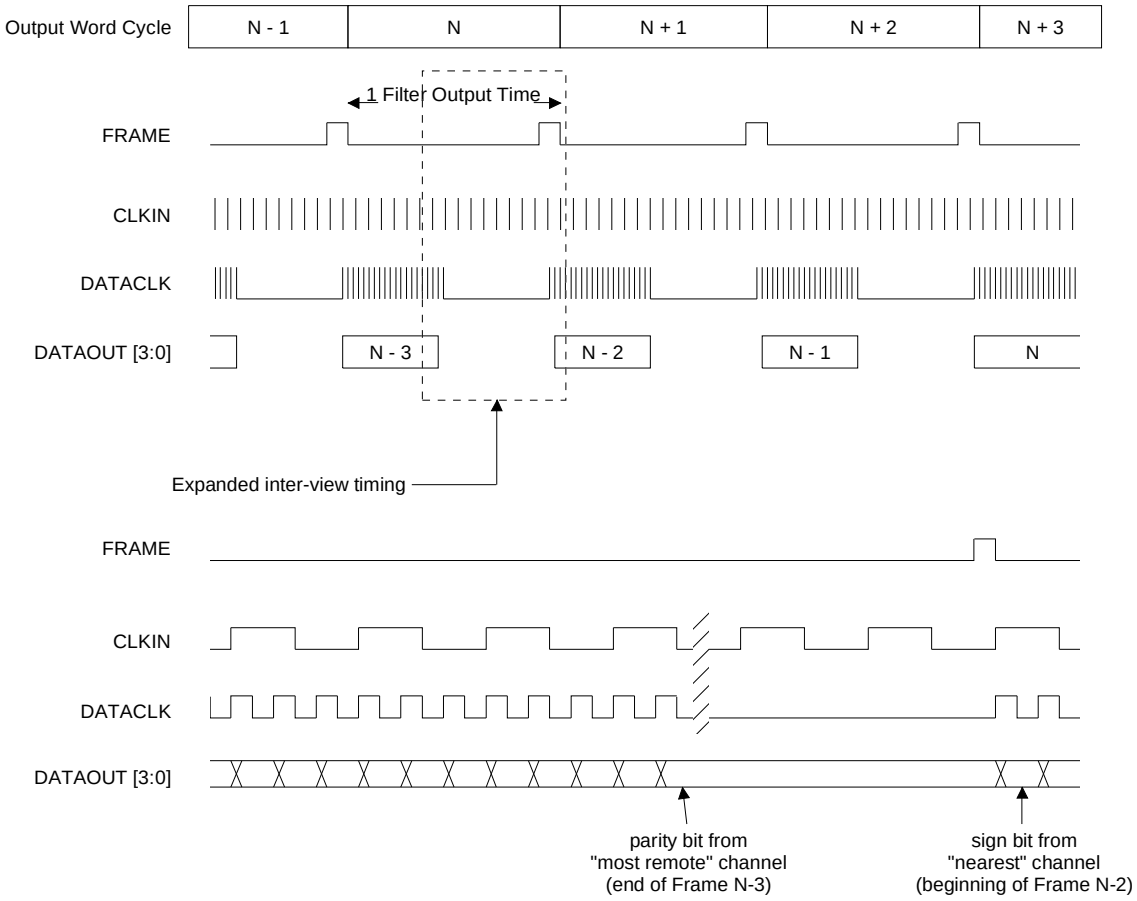
CS5542 MDATA3-MDATA0 Output Timing Characteristics

CS5542 / CS5543 SYSTEM SWITCHING CHARACTERISTICS: (T_A= 25°C, VD1+ = VD2+ = VD3+ = 5 V ±5%; GND1 = GND2 = GND3 = 0 V; For timing parameters: CLKIN= 2.048 MHz; DATACLK = 6.144 MHz; MCLK = 2.048 MHz; Outputs loaded with 50 pF.)

Parameter	Number	Min	Typ	Max	Units
CS5542 Modulator Timing					
MCLK Frequency	0	1.024	-	2.048	MHz
MCLK Duty Cycle	1	40	-	60	%
FSYNC Frequency	2	-	MCLK/ 16	-	Hz
FSYNC set-up before MCLK rising edge	3	70	-	-	ns
FSYNC hold time after MCLK rising edge	4	70	-	-	ns
MCLK rising to MDATA[3:0] valid	5			70	ns
MCLK rising to MDATA[3:0] high	6			70	ns
MCLK falling to MDATA[3:0] to Hi-Z	7			70	ns
MCLK falling to MDATA[3:0] active	8			70	ns
CS5543 System Timing					
CLKIN Frequency (1/Clock Period)	9	1.024	-	2.048	MHz
CLKIN Duty Cycle	10	40	-	60	%
DATACLK Frequency (1/Clock Period)	11	3.072	-	6.144	MHz
DATACLK Duty Cycle	12	40	-	60	%
FRAME rising to CLKIN rising	13	20			ns
FRAME rising to next DATACLK rising	14	20			ns
FRAME period	15		1		ms
CLKIN rising to MCLK rising	16	0		50	ns
CLKIN falling to MCLK falling	17	0		50	ns
CS5542 /CS5543 Interface					
FSYNC period	18	-	7.81	-	µs
MCLK falling to FSYNC rising or falling	19	0		70	ns
CS5543 to CS5543 Interface					
DATACLK rising to DATAOUT valid	20			65	ns
DATAIN set-up time before DATACLK rising	21	0		15	ns
DATAIN hold time after DATACLK rising	22	15		15	ns



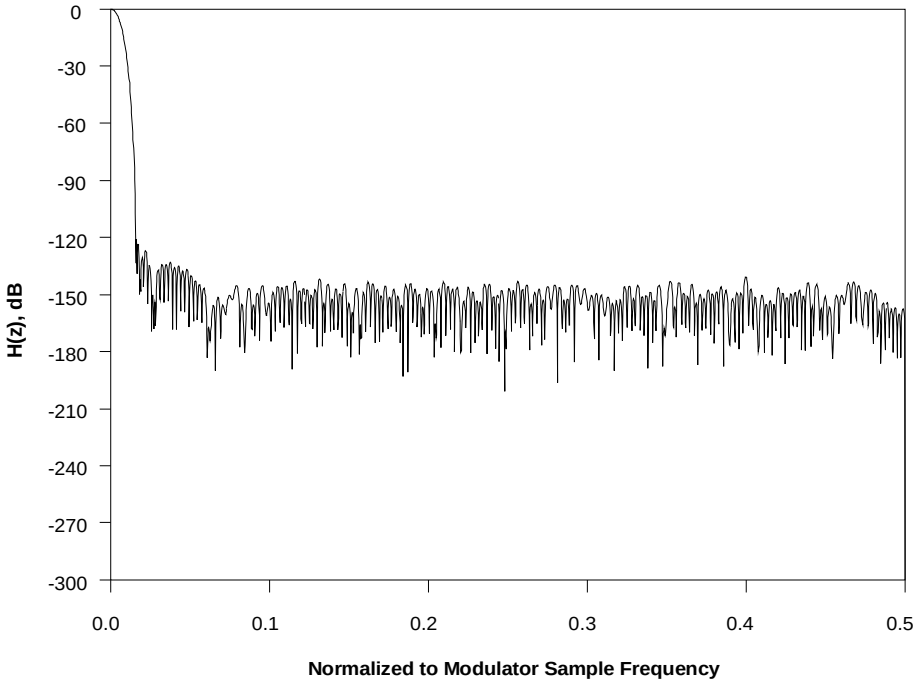
CS5542/CS5543 System Timing Diagram



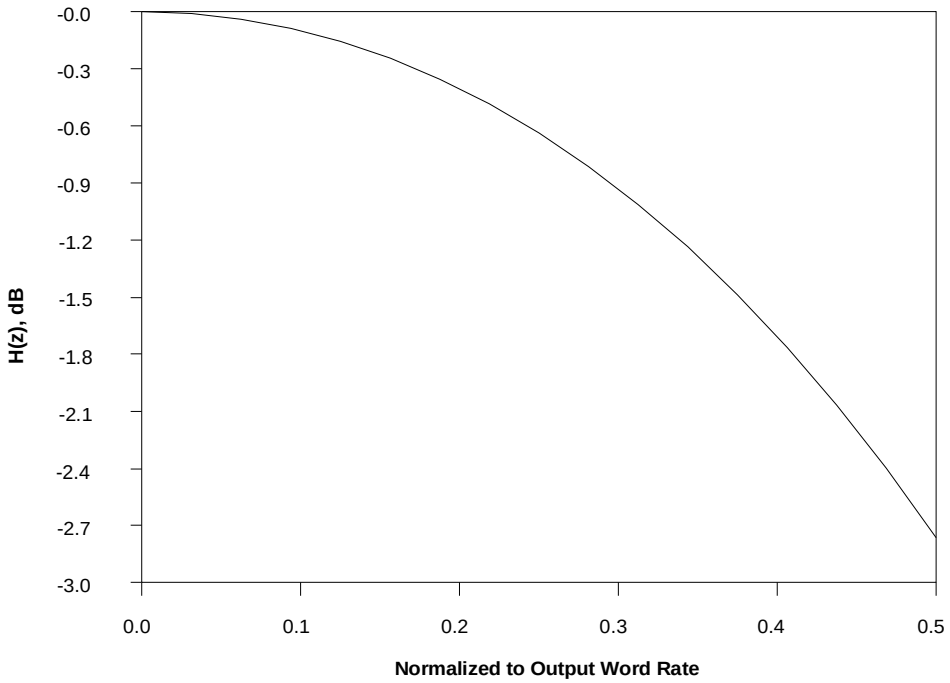
Multi-Frame System Timing Diagram

CS5543 FILTER CHARACTERISTICS: (T_A= 25°C, VD1+ = VD2+ = VD3+ = 5 V ±5%; GND1 = GND2 = GND3 = 0 V; Output Word Rate (OWR) = CLKIN/2048)

Parameter		Min	Typ	Max	Units
Passband		-	-	0.5	OWR
-3 dB Frequency		-	0.536	-	OWR
Equivalent Noise Bandwidth			0.536		OWR
Stop Band		0.016		0.5	128 X OWR
Stop Band Rejection	(CS5543 only)	120			dB
Stop Band Rejection	(CS5542/43 Combination)	127			dB
Group Delay			3/OWR		s
Group Delay vs. Frequency	(Linear Phase)			0	s
Decimation Ratio	(CS5543 input to output)		128		



Modulator Sample Frequency = MCLK/16; Output Word Rate = MCLK/2048 Hz
Digital Filter Total Response



CS5543 Digital Filter Passband Response

CS5542 DIGITAL CHARACTERISTICS: (T_A = 25°C, VD+ = 5 V ±5%; DGND = 0V; Output loaded with 50 pF)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{ih}	VD+ -1.0	-	-	V
Low-Level Input Voltage	V_{il}	-	-	1	V
High-Level Output Voltage (I_{out} = 600µA)	V_{oh}	VD+ -0.4	-	-	V
Low-Level Output Voltage (I_{out} = 800µA)	V_{ol}	-	-	0.4	V
Input Leakage Current (All pins except OE = Logic 0)	I_{in}	-	-	10	µA
Input Leakage Current (OE pin only, OE pin = Logic 0)	I_{in}	-	-	25	µA
Output Leakage Current	I_{out}	-	-	10	µA
Digital Input Capacitance	C_{in}	-	7	-	pF
Digital Output Capacitance	C_{out}	-	7	-	pF

CS5542 RECOMMENDED OPERATING CONDITIONS: (GNDR = GNDL = REFGNDR = REFGNDL = DGND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Operating Voltages					
Positive Analog	VA+	4.75	5.0	+5.25	V
Negative Analog	VA-	-4.75	-5.0	-5.25	V
Positive Digital	VD+	4.75	5.0	+5.25	V
VREF+	VREF+	2.0	4.0	4.1	V
VREF-	VREF-	-2.0	-4.0	-4.1	V

CS5542 ABSOLUTE MAXIMUM RATINGS*: (Voltages with respect to GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Source Transient Voltage into INL and INR inputs (Note 7)		-	-	1000	V
Source Transient Current into INL and INR inputs		-	-	100	mA
Operating Voltages					
Positive Analog	VA+	-0.3	-	6.0	V
Negative Analog	VA-	+0.3	-	-6.0	V
Positive Digital	VD+	0.3	-	(VA+)+0.3	V
Input Current, Any Pin Except Supplies	I_{in}	-	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	-	(VD+)+0.3	V
Storage Temperature	T_{stg}	-65		150	°C

Notes: 7. Transient model is 100 pF through a 1500 ohm source resistance.

*Warning: Operation beyond these limits may result in permanent damage to the device
Normal operations not guaranteed at these extremes

CS5543 POWER SUPPLY: (T_A = 25°C; CLKIN = 2.048 MHz; DATACLK = 6.144 MHz, VD+ = 5.25 V; GND1 = GND2 = GND3 = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Consumption					
Active			75	95	mW
Powerdown			-	1700	uW

CS5543 DIGITAL CHARACTERISTICS: (T_A = 25°C, V_D+ = 5 V ±5%; GND1 = GND2 = GND3 = 0V; Output loaded with 50 pF)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{ih}	VD+-1.0	-	-	V
Low-Level Input Voltage	V_{il}	-	-	1	V
High-Level Output Voltage (I_{out} = -600µA)	V_{oh}	VD+-0.4	-	-	V
Low-Level Output Voltage (I_{out} = 800µA)	V_{ol}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	µA
Output Leakage Current	I_{out}	-	-	10	µA
Digital Input Capacitance	C_{in}	-	7	-	pF
Digital Output Capacitance	C_{out}	-	7	-	pF

CS5543 RECOMMENDED OPERATING CONDITIONS: (GND1 = GND2 = GND3 = 0V, All voltages with respect to 0V.)

Parameter	Symbol	Min	Typ	Max	Units
Digital DC Supply	VD+	4.75	5.0	5.25	V
Supply Voltage Required to Maintain Calibration Information		4.0	-	-	V

CS5543 ABSOLUTE MAXIMUM RATINGS*: (GND = 0V, All voltages with respect to 0V.)

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies:	VD1+ VD2+ VD3+	-0.3		6.0	V
Input Current (Except Supply Pins)	I_{in}			±10.0	mA
Digital Input Voltage	V_{inp}	-0.3		(VD+)+0.3	V
Storage Temperature	T_{stg}	-65		150	°C

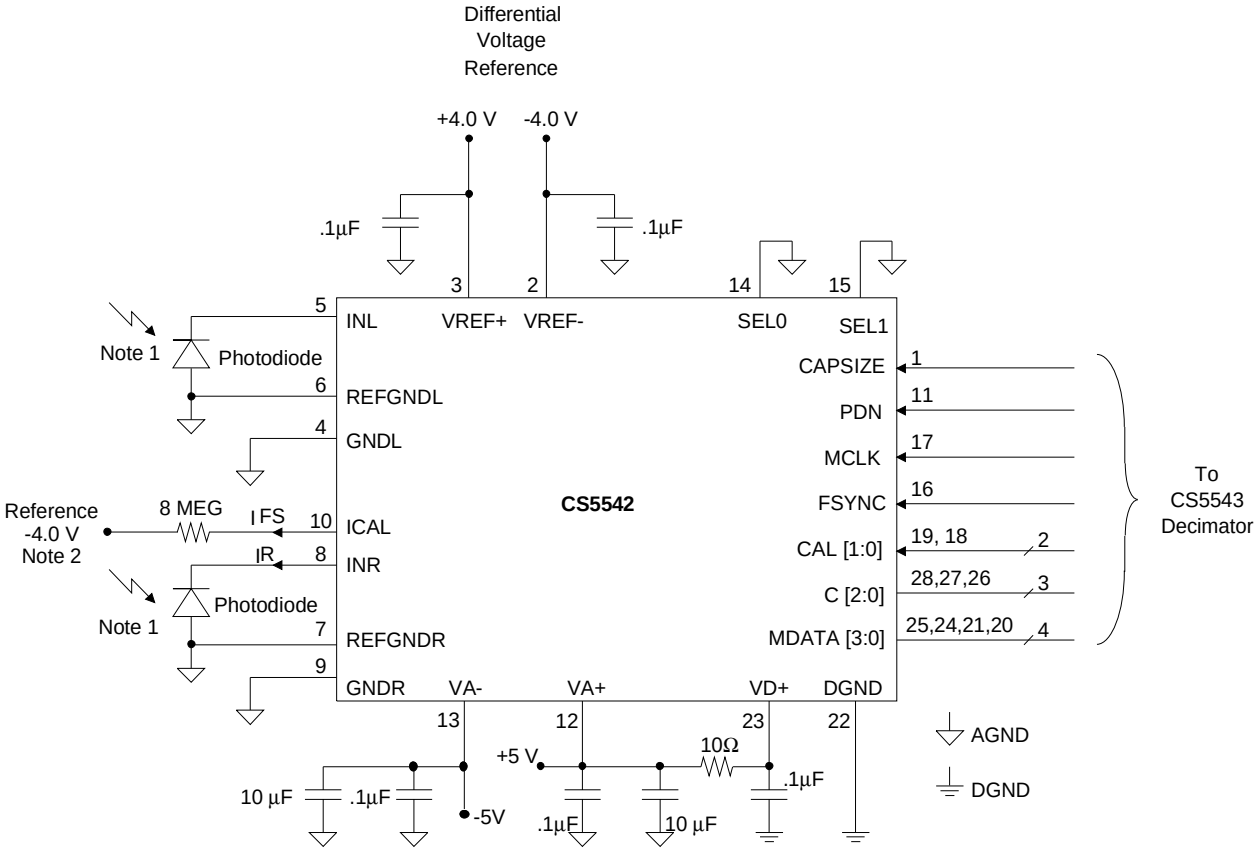
*Warning: Operation beyond these limits may result in permanent damage to the device
Normal operations not guaranteed at these extremes

GENERAL DESCRIPTION

The CS5542 is a monolithic CMOS dual delta-sigma modulator. Each modulator in the CS5542 accepts a low level current input, usually supplied by a photodiode (see Figure 1). This current is digitized by the CS5542 modulator and filtered by the CS5543 digital FIR decimation filter. Four CS5542 modulator chips can be combined with one CS5543 filter chip to provide eight channels of data conversion as shown in Figure 2. Up to 128 8-channel blocks of CS5542/CS5543 chip sets can be connected to build a 1024 channel system as shown in Figure 3. The CS5542/CS5543 combination supports several calibration modes for the data acquisition system.

THEORY OF OPERATION

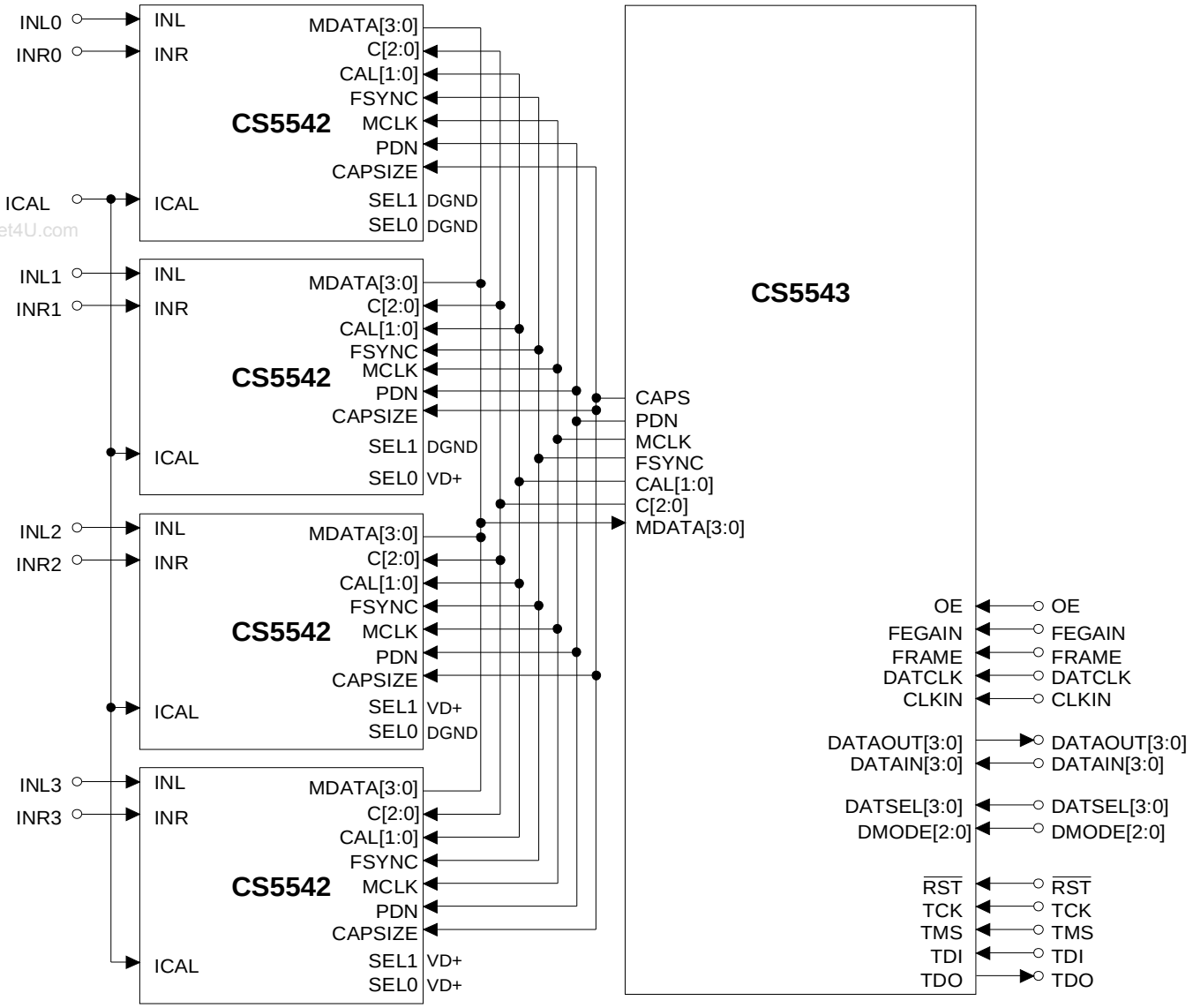
The CS5542/CS5543 chip set is designed to construct multi-channel current input digitizer systems. The conversion clock input (CLKIN) into the CS5543 provides the master clock for the digital filter. This clock can be as fast as 2.048 MHz. CLKIN is buffered inside the CS5543 and is passed to each of the CS5542 modulator chips as the MCLK (modulator clock) signal. The CS5542/CS5543 combination provides output conversion data at a word rate equal to CLKIN/2048.



Note 1: Diodes can be connected with either polarity. As shown the CS5542/43 will generate a more negative code as the photodiode outputs more current.

2: The ICAL current can be of either polarity. Its magnitude will determine the full scale measurement range.

Figure 1. CS5542 Typical Connection Diagram



Supplies omitted for clarity

Figure 2. Typical 8-channel Connection Diagram

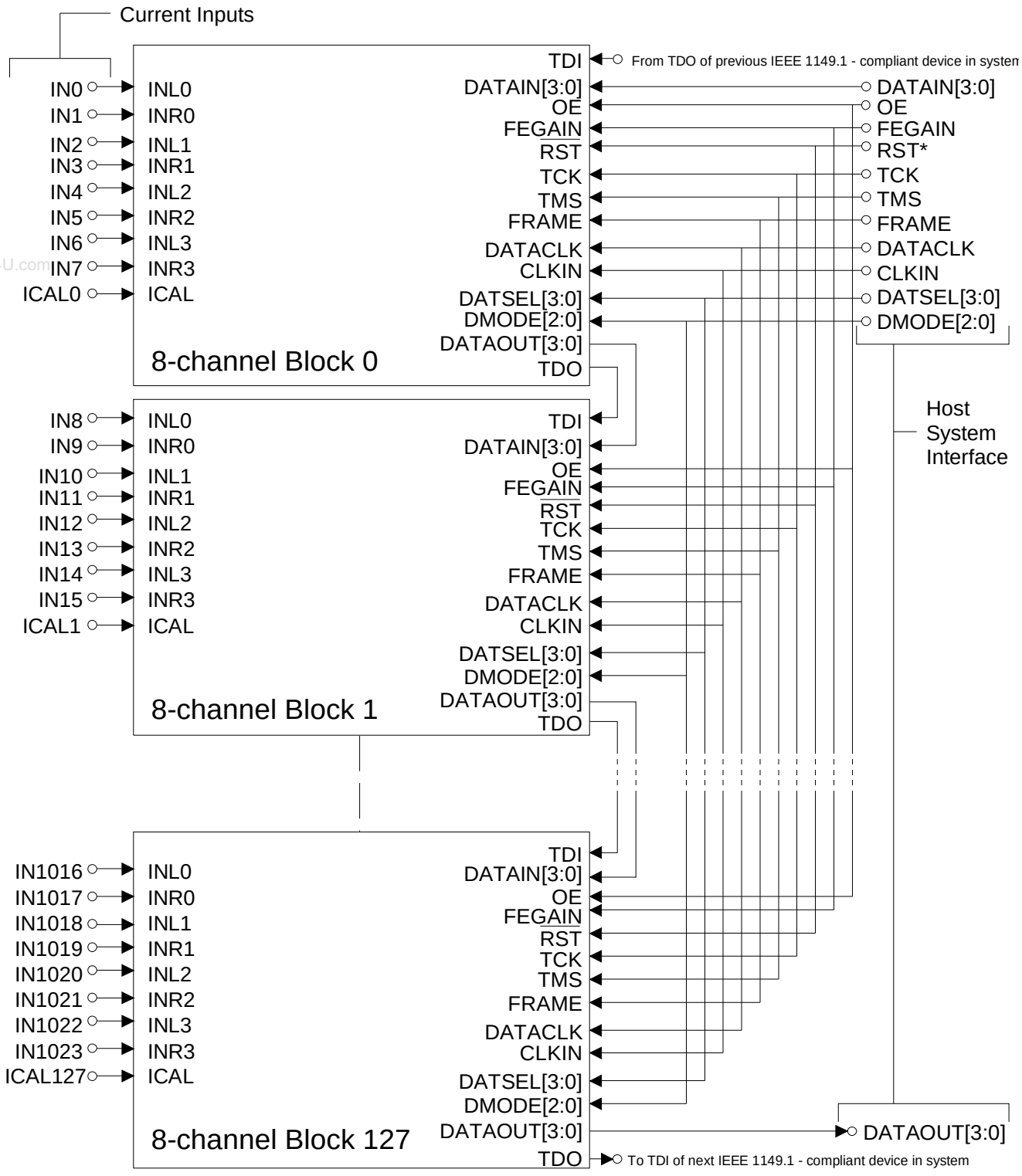


Figure 3. Typical 1024 Connection Diagram

The CS5542 includes two modulators. The input current into each of the modulators is set by the following factors: the MCLK (modulator clock) frequency, the value of the VREF voltage to modulator chip, and the logic value of the CAPSIZE input to the CS5542 modulator (this selects either a 1.6 pF or a 4.8 pF transimpedance feedback capacitor). MCLK is typically set as some frequency between 1.024 MHz and 2.048 MHz. The VREF voltage is optimally set to 4.0 Volts. The voltage reference for the modulator is actually input into both the VREF+ and VREF- pins as +4.0 and -4.0 volts.

The full scale input current is defined by the following equation:

$(V_{REF})\ X\ (C_{DAC})\ X\ (MCLK/16) = I_{FS}$

With VREF = 4.0, MCLK = 2.048 MHz, and CDAC set to select 1.6 pF, the nominal full scale current will be set at 819 nA. The value of the offset and gain register contents will affect the actual conversion words which are output from the converter with a specific input current. Several calibration steps (to be discussed later) are necessary to ensure that the chip converts accurately.

The CS5542 dual modulator and CS5543 multichannel filter are designed to interface together. The CS5542 modulator uses a tri-level modulator. The modulator thresholds must be calibrated before accurate measurements can be accomplished. The threshold values are measured and digitally corrected inside the CS5543 digital filter. The CS5543 digital filter functions as a digital calibration engine and a communications interface in addition to being an FIR filter.

The CS5543 digital filter collects the multi-bit quantized data from four dual modulator CS5542s and computes offset and gain corrections to the data, yielding a 24-bit output word. The 24-bit output data word includes an overflow bit, a parity bit, and 22 data bits (21 bits plus sign).

There are several clocks which control the timing to the multi-channel system. CLKIN (Master Clock) is the primary clock to the system. CLKIN (typically 2.048 MHz) is input to the CS5543 filter. Inside the filter CLKIN is buffered and passed to the CS5542s as MCLK. For each two clock cycles of MCLK to the modulator, a four bit modulator sample is passed to the CS5543 digital filter. The digital filter computes an output conversion word for each set of 1024 modulator samples. The output word rate of the filter is therefore related to the CLKIN or MCLK frequency by the ratio CLKIN/2048 = OWR (output word rate). The conversion data for eight CS5542 modulator channels is output from the four CS5543 DATAOUT pins in a serial-formatted, time-multiplexed fashion. The DATACLK controls the rate at which data is output from the DATAOUT pins. DATACLK is three times the frequency of CLKIN.

The CS5542/CS5543 chip set is designed to support constructing a serially-connected current digitization system with up to 1024 channels.

System Initialization and Calibration

After power is applied to the CS5542/CS5543 system, a reset must be issued to the CS5543 device by taking the $\overline{RST}$ pin low. This resets the gain register to 0.8 (199998(H)) and all other registers to 0.0. After $\overline{RST}$ is returned high, the release of the $\overline{RST}$ state is not recognized until the next rising edge of the FRAME signal.

After a reset is recognized, the CS5542/CS5543 system must complete a full set of calibration steps before being used for measurement. Calibrations are performed by controlling the states of the DTEST (Digital Test Mode Select) pins with the DATSEL (Data Select Mode) pins held as logic 0s. Tables 1 and 2 illustrate the commands available via the DTEST and DATSEL

DATSEL[3:0]	DTEST[2:0]	FUNCTION
0 0 0 0	0 0 0	Normal Operation
0 0 0 0	0 0 1	Input Offset Voltage Cal
0 0 0 0	0 1 0	Noise Cal
0 0 0 0	0 1 1	System Offset Cal
0 0 0 0	1 0 0	Full-Scale Gain Cal (Uses ICAL input)
0 0 0 0	1 0 1	Full-Scale Gain Cal (Uses INL(INR) input)
0 0 0 0	1 1 0	Decimator and Modulator Power-Down
0 0 0 0	1 1 1	Modular Power Down

Table 1. Operation Modes

DTEST[2:0]	DATSEL[3:0]	FUNCTION	DATA TYPE
0 0 0	0 0 0 0	Normal Operation	(SIGN, MSB first)
0 0 0	0 0 0 1	Tri-State Dataout [3:0] Pins	(- - -)
0 0 0	0 0 1 0	Test Pattern #1	
0 0 0	0 0 1 1	Test Pattern #2	
0 0 0	0 1 0 0	Offset Cal Register Load	(MSW) (Note 1)
0 0 0	0 1 0 1	Offset Cal Register Load	(LSW) (Note 2)
0 0 0	0 1 1 0	Gain Cal Register Load	
0 0 0	0 1 1 1	Noise Cal Register Load	
0 0 0	1 0 0 0	Offset Cal Register Read	(MSW)
0 0 0	1 0 0 1	Offset Cal Register Read	(LSW)
0 0 0	1 0 1 0	Gain Cal Register Read	
0 0 0	1 0 1 1	Noise Cal Register Read	
0 0 0	1 1 X X	Reserved	

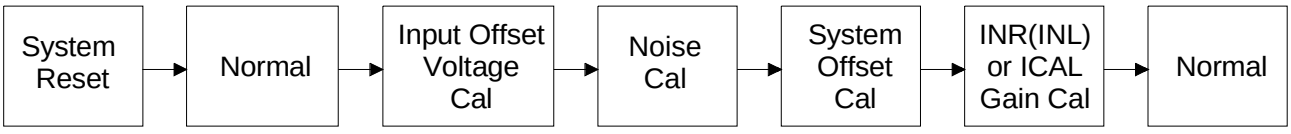
Notes: 1. MSW = Most Significant Word
2. LSW = Least Significant Word

Table 2. Control Modes

pins.

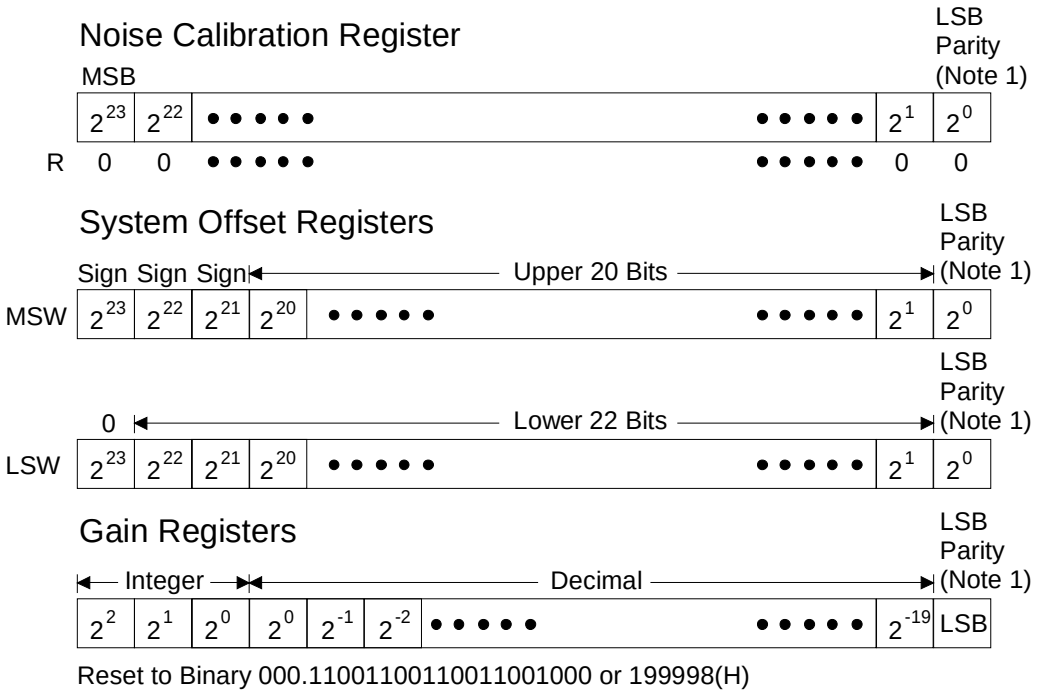
When entering calibration commands via the DTEST lines, the calibration steps must follow a specific sequence for the CS5542/CS5543 pair to be properly calibrated. Figure 4 illustrates the calibration sequence for the CS5542/CS5543 chip set. After the $\overline{RST}$ is issued, the chip set will be in the normal mode. The first calibration step is the Input Offset Voltage Cal mode.

The CS5542 is designed to digitize an input current. This current is normally sourced from a photodiode at the input of the chip. The Input Offset Voltage Cal step is intended to remove any offset at the front end of the modulator. This should be calibrated with no photodiode current present. If the phototdiode is replaced with a resistor, the voltage



Note: Main Current Input must be idle for all calibration modes except for Gain Cal using INL(INR).

Figure 4. Calibration Sequence CS5542/CS5543



Reset to Binary 000.11001100110011001000 or 199998(H)

Note 1: All Parity bits are odd.

Table 3. Calibration Registers

should be zeroed before calibrating the Input Offset Voltage Cal step. The Input Offset Voltage Cal mode will require 23 filter cycles (a filter cycle is one output conversion word) to complete. The CS5543 will not accept new mode commands until the 23 filter cycles have been completed, even if the DTEST pins are changed. After the 23 filter cycles, the calibration step is complete. Note that when the Input Offset Voltage Cal command is initiated inside the CS5543 decimator, the modulators of all of the CS5542 chips connected to the CS5543 will execute the calibration step at the same time. There is no calibration word or register inside the CS5543 which contains the calibration data for this calibration step.

The next calibration to be performed is the Noise Cal. This calibration step is necessary to calibrate the quantizer threshold of the modulators. This ensures linearity in the multi-bit quantizer. The Noise Cal lasts 409 filter cycles. Upon entering the Noise Cal mode, the system offset registers are set to 0; all gain registers are unaffected. The Noise Cal step can be performed at any time and it can be performed independent of the other calibration steps. When this step is executed, all eight modulators associated with a CS5543 calibrate at the same time. At the end of the Noise Cal step, a 24-bit calibration word is placed into the Noise Cal register inside the CS5543.

After the modulators have been calibrated by the Noise Cal step, the System Offset Cal step is performed. The current present at the INL (INR) input at the time the System Offset Cal is performed will treated as the zero point of the converter transfer function. The System Offset Cal step lasts 1028 filter cycles. At the end of the System Offset Cal, a signed 43-bit result is placed into two System Offset Cal registers (MSW and LSW; Most Significant Word and Least Significant Word) inside the CS5543. After the System Offset Cal is complete, the next calibration step is a gain calibration. To perform a gain calibration, an input signal must be

provided into the CS5542. The CS5542 dual modulator is designed to allow for two possible means of inputting the signal necessary to perform this calibration step. The input method chosen will dictate whether an ICAL Full-Scale Gain Cal or a System Full-Scale Gain Cal is to be performed.

At the input of the CS5542 is an ICAL pin. A current can be sourced into this pin to provide a calibration current to set the full scale point (actually 97% of the full scale value as will be discussed later) of the system. The current into the ICAL pin will be used to calibrate the gain if the Full-Scale Gain Cal mode (using the ICAL input) is selected. Note that the ICAL pin on the CS5542 is shared between the two modulators. Each modulator will be calibrated sequentially (only one of eight channels will be active at a time during the calibration if the ICAL Full-Scale Gain Cal mode is executed. The CS5543 will sequentially calibrate each one of the eight modulators associated with it. Each Gain Cal requires 5 filter cycles; therefore 40 filter cycles will elapse for the ICAL Full-Scale Gain Cal. At the end of the Gain Cal, a 24-bit calibration word is placed into the Gain Register of the CS5543.

Selection of the ICAL Full-Scale Gain Cal mode enables the ICAL input switch (note that the normal current input remains active and its current will be summed with the ICAL current when using this mode). During an ICAL Full-Scale Gain Cal cycle, only one ICAL input is active at any one time, therefore a single external resistor and a voltage source can supply a current which can be used to calibrate all eight channels associated with a single CS5543. Alternatively, four individual resistors can be supplied, one for each CS5542 dual channel ICAL input.

The magnitude of the calibration current should be 3% less than the desired full scale current. Recall that the nominal full scale input current magnitude is set by the size of the internal transimpedance capacitor, the clock rate, and the VREF voltage. The output code produced by this current will be 2^{21} - 2^{16} -1 or approximately 97% of full scale. The 97% gain point can be calibrated with currents as low as 40% below the nominal full scale value set by the clock rate, cap size, and VREF voltage. It is preferable to keep the input current for calibration within 20% of the nominal full scale value as lower levels of input calibration magnitude will exhibit a slight reduction in dynamic range.

If the Full-Scale Gain Cal mode using INL (INR) is selected, the ICAL input MUX at the front of each CS5542 is not used. Instead, the gain is calibrated using the current input into the INL and INR pins. Again, the current supplied should be 3% less than the desired full scale value. The output code due to this current will be set to 2^{21} - 2^{16} -1 or approximately 97% of full scale.

For either gain calibration mode (ICAL or INL (INR)) the magnitude of the input current should be 97% of the nominal full scale, but the polarity is not important. The current can be sinked or sourced. In either case the CS5543 will calibrate the positive full scale point. Once calibrated, currents into the INL or INR pins will result in a positive output code, while currents out of the pins will yield a negative output code.

Calibration Register Readability

The CS5543 has registers which hold the digital calibration words for each of the eight channels. For each of the channels, there are four 24-bit registers. The Noise Cal and Gain Cal functions each result in a 24-bit digital calibration word, whereas the System Offset Cal function produces a 48-bit calibration word which is split into two 24-bit registers. These registers can be read and their contents stored into some nonvolatile storage from which they can be recalled and reloaded if so desired.

The 48-bit Offset register contents must be read or

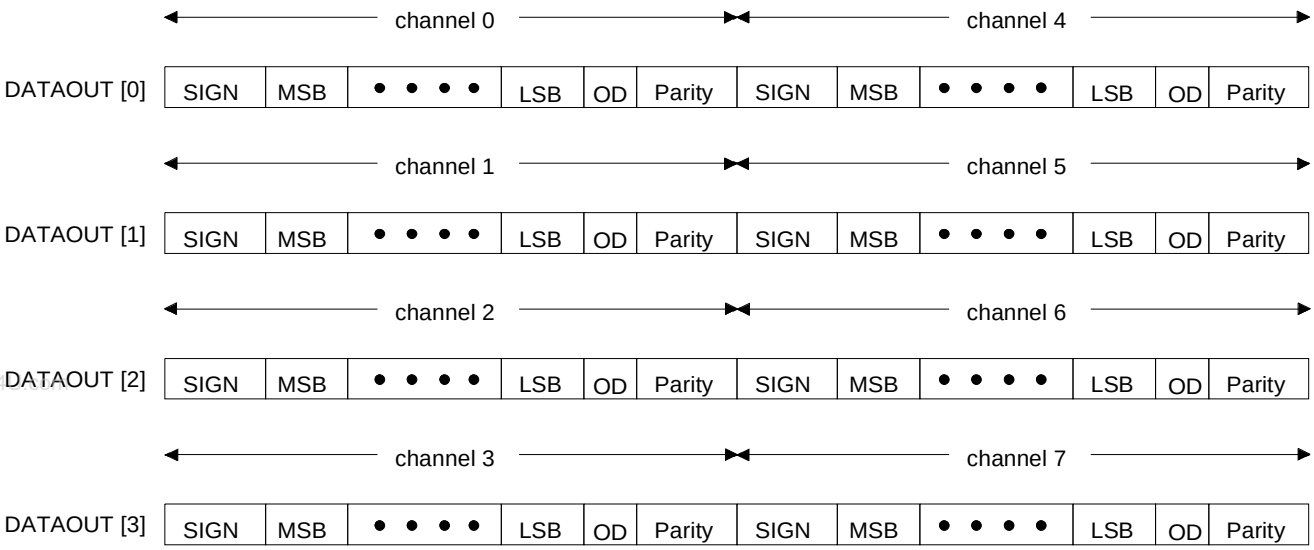


Figure 5. Data Transfer Timing

written with two read cycles using different commands to read either the MSW (Most Significant Word) or the LSW (Least Significant Word).

When reading or writing to the calibration registers, the register contents are time-division multiplexed into or out of the CS5543 in the same manner as conversion data as shown in Figure 5.

In addition to writing or reading the calibration registers, the CS5543 provides several test modes. Some of these test modes are as follows: The DATAOUT [3:0] pins can be set to a high impedance output state; or either of two different test patterns can be requested to be output on the DATAOUT [3:0] pins of the CS5543. See Table 4 for the test pattern information.

Commands to change calibration modes or control modes should not be issued to the system while a calibration is in progress. New data for the calibration or control modes is latched on every falling edge of CLKIN and takes effect on the following rising edge of FRAME.

Test Pattern #1:
(all channels)

HEX	BINARY
Test Pattern #1: (All channels)	
A00001	0001 0000 0000 0000 0000 0001 Sign, MSB LSB, parity

Test Pattern #2:
(Unique for each channel)

Channel	HEX	BINARY
0	1000A0	0001 0000 0000 0000 0000 0001
1	000A01	0000 0000 0000 1010 0000 0001
2	20A000	0010 0000 1010 0000 0000 0000
3	0A0001	0000 1010 0000 0000 0000 0001
4	450000	0100 0101 0000 0000 0000 0000
5	005001	0000 0000 0101 0000 0000 0001
6	800500	1000 0000 0000 0101 0000 0000
7	000051	0000 0000 0000 0000 0101 0001
		Sign, MSB LSB, parity

Table 4. Test Patterns

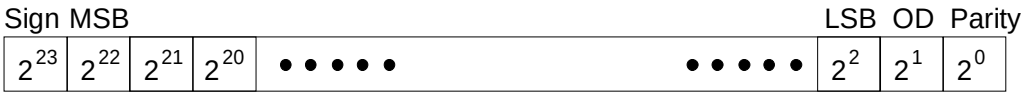


Figure 6. Data Conversion Word Format

Bipolar Input Current	Output Code (Sign and 21 Data Bits)						
Positive Full Scale[1]	1	0	0000	0000	0000	0000	0000
Zero Input	0	0	0000	0000	0000	0000	0000
Negative Full Scale	1	1	1111	1111	1111	1111	1111

Note 1 Positive Full Scale is current going into the modulator.

$D_{OUT} = 2{,}097{,}151\ [(I_{IN} - I_{OF})/(I_{FS} - I_{OF})]$ where D_{OUT} is the digital output code from the CS5543; I_{OF} is the current going into the modulator during System Offset Voltage Calibration; I_{FS} is the full scale input current which is always positive in magnitude and will be the absolute value of the current going into either INL/INR or ICAL pin, divided by 0.97; and I_{IN} is the current going into the modulator during the conversion. 2,097,151 is $2^{21} - 1$.

Table 5. Output Coding for CS5542/CS5543.

Conversion Coding

Each of the channels of the CS5543 outputs a 24-bit conversion data word. The word includes a sign bit along with 21 additional data bits, an Oscillation Detect flag (OD), and an odd parity bit. The format of the data conversion word is shown in Figure 6.

The OD bit is set whenever the modulator in the CS5542 is overranged to the point of making it lose stability. Under this condition the output data can be erroneous. The OD bit can be set whenever the input magnitude exceeds the full scale point by greater than 5%. The OD bit will be cleared whenever the modulator input comes back into proper range.

Table 5 illustrates the output coding for the CS5542/CS5543 chip set. Positive current means that current is flowing into the INL (INR) pin and produces a positive output code.

CS5543 Serial Data Interface

The serial data interface on the CS5543 has four input signals and four output signals. Data read from the CS5543 is output from the DATAOUT[3:0] pins. DATAOUT[0] outputs data from channels 0 and 4; DATAOUT[1] outputs data from channels 1 and 5; DATAOUT[2] outputs data from channels 2 and 6; and DATAOUT[3] outputs data from channels 3 and 7. Information from DATAOUT[0] is output beginning with the sign bit of channel 0 and ends with the parity (odd) bit of channel 4. Data out of the other DATAOUT pins follows the same convention.

In a system, multiple CS5543s are connected with the DATAOUT pins of one CS5543 connected to the DATAIN pins of the next CS5543. DATAOUT[3:0] lines will change immediately after the rising edge of DATACLK, and be latched into the DATAIN[3:0] pins on the next rising edge of DATACLK.

A timing diagram which shows eight channels of data transfer from one CS5543 to another is shown in Figure 5.

The data which is transmitted either to or from the series-connected CS5543s is synchronized by the FRAME signal. FRAME should be a pulse, one CLKIN cycle wide, generated by falling edges of

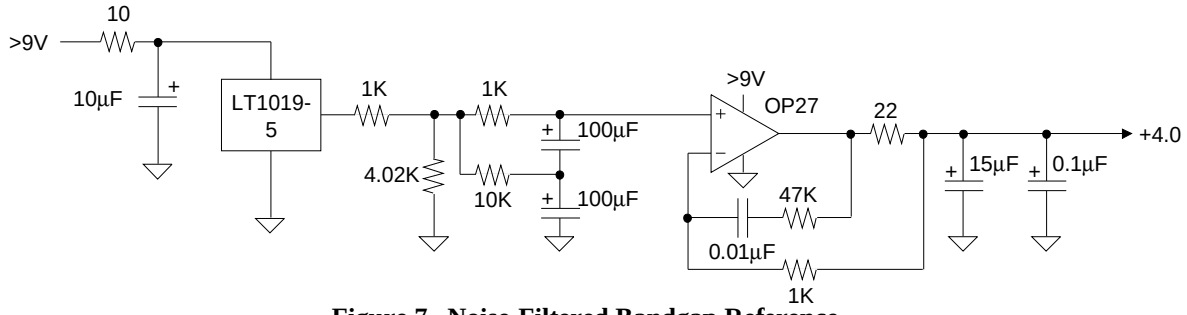


Figure 7. Noise-Filtered Bandgap Reference

CLKIN. FRAME will be latched into the CS5543 by the rising edge of CLKIN. This will subsequently generate an FSYNC signal to synchronize the CS5542 modulators.

System Connections

An eight channel digitizer system can be constructed using four CS5542 dual modulators with one CS5543 eight-channel decimator. Figure 2 illustrates the hardware signal connections for an eight channel system.

Digitizer blocks of eight channels each can be cascaded to connect 128 blocks together for a total of 1024 digitizer channels. All clocks in the system are related to the CLKIN master clock. Assuming that CLKIN= 2.048 MHz, the converter output word rate will be CLKIN/2048. A data framing signal, FRAME, synchronizes the digital output data and the modulator data. The FRAME signal must occur at the output word rate. The DATACLK must be three times faster than the CLKIN rate, 6.144 MHz in this example.

The CS5543 has four DATAOUT lines. Each of the lines provides an output for the data from two of the eight channels associated with a single CS5543. Data from any one DATAOUT line is serially transferred out of the DATAOUT pin in 48-bit blocks, consisting of two 24-bit words.

With 128 CS5543 linked together, each of the four serial lines linking DATAOUT pins to DATAIN pins is in effect a serial shift register 6144 (48 X 128) bits long. The DATACLK is used to shift data out of each CS5543 in 48 bit blocks. For a 1024 channel system with an CLKIN rate of 2.048 MHz, the 6.144 MHz DATACLK will shift out the data for all 1024 channels in one millisecond.

Analog Input

The CS5542 modulator is optimized to be driven by a photodiode current source. Photodiodes have large output impedances. A photodiode also has a capacitance which is a function of its size. The CS5542 relies on this capacitance to ensure the stability of its input stage. The capacitance also affects the bandwidth of the input circuit.

In all cases the modulator assumes that the external shunt capacitance of the photodiode is at least 220pF.

If the input source is actually a voltage source and a resistor is used to generate the input current, a 220 pF capacitor should be connected between the input pin and ground. The resistor will add additional current noise into the circuit and will degrade the dynamic range somewhat.

Voltage Reference

The voltages supplied to the VREF+ and VREF- pins can range from ±2.0 volts to ±4.1 volts with ±4. 0 volts being preferred. VREF+ and VREF- voltages should be balanced and have low noise. Figure 7 illustrates how a bandgap voltage reference can be well filtered to provide a low noise source for +4.0 volts.

Each VREF+ or VREF- input on a CS5542 may require up to 1 microamp of reference current. The number of channels which can be supplied from one voltage reference buffer will depend upon the buffer's output impedance and the distance between the CS5542 and the reference circuitry. A well-designed voltage reference should be able to supply 32 channels (16 CS5542s) in a system.

Board Layout

The circuit board containing the CS5542 modulator should have a ground plane split through middle of the modulator with pins 2 through 13 over a quiet analog ground plane. In addition, guarding techniques should be used around the low level inputs INL, INR, and ICAL. Care must also be exercised to ensure that the circuit card is manufactured with good quality to ensure low leakage. After assembly, the card should be cleaned to ensure it is free from all surface contaminants.

Clock Source

CLKIN must have low jitter; less than 20 psec RMS. Note that any drift in CLKIN over time or temperature will show up as a gain error in the CS5542/CS5543 measurement system; therefore a stable clock source is highly desirable.

Power Supply

Power supply noise and ripple must be very low within the passband of the CS5543 digital filter. This noise and ripple can pass through the ESD (Electrostatic Discharge) protection diodes at the INL (INR) pin into the transimpedance stage of the CS5542 modulator. With the capacitance of this diode at about 5 pF, and the transimpedance resistor of the first stage at about 2-10 megohm, coupling of supply ripple is going to occur. For this reason, the noise and ripple on the power supplies should be low enough that the noise coupled into the transimpedance stage should remain below the noise floor of the converter across the bandwidth of the digital filter. To achieve this, 60 Hz related noise and ripple should remain below 50 microvolts peak-to-peak.

Digital Filter

The digital filter is a linear phase FIR filter. The filter has a group delay of three conversion words and an equivalent noise bandwidth of 0.536 of the output word frequency. Plots for the filter are shown in the data sheet tables. Coefficients are tabulated in the Appendix of this data sheet.

Joint Test Action Group (JTAG) Boundary-Scan Interface

The CS5543 is designed for large multi-channel systems. For this reason the chip is designed to support the IEEE Standard Access Port and Boundary-Scan Architecture as defined in IEEE Std. 1149.1-1990, or P1149.1. This standard defines circuitry which is built into the an integrated circuit to assist in the test, maintenance, and support of a system at the printed circuit board level. The CS5543 includes circuitry which supports this standard.

It is highly recommended that if this type of test capability is desired in your system, that you acquire a copy of the IEEE standard which thoroughly discusses the IEEE Standard Access Port and Boundary-Scan Architecture as it will only be discussed briefly here.

The CS5543 includes a TAP (Test Access Port) made of the following connections: TCK (Test Clock), TMS (Test Mode Select input), TDI (Test Data Input), and TDO (Test Data Output). In addition to the TAP, the test logic includes a TAP controller, an instruction register, and a set of test registers. The TAP controller is a synchronous finite state machine which controls the sequence of operations necessary to implement the boundary-scan architecture. Figure 8 illustrates the TAP controller state diagram. The instruction register allows an instruction to be shifted into the design.

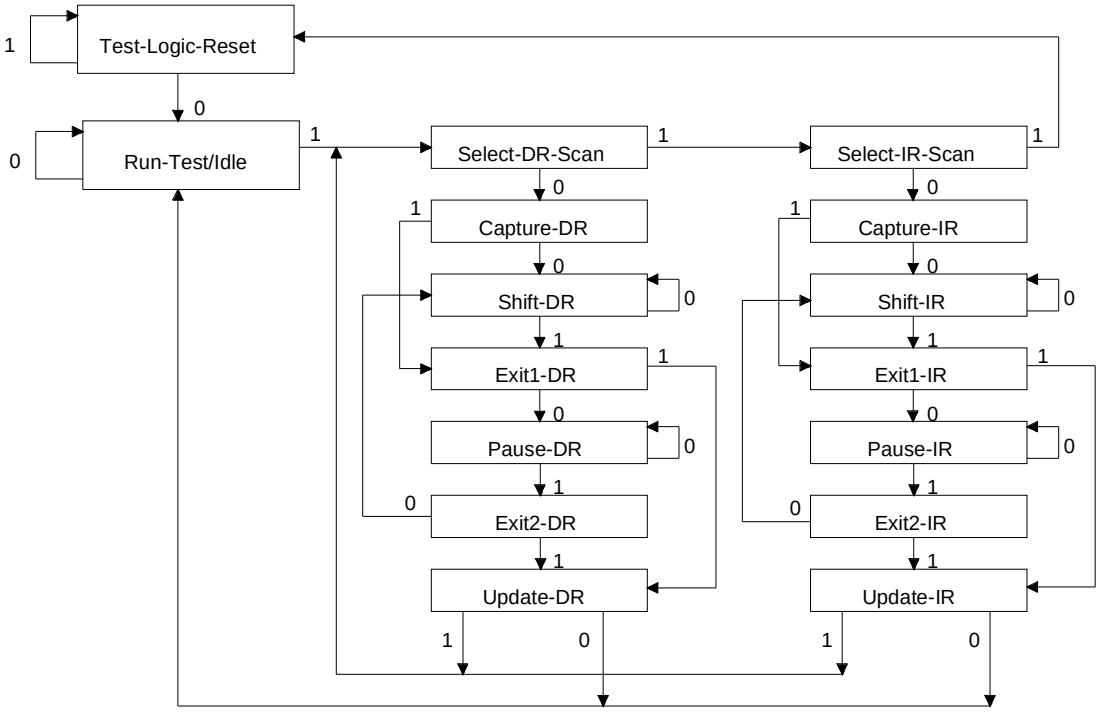


Figure 8. TPA Controller State Diagram

The instruction register is used to select the test to be performed or to select the test data register to be accessed. The 3-bit instructions available in the instruction register are illustrated in Table 6. The LSB of the 3-bit instruction is shifted in first.

IR CODE	INSTRUCTION
000	EXTEST
001	SAMPLE/PRELOAD
010	IDCODE
011	OPERATING MODE REGISTER
100	reserved
101	reserved
110	reserved
111	BYPASS

Table 6. Boundary Scan Instructions

Several test registers are in the design including the Boundary-Scan Register (BSR), the Device Identification Register (DIR), the Operating Mode Register (OMR), and the Bypass Register (BR).

The Boundary-Scan Register allows for the testing of board interconnects. The bit ordering for the BSR is the same as the top-view packaged pinout, clockwise beginning with the MDATA[3], and ending with $\overline{RST}$. The TAP, power and gnd pins are not included as part of the boundary-scan register. The BSR is 47 bits long. Inputs can be set via the BSR, bypassing the actual pin. All outputs are 3-state (logic high, low and or high impedance) outputs. Their states during test can be controlled via the PRELOAD instruction. In the boundary-scan register, each input pin of the device is represented by one bit position of the boundary scan register, whereas each of the outputs, having the possibility of any one of three states, require two bits each in the boundary-scan register.

The Device Identification Register is designed to identify the manufacturer, the part number, and the version number of the CS5543. The format of the DIR is illustrated in Table 7. Data from the DIR is shifted out of the TDO LSB first. Note that when the CS5543 is reset, the Instruction Register is set to select IDCODE.

The Operating Mode Register (OMR) allows access to the device operating modes via the DATSEL and DMODE pins as shown in figure 9.

The Bypass Register allows a minimum length path between the TDI and TDO pins on the device. This register can be selected whenever the device does not need to be tested during board-level test operation.

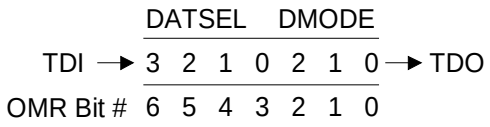


Figure 9. Operating Mode Register

TAP Operation for EXTEST

Before execution of the instruction EXTEST, the SAMPLE/PRELOAD instruction must be used to load testing data to all output pins through TDI. Each output pin requires two bits. The first bit to be shifted in controls the output enable function. If a logic 1 is entered, the output is enabled; if a logic 0 is entered, the output is disabled. The second bit shifted in after the first bit is the test data. Therefore, two TCK cycles are required to load testing data into the boundary-scan register for each output pin.

Device Identification Register

MSB 31 … 16

V3	V2	V1	V0	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4

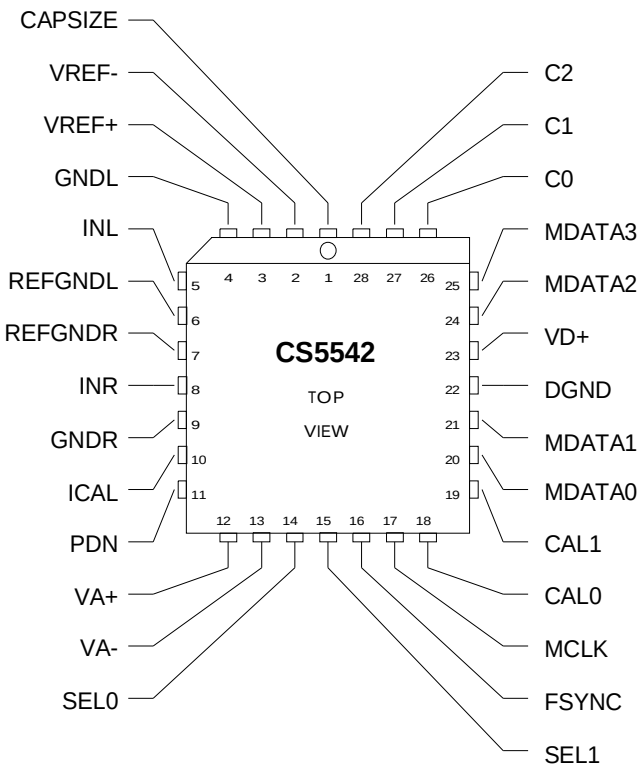
15 … LSB 0

P3	P2	P1	P0	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	1

BIT	NAME	VALUE	FUNCTION
V3-V0	Version Bits	0000	Version Number of Device
P15-P0	Part Number Bits	0101010101000011	Part Number of Device
M10-M0	Manufacture Number Bits	00001100100	Manufacture Number
L0	Logic 1	1	Always Logic 1

Table 7. Device Identification Register

CS5542 PIN DESCRIPTIONS



Power Supplies

GNDL - Ground Left, Pin 4.

Left modulator analog ground for integrators 2 through 5.

REFGNDL - Reference Ground Left, Pin 6.

Analog ground for left modulator integrator 1 and summing node.

GNDR - Ground Right, Pin 9.

Right modulator analog ground for integrators 2 through 5.

REFGNDR - Reference Ground Right, Pin 7

Analog ground for right modulator integrator 1 and summing node.

VA+ - Positive Analog Supply, Pin 12.

Positive analog supply voltage. Nominally +5 volts.

VA- - Negative Analog Supply, Pin 13.

Negative analog supply voltage. Nominally -5 volts.

VD+ - Digital Supply, Pin 23.

Digital supply voltage. Nominally +5 volts.

CS5542 PIN DESCRIPTIONS

DGND - Digital Ground, Pin 22.

Digital ground.

Digital Input Pins-

MCLK - Modulator Clock Input, Pin 17.

The modulator clock input provides the necessary clock for operation of the modulator. MCLK operates at 16 times the modulator sample rate. MCLK is 2048 times the output word rate.

FSYNC - Frame Sync, Pin 16.

The transition from a low to high level on this input supplied by the CS5543, will reset the internal master timing of the CS5542 and synchronize its data with each output word.

CAL[1:0] - Calibration Control, Pins 19, 18.

The mode of operation for the CS5542 is selected through the calibration control pins via the CS5543 and is summarized in the table below.

CAL1	CAL0	Mode Selected
0	0	Normal Operation, Noise CAL, Offset CAL
0	1	Input offset voltage calibrate
1	0	Unused code
1	1	Full Scale gain calibrate

Normal Calibration Sequence

01	Input Offset
00	Noise CAL(Dark)
00	Offset CAL(Dark)
11	Gain CAL
00	Normal Operation

SEL[1:0] - Time Slot Selections, Pins 15,14

The binary code applied to SEL0 and SEL1 will determine the time slot pair associated with the CS5542. Each of the up to four CS5542's connected to a single CS5543 must have a unique code assigned to the combination of SEL0 and SEL1.

CAPSIZE - Full Scale Input Range Select, Pin 1.

When CAPSIZE = 0, C_{DAC} = 1.6 pF; when CAPSIZE = 1, C_{DAC} = 4.8 pF

CS5542 PIN DESCRIPTIONS

PDN - Power Down, Pin 11.

When asserted the CS5542 will enter the power-down state.

C[2:0] - ICAL Input Select, Pins 28, 27, 26.

In an array of 4 CS5542's (eight channels), C2-C0 will select which channel is to receive the d.c. current applied to the ICAL pins.

Digital Outputs Pins-

MDATA[3:0] - Modulator Data Outputs, Pins 25, 24, 21, 20.

The tri-level modulator data is output on MDATA3 - MDATA0 for decimation by the CS5543.

Modulator Output Coding Table

Overload	-1	zero	+1	
MDATA3	MDATA2	MDATA_1	MDATA0	Value / Meaning
1	0	0	1	+1 / Normal operation
1	0	1	0	0 / Normal operation
1	1	0	0	-1 / Normal operation
0	1	1	0	+1 / Modulator Overload
0	1	0	1	0 / Modulator Overload
0	0	1	1	-1 / Modulator Overload

As shown in the table above, a constant number of zeros and ones exist for all output states. This provides a data-independent noise invariant coding to maximize isolation between channels.

Analog Input Pins -

VREF-,VREF+ - Differential Voltage Reference Inputs, Pins 2, 3.

A differential voltage reference on these pins operates as the voltage reference for the CS5542. Nominally, it is -4.0 V and + 4.0 respectively.

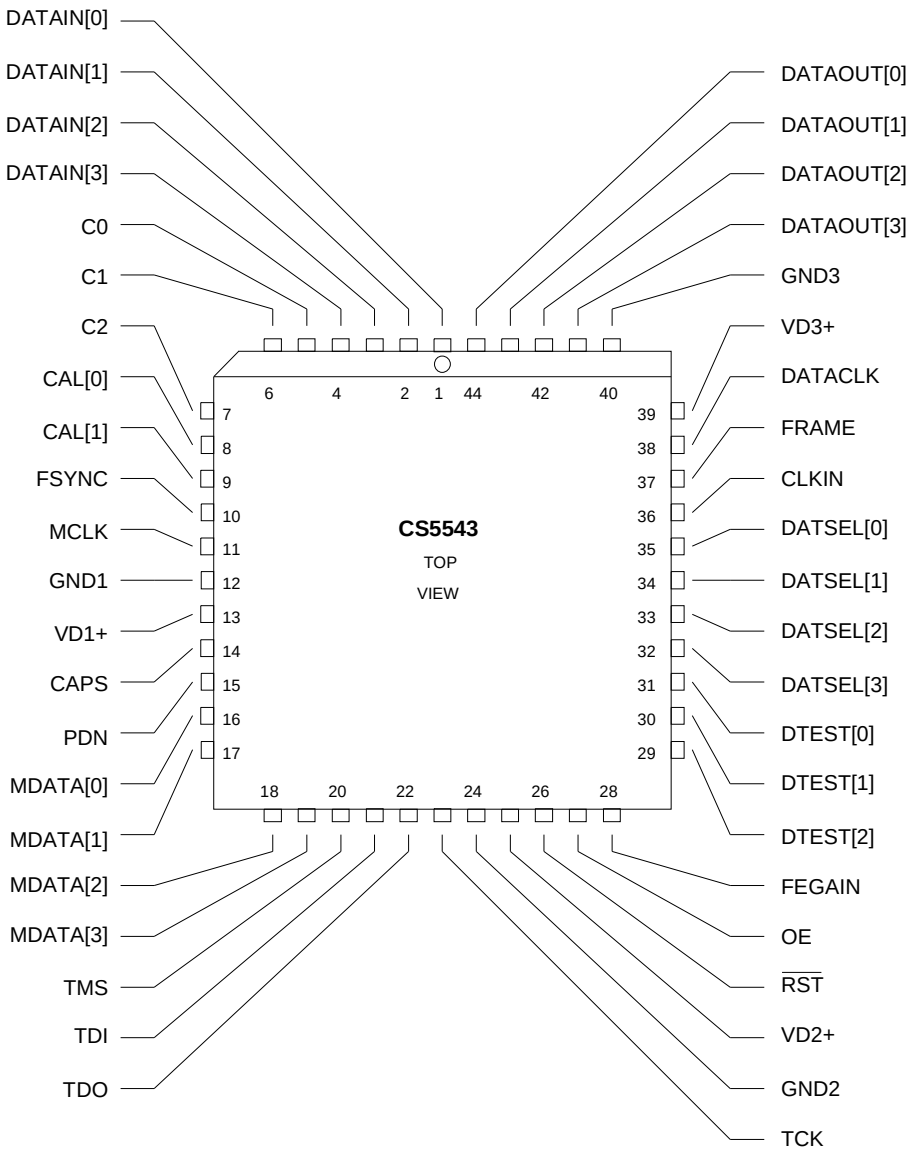
ICAL - Full-Scale Current Calibration Input, Pin 10.

ICAL needs to be supplied for full-scale gain calibration.

INL, INR - Input Left and Input Right, Pins 5, 8.

INL and INR are the left and right modulator current input pins.

CS5543 PIN DESCRIPTIONS



Power Supply

VD1+, VD2+, VD3+ - Digital Power Supplies, Pins 13, 25, 39.
Digital supply voltages. Nominally +5 Volts.

GND1, GND2, GND3 - Digital Ground, Pins 12, 24, 40.
Digital grounds.

DSM-DSD Interface Pins

C[2:0] - ICAL Channel Select (Outputs), Pins 7, 6, 5.
In an array of 4 CS5542's (eight channels), C2-C0 will select which channel is to receive the d.c. current applied to the ICAL pins during full-scale gain calibration.

CS5543 PIN DESCRIPTIONS

CAL[1:0] - Calibration Control (Outputs), Pins 8, 9.

The mode of operation for the CS5542 is selected through the calibration Control pins. See the table in the pin-out section of the CS5542 data sheet for details.

FSYNC - Frame Sync (Output), Pin 10.

The transition from a low to high level at the CS5542's input will reset the internal master timing of the CS5542 and synchronize its data with each output word from the CS5543.

MCLK - Modulator Clock (Output), Pin 11.

The modulator clock output provides the necessary clock for operation of the modulator.

CAPSIZE - Full Scale Input Range Select (Output), Pin 14.

Controls the CAPSIZE input to the CS5542. This determines the size of the sampling capacitor used by the CS5542.

PDN - Power Down (Output), Pin 15.

When asserted the CS5542 will enter the power-down state.

MDATA[3:0] - Modulator Data Inputs (Inputs), Pins 16, 17, 18, 19.

The tri-level modulator data is input to the CS5543 via MDATA3 - MDATA0 for decimation. See the table in the pin-out section of the CS5542 data sheet for details.

Test Access Port Pins

TMS -Test Mode Select (Input), Pin 20.

Controls the state-to-state operation of the TAP controller.

TDI - Test Data Input (Input) , Pin 21.

Serially inputs data to the Test Access Port.

TDO - Test Data Output (Output), Pin 22.

Serially outputs data from the Test Access Port.

TCK - Test Clock (Input), Pin 23.

The clock for the Test Access Port, shorted to MCLK

Control Pins

OE - Output Enable (Input), Pin 27.

Enables or disables (tri-states) all output pins on the CS5543.

FEGAIN - Front-End Gain Select (Input), Pin 28.

Selects the Front-End Capacitor Gain Ratio. A full calibration is necessary following any change to this input.

CS5543 PIN DESCRIPTIONS

DMODE[2:0] - Digital Mode Select (Inputs), Pins 29, 30, 31.
Selects the operation mode of the CS5543.

DATSEL[3:0] - Data Selection Mode (Inputs), Pins 32, 33, 34, 35.
Selects the Data to be placed on the DATAOUT[3:0] pins.

$\overline{\text{RST}}$ - Chip Reset (Input), Pin 26
Resets all internal logic and registers.

DSD-System Interface Pins

DATACLK - Serial Data Clock (Input), Pin 38.
Clock signal generated by the system controller which governs all serial output data timing from the CS5543.

CLKIN - Master System Clock (Input), Pin 36.
A CMOS compatible clock input to this pin governs all non-serial data timing.

FRAME - Framing Signal (Input), Pin 37.
Synchronizes DATACLK and MCLK for each frame of output data from the CS5543.

DATAOUT[3:0] - Serial Output Data (Outputs), Pins 41-44.
CS5543 serial output data.

DATAIN[3:0] - Serial Data Inputs (Inputs), Pins 1-4.
CS5543 serial input data from the serial output of the adjacent CS5543 in a multi-decimator system.

Filter Coefficients

h(0)=h(383)= -6	h(32)=h(351)= -2988	h(64)=h(319)= -32337	h(96)=h(287)= -6663	h(128)=h(255)= 613898	h(160)=h(223)= 2079544
h(1)=h(382)= -7	h(33)=h(350)= -3327	h(65)=h(318)= -33741	h(97)=h(286)= -229	h(129)=h(254)= 649637	h(161)=h(222)= 2126869
h(2)=h(381)= -10	h(34)=h(349)= -3695	h(66)=h(317)= -35134	h(98)=h(285)= 6812	h(130)=h(253)= 686379	h(162)=h(221)= 2173544
h(3)=h(380)= -15	h(35)=h(348)= -4094	h(67)=h(316)= -36508	h(99)=h(284)= 14489	h(131)=h(252)= 724107	h(163)=h(220)= 2219496
h(4)=h(379)= -21	h(36)=h(347)= -4524	h(68)=h(315)= -37856	h(100)=h(283)= 22828	h(132)=h(251)= 762800	h(164)=h(219)= 2264653
h(5)=h(378)= -29	h(37)=h(346)= -4988	h(69)=h(314)= -39167	h(101)=h(282)= 31855	h(133)=h(250)= 802436	h(165)=h(218)= 2308943
h(6)=h(377)= -39	h(38)=h(345)= -5487	h(70)=h(313)= -40431	h(102)=h(281)= 41596	h(134)=h(249)= 842990	h(166)=h(217)= 2352295
h(7)=h(376)= -52	h(39)=h(344)= -6021	h(71)=h(312)= -41638	h(103)=h(280)= 52077	h(135)=h(248)= 884434	h(167)=h(216)= 2394640
h(8)=h(375)= -67	h(40)=h(343)= -6594	h(72)=h(311)= -42777	h(104)=h(279)= 63323	h(136)=h(247)= 926737	h(168)=h(215)= 2435908
h(9)=h(374)= -85	h(41)=h(342)= -7205	h(73)=h(310)= -43834	h(105)=h(278)= 75361	h(137)=h(246)= 969867	h(169)=h(214)= 2476030
h(10)=h(373)= -107	h(42)=h(341)= -7856	h(74)=h(309)= -44798	h(106)=h(277)= 88214	h(138)=h(245)= 1013788	h(170)=h(213)= 2514942
h(11)=h(372)= -133	h(43)=h(340)= -8549	h(75)=h(308)= -45655	h(107)=h(276)= 101906	h(139)=h(244)= 1058463	h(171)=h(212)= 2552576
h(12)=h(371)= -163	h(44)=h(339)= -9283	h(76)=h(307)= -46389	h(108)=h(275)= 116461	h(140)=h(243)= 1103850	h(172)=h(211)= 2588870
h(13)=h(370)= -199	h(45)=h(338)= -10060	h(77)=h(306)= -46987	h(109)=h(274)= 131900	h(141)=h(242)= 1149907	h(173)=h(210)= 2623763
h(14)=h(369)= -240	h(46)=h(337)= -10881	h(78)=h(305)= -47431	h(110)=h(273)= 148246	h(142)=h(241)= 1196589	h(174)=h(209)= 2657194
h(15)=h(368)= -287	h(47)=h(336)= -11745	h(79)=h(304)= -47706	h(111)=h(272)= 165518	h(143)=h(240)= 1243847	h(175)=h(208)= 2689106
h(16)=h(367)= -342	h(48)=h(335)= -12654	h(80)=h(303)= -47793	h(112)=h(271)= 183736	h(144)=h(239)= 1291632	h(176)=h(207)= 2719443
h(17)=h(366)= -404	h(49)=h(334)= -13608	h(81)=h(302)= -47674	h(113)=h(270)= 202918	h(145)=h(238)= 1339892	h(177)=h(206)= 2748154
h(18)=h(365)= -475	h(50)=h(333)= -14605	h(82)=h(301)= -47330	h(114)=h(269)= 223081	h(146)=h(237)= 1388572	h(178)=h(205)= 2775188
h(19)=h(364)= -556	h(51)=h(332)= -15646	h(83)=h(300)= -46742	h(115)=h(268)= 244240	h(147)=h(236)= 1437615	h(179)=h(204)= 2800497
h(20)=h(363)= -647	h(52)=h(331)= -16730	h(84)=h(299)= -45888	h(116)=h(267)= 266410	h(148)=h(235)= 1486965	h(180)=h(203)= 2824037
h(21)=h(362)= -750	h(53)=h(330)= -17856	h(85)=h(298)= -44749	h(117)=h(266)= 289602	h(149)=h(234)= 1536559	h(181)=h(202)= 2845767
h(22)=h(361)= -865	h(54)=h(329)= -19023	h(86)=h(297)= -43301	h(118)=h(265)= 313827	h(150)=h(233)= 1586337	h(182)=h(201)= 2865647
h(23)=h(360)= -995	h(55)=h(328)= -20228	h(87)=h(296)= -41523	h(119)=h(264)= 339094	h(151)=h(232)= 1636234	h(183)=h(200)= 2883642
h(24)=h(359)= -1139	h(56)=h(327)= -21471	h(88)=h(295)= -39391	h(120)=h(263)= 365410	h(152)=h(231)= 1686186	h(184)=h(199)= 2899720
h(25)=h(358)= -1299	h(57)=h(326)= -22747	h(89)=h(294)= -36881	h(121)=h(262)= 392781	h(153)=h(230)= 1736126	h(185)=h(198)= 2913852
h(26)=h(357)= -1477	h(58)=h(325)= -24055	h(90)=h(293)= -33970	h(122)=h(261)= 421209	h(154)=h(229)= 1785986	h(186)=h(197)= 2926013
h(27)=h(356)= -1674	h(59)=h(324)= -25391	h(91)=h(292)= -30633	h(123)=h(260)= 450696	h(155)=h(228)= 1835697	h(187)=h(196)= 2936181
h(28)=h(355)= -1891	h(60)=h(323)= -26751	h(92)=h(291)= -26845	h(124)=h(259)= 481241	h(156)=h(227)= 1885189	h(188)=h(195)= 2944337
h(29)=h(354)= -2129	h(61)=h(322)= -28131	h(93)=h(290)= -22580	h(125)=h(258)= 512840	h(157)=h(226)= 1934391	h(189)=h(194)= 2950467
h(30)=h(353)= -2391	h(62)=h(321)= -29526	h(94)=h(289)= -17812	h(126)=h(257)= 545489	h(158)=h(225)= 1983233	h(190)=h(193)= 2954560
h(31)=h(352)= -2676	h(63)=h(320)= -30930	h(95)=h(288)= -12515	h(127)=h(256)= 579178	h(159)=h(224)= 2031641	h(191)=h(192)= 2956609

SMART Analog™