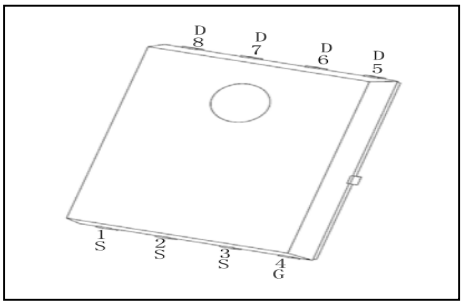
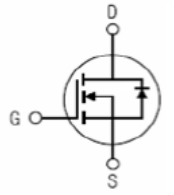
General Description:

CS55N06 AQ3-G, the silicon N-channel Enhanced VDMOSFETs, is obtained by the high density Trenchtechnology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is PDFN 5×6, which accords with the RoHS standard.

V_{DSS}	60	V
I_D（Silicon limited current）	55	A
$R_{DS(ON)Typ}$	11	mΩ



Inner Equivalent Principium Chart



Features:

- **Fast Switching**
- **Low ON Resistance**
- **Low Gate Charge**
- **Low Reverse transfer capacitances**
- **100% Single Pulse avalanche energy Test**
- **Halogen Free**

Applications:

Power switch circuit of adaptor and charger.

Absolute（Tc= 25℃ unless otherwise specified）:

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	60	V
I_D	Continuous Drain Current	55	A
	Continuous Drain Current T_C = 100 °C	38	A
I_{DM}[a1]	Pulsed Drain Current	220	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}[a2]	Single Pulse Avalanche Energy	135	mJ
P_D	Power Dissipation	69.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, –55 to 150	℃

Electrical Characteristics（Tc= 25℃ unless otherwise specified）:

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	60	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 60V, V_{GS}= 0V, T_a = 25℃	--	--	1	μA
		V_{DS} =48V, V_{GS}= 0V, T_a = 125℃	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+20V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-20V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=20A	--	11	14	mΩ
		V_{GS}=4.5V,I_D=20A		13	16	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	0.9	1.4	1.9	V
Pulse width tp≤300μs, δ ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{DS}=30V, V_{GS}=0V, f=1.0MHz	--	2370	--	pF
C_{oss}	Output Capacitance		--	164	--	
C_{rss}	Reverse Transfer Capacitance		--	123	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD} =30V, I_D =10A, R_G = 3Ω, V_{GS}=10V	--	13.1	--	ns
tr	Rise Time		--	25.1	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	60.8	--	
t_f	Fall Time		--	9.0	--	
Q_g	Total Gate Charge	V_{DS}=30V, I_D=20A, V_{GS}=10V	--	50.7		nC
Q_{gs}	Gate to Source Charge		--	7.0	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	12.3	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{SD}	Diode Forward Voltage	I_S=20A,V_{GS}=0V	--	--	1.2	V
trr	Reverse Recovery Time	V_{GS}=0V, I_S=20A, di/dt=100A/us	--	22		ns
Qrr	Reverse Recovery Charge		--	19.5		nC
Pulse width tp≤300μs, δ ≤2%						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	1.8	℃/W

Notes:

[a1]: Repetitive rating; pulse width limited by maximum junction temperature

[a2]: Vdd=25V，L=1mH, I_{AS}=17A, Start T_J=25℃

[a3]: Recommend soldering temperature defined by IPC/JEDEC J-STD 020

Characteristics Curve:

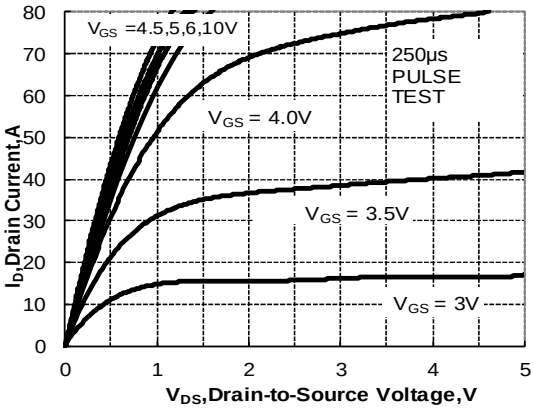


Figure 1. Output Characteristics

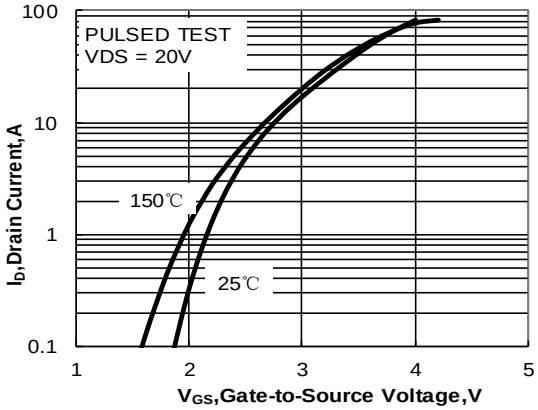


Figure 2.Transfer Characteristics

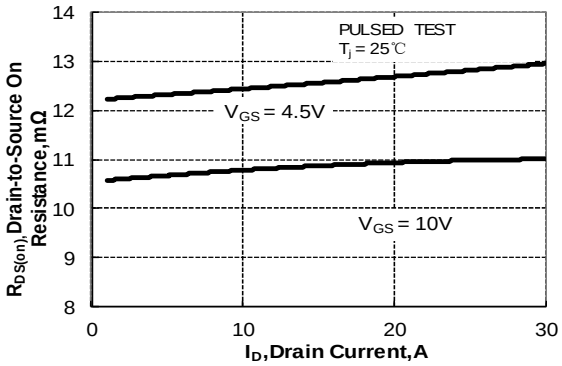


Figure 3. Drain-to-Source On Resistance vs Drain Current

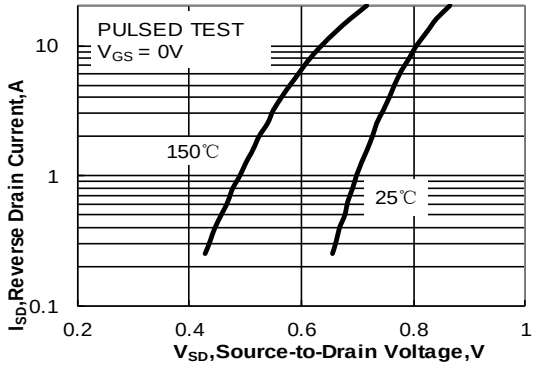


Figure 4. Typical Body Diode Transfer Characteristics

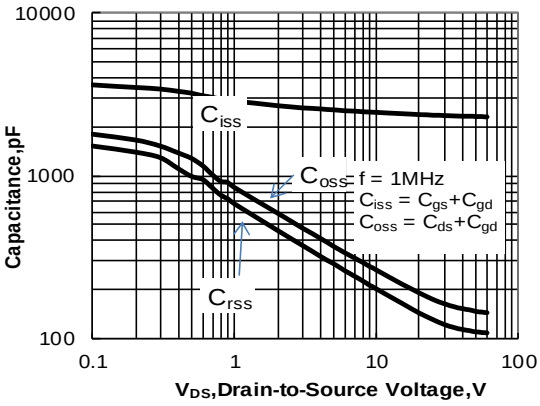


Figure 5. Capacitance Characteristics

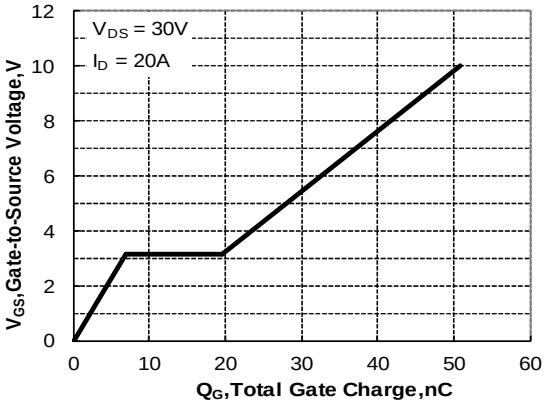


Figure 6. Gate Charge Characteristics

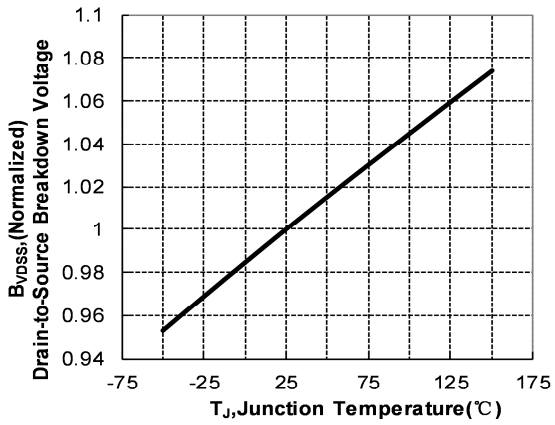


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

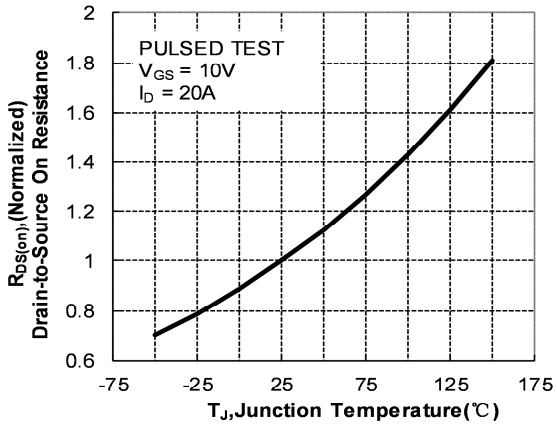


Figure 8. Normalized On Resistance vs Junction Temperature

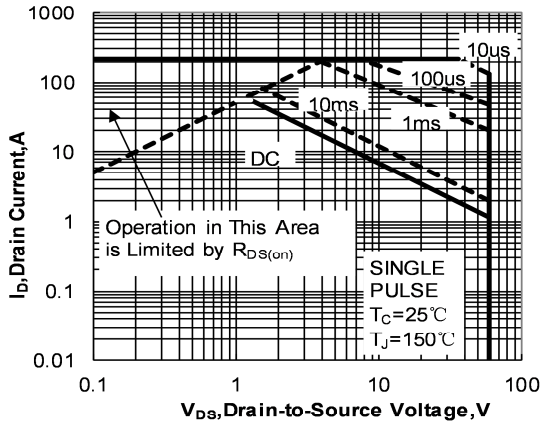


Figure 9. Maximum Safe Operating

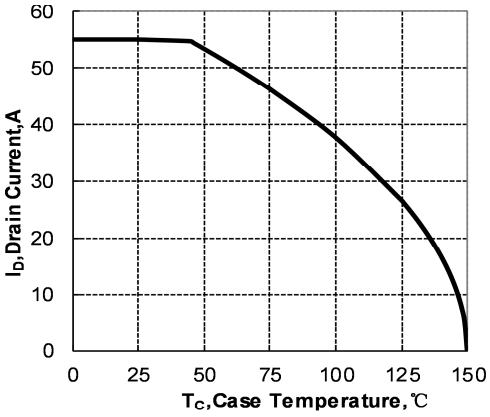


Figure 10. Maximum Continuous Drain Current vs Case Temperature

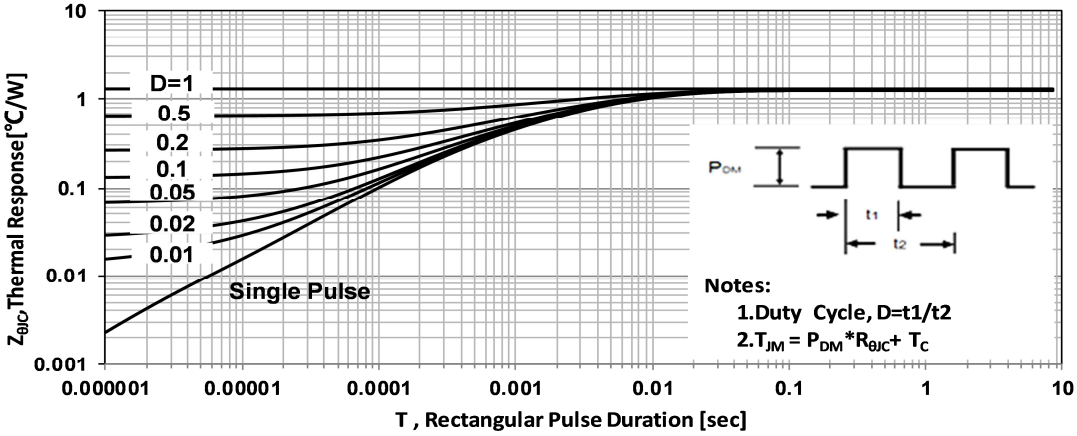


Figure 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

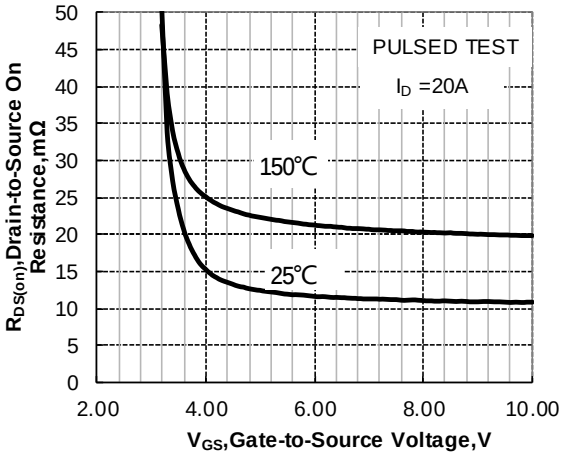


Figure 12. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

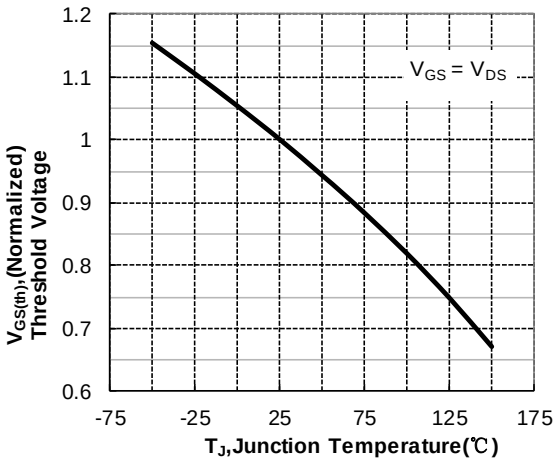


Figure 13. Normalized Threshold Voltage vs Junction Temperature

Test Circuit and Waveform：

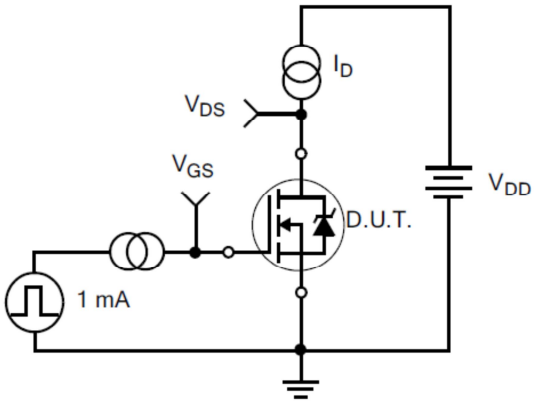


Figure 14. Gate Charge Test Circuit

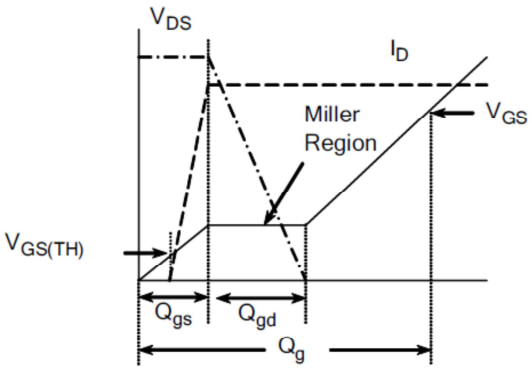


Figure 15. Gate Charge Waveforms

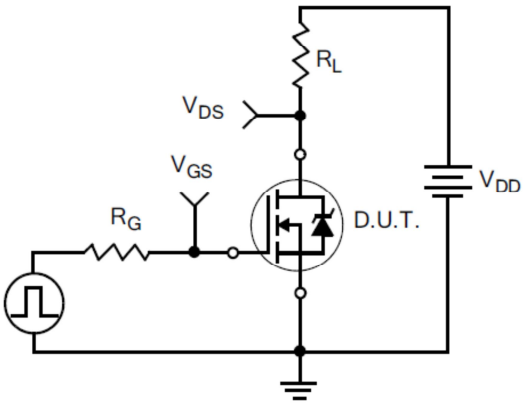


Figure 16. Resistive Switching Test Circuit

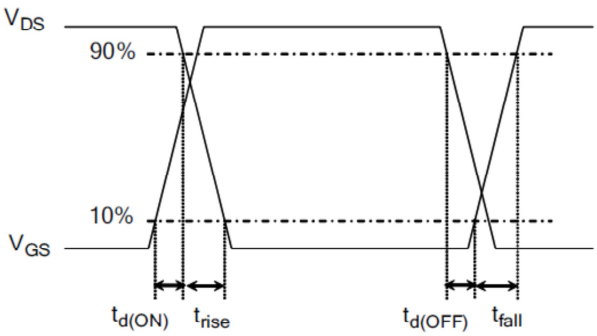


Figure 17. Resistive Switching Waveforms

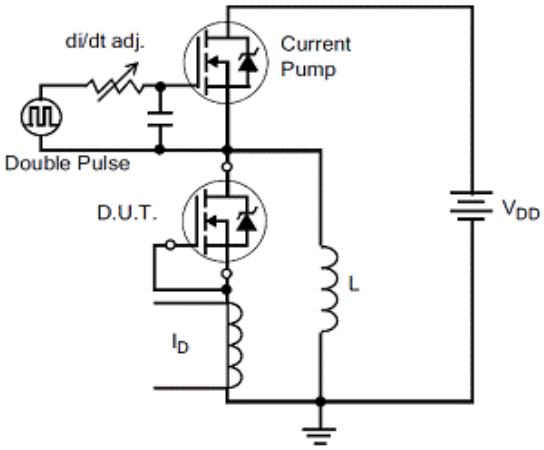


Figure 18. Diode Reverse Recovery Test Circuit

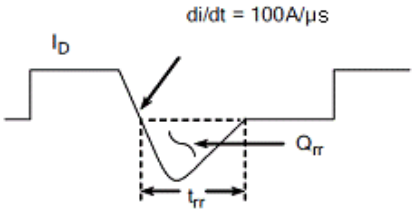


Figure 19. Diode Reverse Recovery Waveform

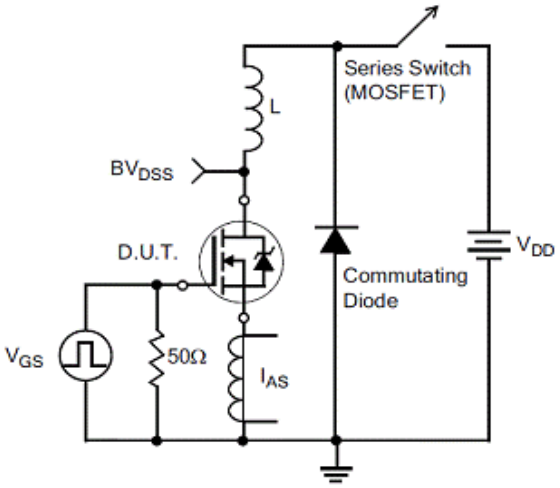


Figure20.Unclamped Inductive Switching Test Circuit

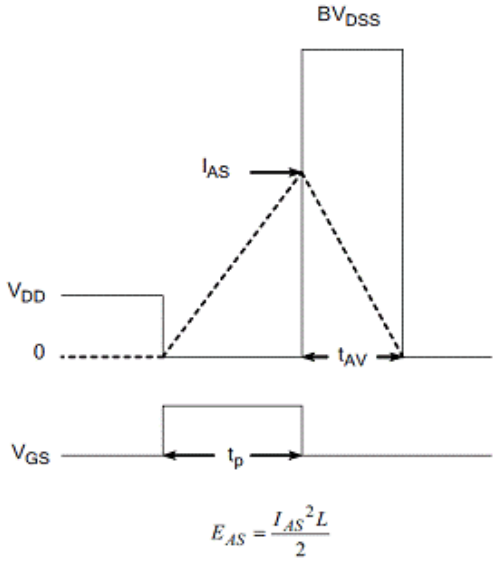
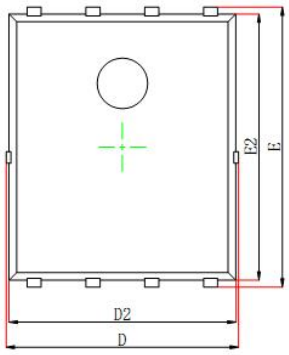
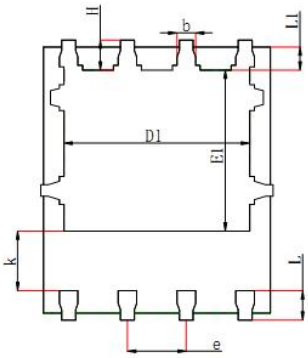


Figure21.Unclamped Inductive Switching Waveform

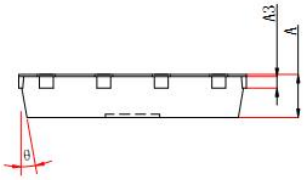
Package Information：



Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters	
	MIN	MAX
A	0.700	1.200
A3	0.254REF	
D	4.844	5.196
E	5.774	6.326
D1	3.810	4.210
E1	3.375	3.575
D2	4.724	5.076
E2	5.574	5.926
k	1.090	1.490
b	0.250	0.550
e	1.270TYP	
L	0.459	0.811
L1	0.424	0.576
H	0.474	0.826
θ	10°	12°

PDFN5×6 Package

The name and content of poisonous and harmful material in products

Part's Name	Hazardous Substance									
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE	DIBP	DEHP	DBP	BBP
Limit	≤ 0.1%	≤ 0.1%	≤ 0.01%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%
Lead Frame	○	○	○	○	○	○	○	○	○	○
Molding	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
Wire Bonding	○	○	○	○	○	○	○	○	○	○
Solder	×	○	○	○	○	○	○	○	○	○
Note	○: Means the hazardous material is under the criterion of 2011/65/EU. ×: Means the hazardous material exceeds the criterion of 2011/65/EU. The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup's RoHS.									

Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heatsink, please pay attention to the torsional moment and the smoothness of the heatsink.
3. VDMOSFETs is the device which is sensitive to the staticelectricity, it is necessary to protect the device from being damaged by thestaticelectricity when using it.
4. This publication is made by Huajing Microelectronics and subject to regularchange without notice.

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