

N-Channel Trench Power MOSFET

General Description

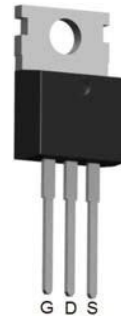
The CS55N53 is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged EAS capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching applications.

Features

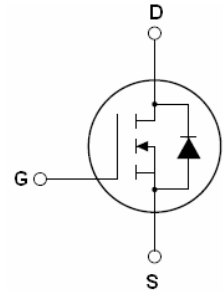
- $V_{DS}=55V$; $I_D=100A @ V_{GS}=10V$;
 $R_{DS(ON)} < 6.4m\Omega @ V_{GS}=10V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



To-220 Top View



Schematic Diagram

$$V_{DS} = 55V$$

$$I_D = 100A$$

$$R_{DS(ON)} = 5.0m\Omega$$

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
CS55N53	CS55N53	TO-220	-	-	-

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	55	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 20	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	100	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	70	A
$I_{DM(pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	400	A
dv/dt	Peak Diode Recovery Voltage	8.8	V/ns
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	120	W
	Derating Factor	0.8	W/°C
E_{AS}	Single Pulse Avalanche Energy (Note 2)	440	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, V_{DD}=33V, V_G=10V, I_D=45A$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	---	1.25	°C/W

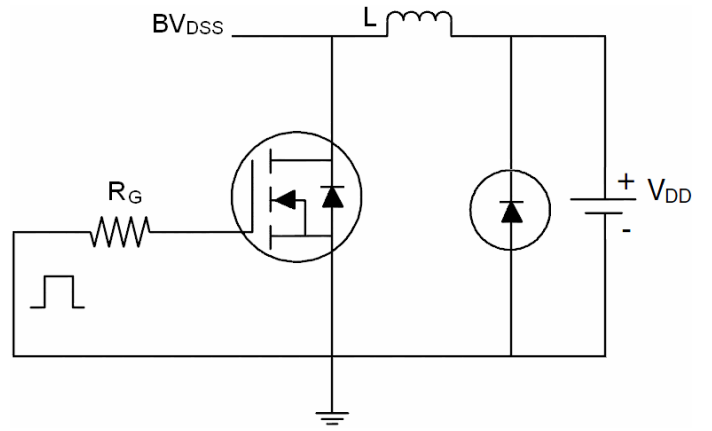
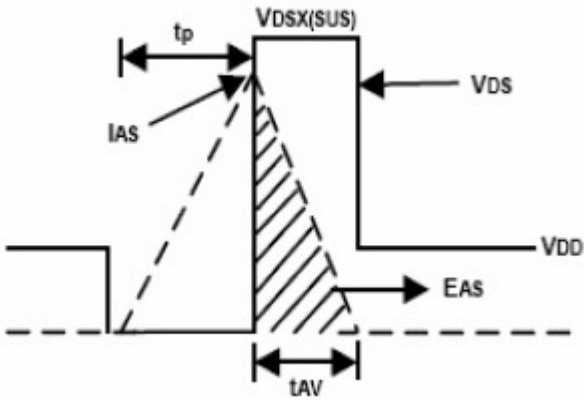
Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	55			V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25°C)	V _{DS} =68V, V _{GS} =0V			1	μA
I _{DSS}	Zero Gate Voltage Drain Current(Tc=125°C)	V _{DS} =68V, V _{GS} =0V			10	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±25V, V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1		2	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =40A		5.0	6.4	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =4.5V, I _D =4A		6.0	8.4	mΩ
Dynamic Characteristics						
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =15A	20			S
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		5538		pF
C _{oss}	Output Capacitance			380		pF
C _{riss}	Reverse Transfer Capacitance			304		pF
Q _g	Total Gate Charge	V _{DS} =50V, I _D =40A, V _{GS} =10V		102		nC
Q _{gs}	Gate-Source Charge			20		nC
Q _{gd}	Gate-Drain Charge			49		nC
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V, I _D =2A, R _L =15Ω V _{GS} =10V, R _G =2.5Ω		24		nS
t _r	Turn-on Rise Time			32		nS
t _{d(off)}	Turn-Off Delay Time			69		nS
t _f	Turn-Off Fall Time			31		nS
Source-Drain Diode Characteristics						
I _{SD}	Source-Drain Current(Body Diode)			100		A
I _{SDM}	Pulsed Source-Drain Current(Body Diode)			400		A
V _{SD}	Forward On Voltage ^(Note 1)	T _J =25°C, I _{SD} =40A, V _{GS} =0V		0.9	0.99	V
t _{rr}	Reverse Recovery Time ^(Note 1)	T _J =25°C, I _F =75A di/dt=100A/μs		28		nS
Q _{rr}	Reverse Recovery Charge ^(Note 1)				39	
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

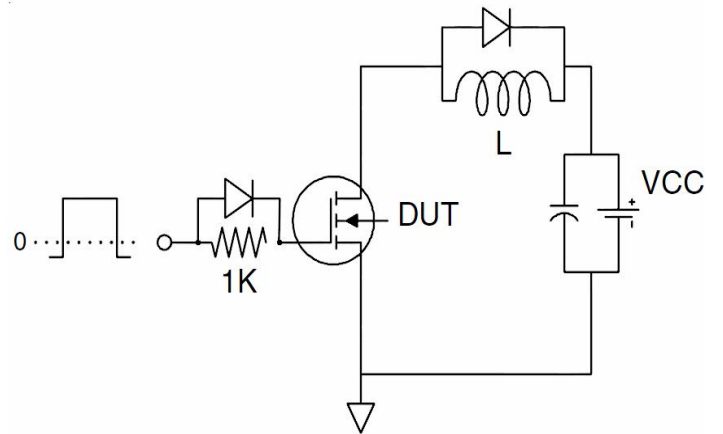
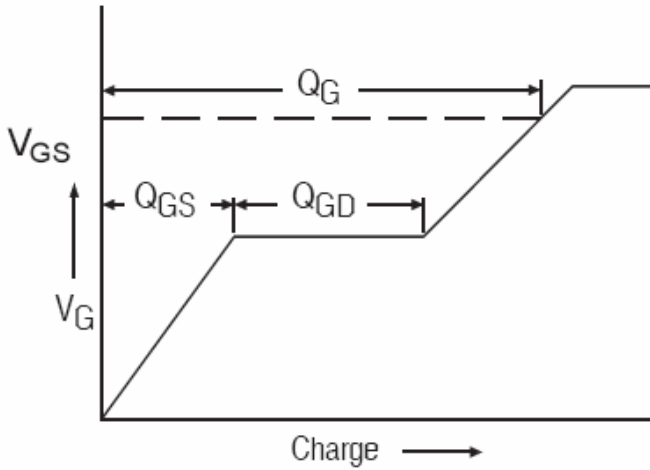
Notes 1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, R_G=25Ω, Starting T_J=25°C

Test Circuit

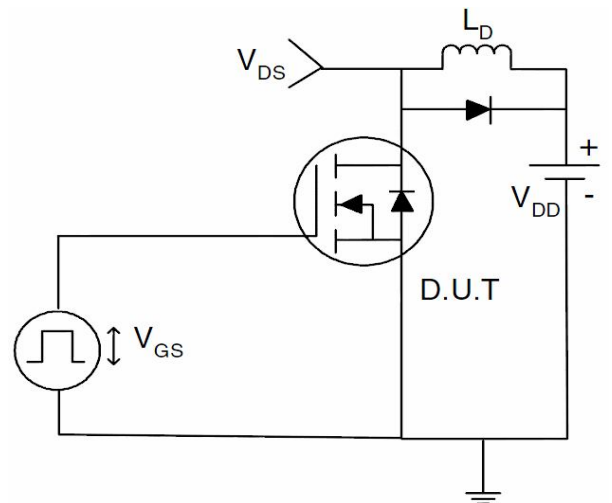
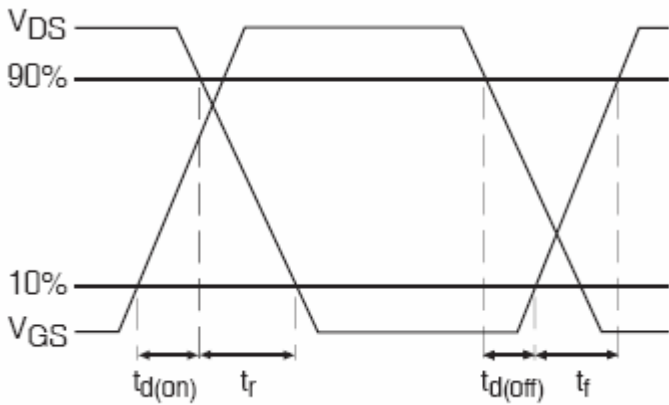
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

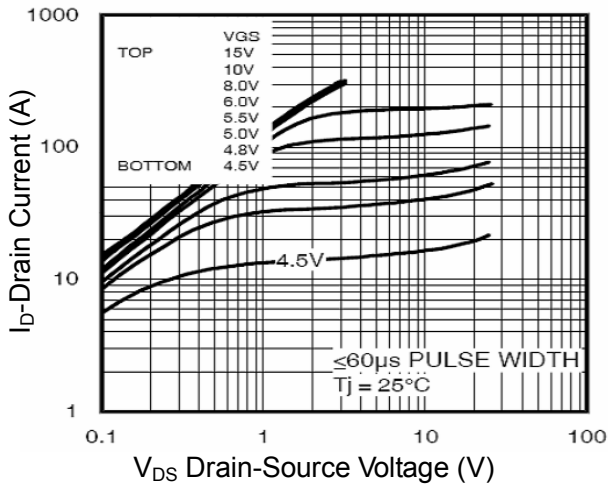


Figure2. Transfer Characteristics

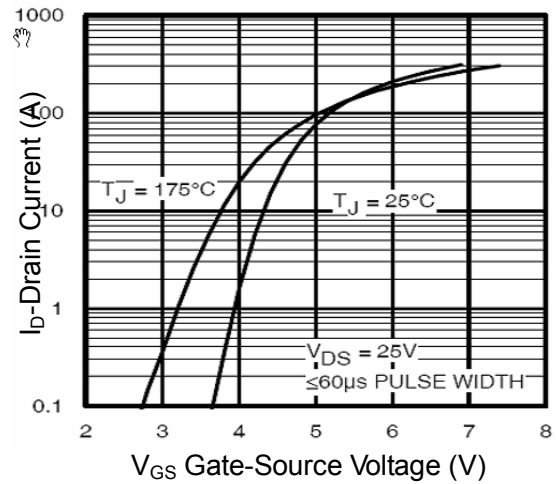


Figure3. BVDS vs Junction Temperature

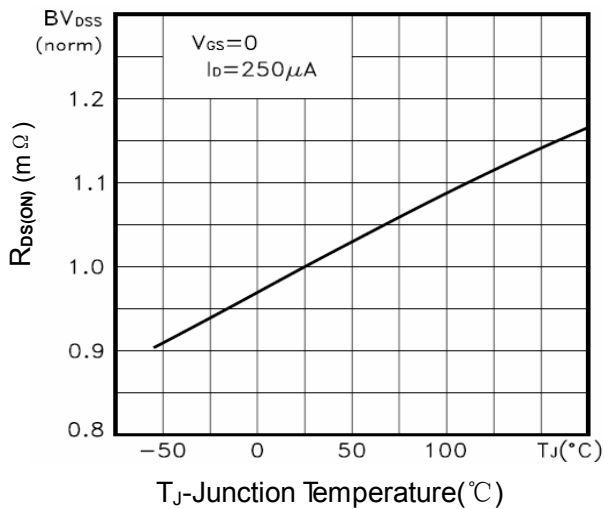


Figure4. ID vs Junction Temperature

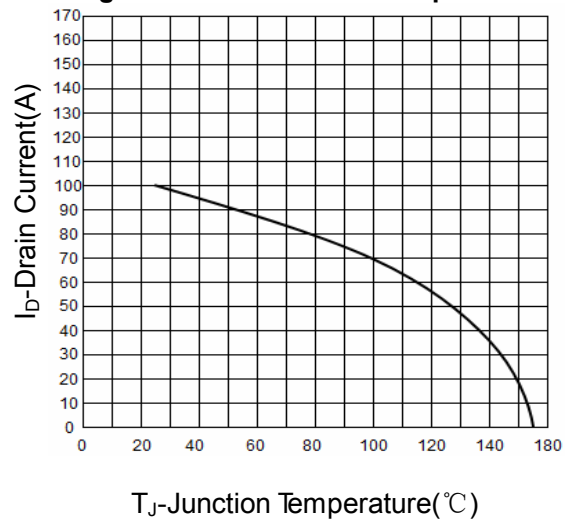


Figure5. Rds(on) Vs Junction Temperature

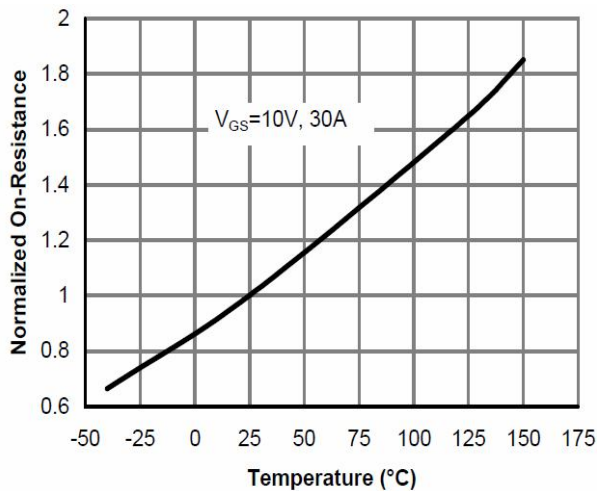


Figure6. VGS(th) vs Junction Temperature

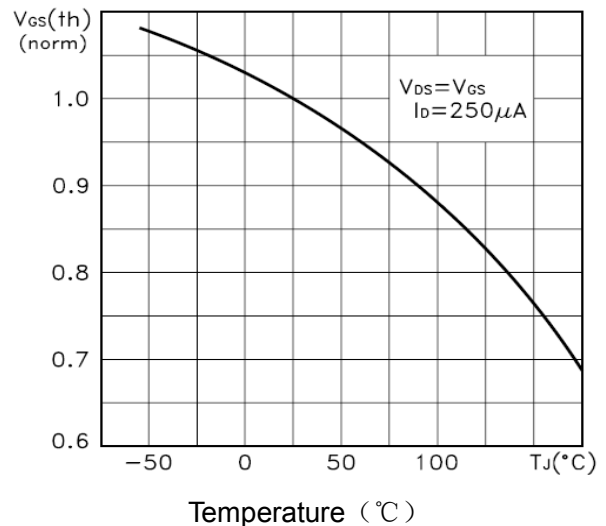


Figure7. Gate Charge

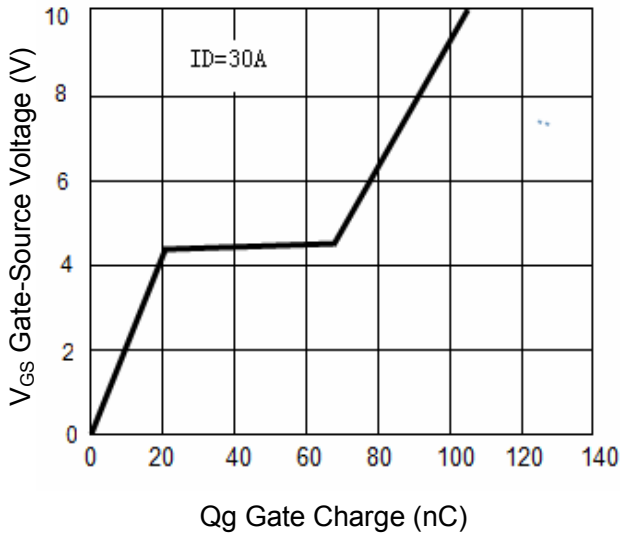


Figure8. Capacitance vs Vds

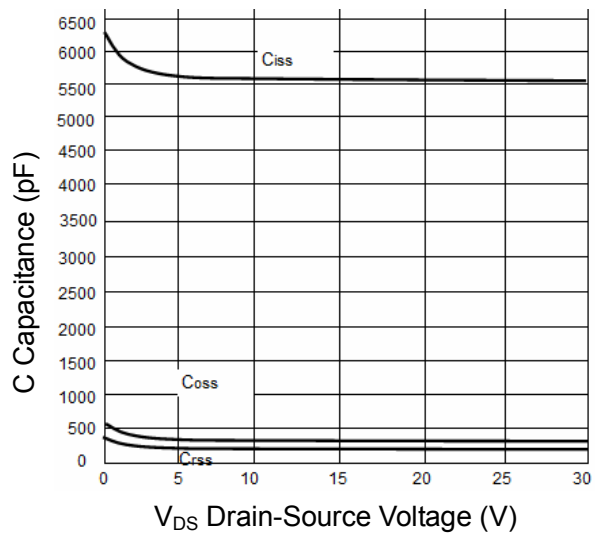


Figure9. Source- Drain Diode Forward

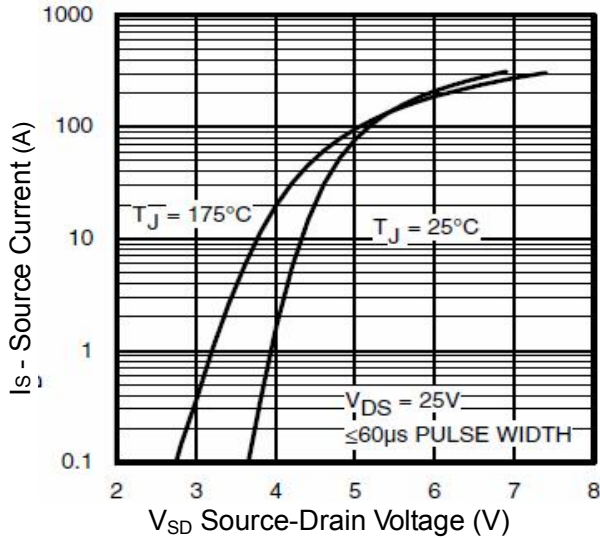


Figure10. Safe Operation Area

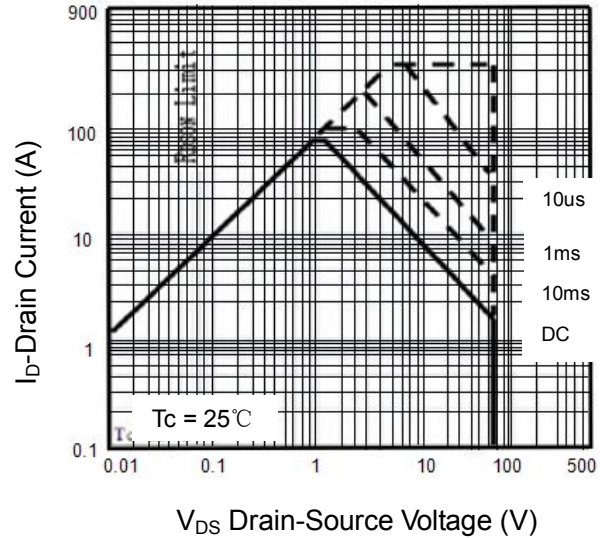
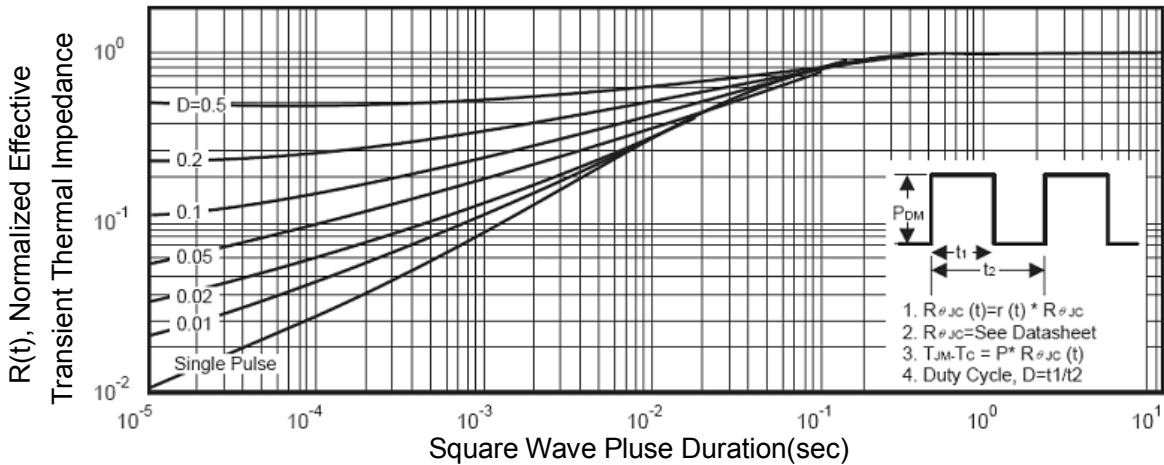
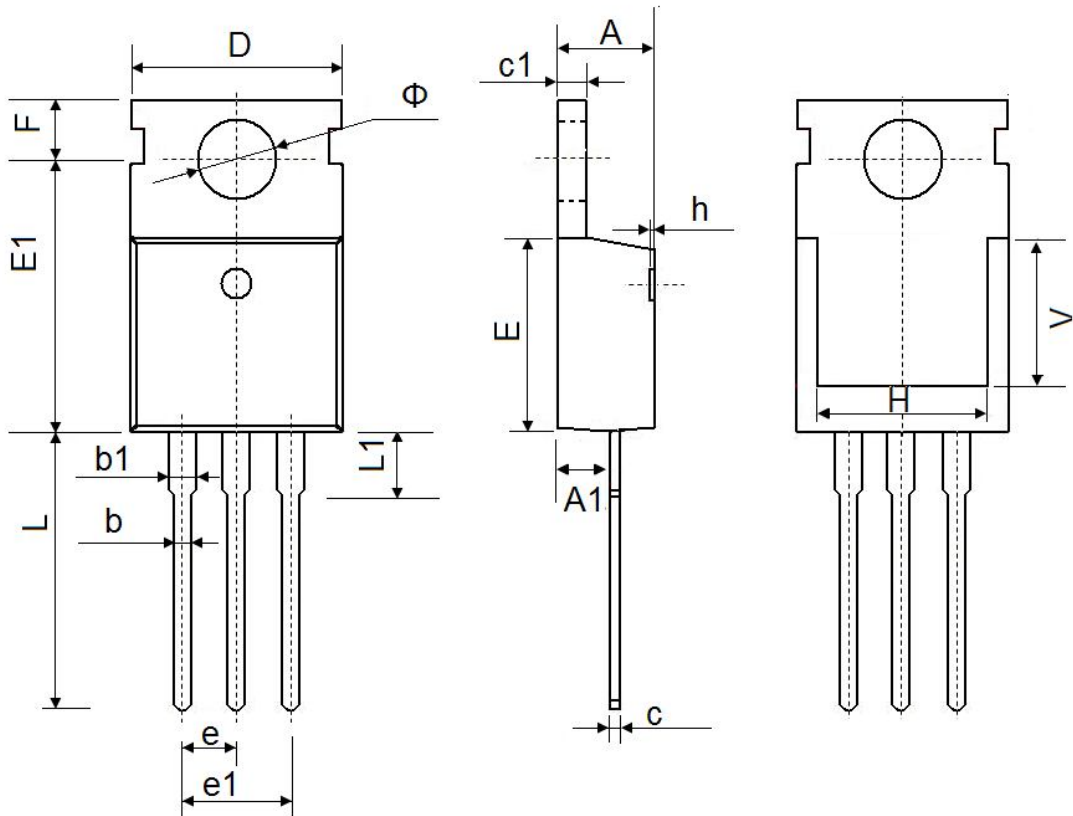


Figure11. Normalized Maximum Transient Thermal Impedance



TO-220 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.300	4.700	0.169	0.185
A1	2.200	2.600	0.087	0.102
b	0.700	0.950	0.028	0.037
b1	1.170	1.410	0.046	0.056
c	0.450	0.650	0.018	0.026
c1	1.200	1.400	0.047	0.055
D	9.600	10.400	0.378	0.409
E	8.8500	9.750	0.348	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.750	14.300	0.502	0.563
L1	2.850	3.950	0.112	0.156
V	7.500 REF.		0.295 REF.	
Φ	3.400	4.000	0.134	0.157