21:3 LVDS Transmitter

GENERAL DESCRIPTION

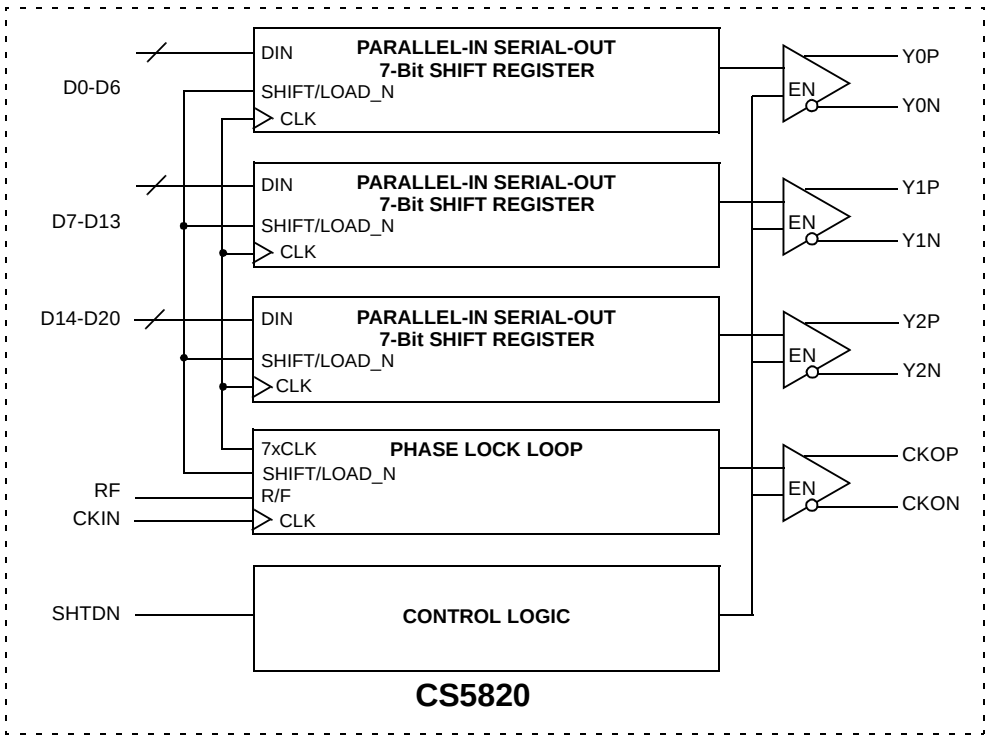
CS5820 receives three sets of 7-bit data in CMOS logic level and convert them into three low-voltage differential signaling (LVDS) serial channels. The 7-bit input data is referenced to the CKIN signal. The RF pin selects either rising or falling edge trigger of CKIN. Parallel to serial conversion is performed by a 7X internal generated clock reference using on-chip PLL using CKIN. A copy of CKIN but phase-locked to the output serial streams, CLKOUT, is also converted to the fourth LVDS channel. CS5820 offers a reliable communication media using LVDS signaling and provides low EMI dealing with wide, high-speed TTL interfaces.

This is especially attractive for interfaces between GUI controller and display systems such as LCD panels for SVGA/XGA/SXGA applications.

FEATURES

- Three 7-bit serial and one clock LVDS channels.
- Compatible with ANSI TIA/EIA-644 LVDS standard.
- Wide CKIN ranges from 31MHz to 68MHz.
- Fully integrated on-chip PLL that provides 7X CKIN serial shift clock.
- Pin selectable for rising or falling edge trigger.
- Support power-down mode.
- 5V/3.3V tolerant data input.
- Single 3.3V supply operation.
- CMOS low power consumption.
- Functional compatible with DS90C363 and SN75LVDS84.
- Available in 48-pin TSSOP package.

BLOCK DIAGRAM



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PIN CONNECTION DIAGRAM

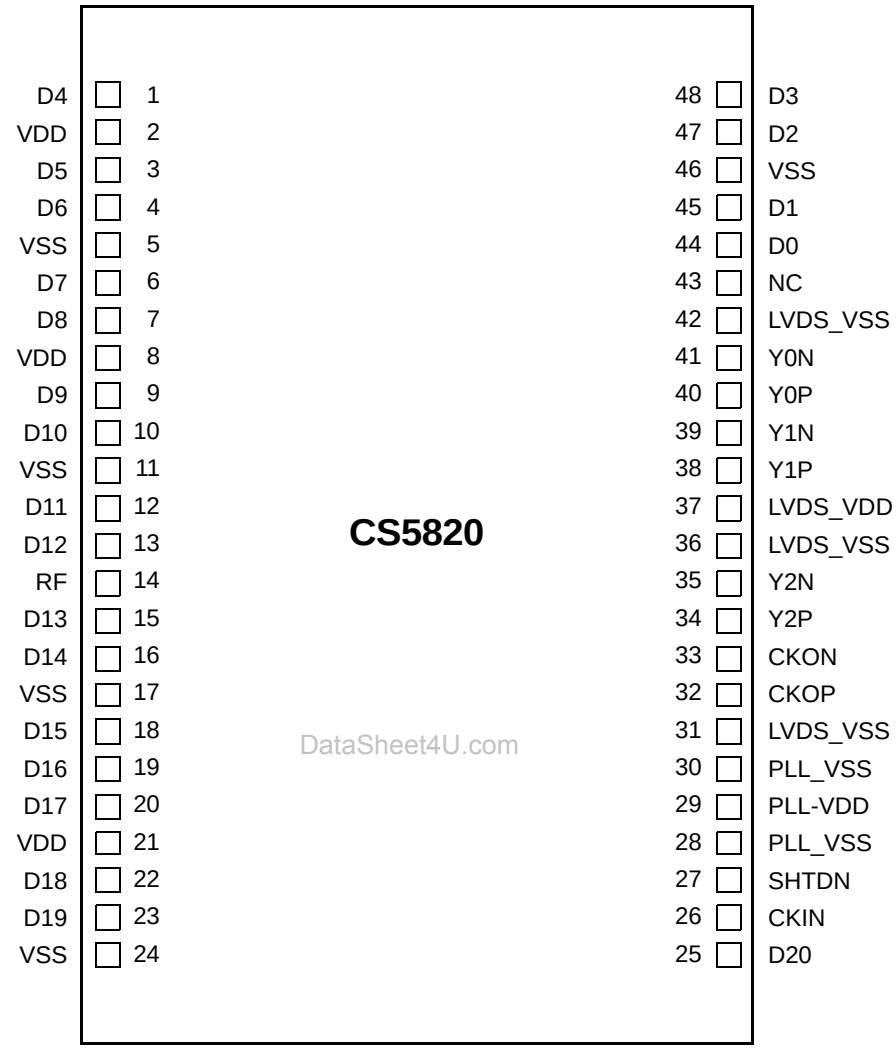


Figure-1 48-pin TSSOP

PIN DESCRIPTION

Name	I/O	Description
D[0-6]	I	Parallel data input for Y0 LVDS channel. D[0] is LSB and D[6] is MSB. MSB is shifted out first.
D[7-13]	I	Parallel data input for Y1 LVDS channel. D[7] is LSB and D[13] is MSB.
D[14-20]	I	Parallel data input for Y2 LVDS channel. D[14] is LSB and D[20] is MSB.
CKIN	I	Parallel input clock.This clock signal is used for parallel data reference. It is also used by the on-chip PLL to generate the 7X shift clock for parallel to serial conversion.
RF	I	Rise/fall select. This pin selects the polarity of the CKIN edge for data input. RF = 1 selects CKIN rise edge, and RF = 0 selects CKIN fall edge.
SHTDN	I	Shutdown control (low active). When SHTDN is low, the internal PLL is put into inhibit mode and all LVDS output channels are shut off. This also resets all internal registers. For normal operation, SHTDN should be set to high.
Y0P, Y0N	O	Y0 LVDS channel output. These are differential LVDS outputs for Y0 channel corresponds to D[0-6].
Y1P, Y1N	O	Y1 LVDS channel output. These are differential LVDS outputs for Y1 channel corresponds to D[7-13].
Y2P, Y2N	O	Y2 LVDS channel output. These are differential LVDS outputs for Y2 channel corresponds to D[14-21].
CKOP, CKON	O	Clock LVDS channel output. These are differential LVDS output for the replica of CKIN signal. CKOP and CKON are derived from the internal phase lock loop and phase aligned with the serial data output and can be used by the LVDS receiver for reference edge.
PLL_VDD	P	Power supply for PLL circuit.
PLL_VSS	P	Power ground for PLL circuit.
LVDS_VDD	P	Power supply for output buffer circuits.
LVDS_VSS	P	Power ground for output buffer circuits.
VDD	P	Power supply for internal circuits.
VSS	P	Power ground for internal circuits.

FUNCTIONAL DESCRIPTION

Control logic

There are two modes in this circuit. One is normal mode, and another is power down mode. Two modes are controlled by the control signal “SHTDN”. If SHTDN is high, the circuit is in the normal mode, else if low, the circuit is in the power down mode. In the power down mode, every block is off to make sure the least power consumption.

7 x CLK PLL

7 x CLK PLL, which is a phase lock loop, generates seven times clock of CKIN. The signal “RF” indicates that the input data (D0 ~ D20) is rising edge or falling edge trigger by CKIN. If RF=1, it is rigging edge trigger, else if RF=0, it is falling trigger. This seven times clock of CKIN is used by the Parallel ~ LOAD 7 Bit shift Register. 7 x CLK PLL also generate the control signal “SHIFT/LOAD”. This signal is also used by the Parallel ~ LOAD 7 Bit Shift Register to indicate when to load data or shift data.

Parallel ~ LOAD 7 Bit shift Register

This block transfers 7 bits parallel data into one bit series data out. It is controlled by SHIFT/$\overline{\text{LOAD}}$. If this control signal is low, the data are loaded into shift registers. Next, the SHIFT/$\overline{\text{LOAD}}$ turns high to shift data from shift register to output buffer seven times. One load and then seven shift.

Ref:

There are two properties in this block. One is that it supports reference voltage to fine the output’s common mode voltage. Another is that it generates about (4ns ~6ns) pulse width’s power on reset signal. When power on, all block would be reset by power on reset signal to make sure that the circuit would not stuck-at some situation we do not care.

Output buffer

There are three data output buffers and one clock output buffer. Output buffer generates differential pair output that swing is under 500 ~ 900mV, and common-mode voltage is under 1.125V ~ 1.375V.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2	-	-	V
V_{IL}	Low-level input voltage	-	-	0.8	V
Z_L	Differential load impedance	90	-	132	Ω
T_A	Operating free-air temperature	0	-	70	°C

TIMING REQUIREMENTS

Symbol	Parameter	Min	Typ	Max	Unit
t_C	Input clock period	14.7		32.4	ns
t_W	Pulse duration, high-level input clock	$0.4t_C$		$0.6t_C$	ns
t_t	Transition time, Input signal			5	ns
t_{su}	Setup time, data, D0~D20 valid before CKIN↓ (RF = 0) or CKIN↑(RF = 1)	3			ns
t_h	Hold time, data, D0~D20 valid after CKIN↓ (RF = 0) or CKIN↑(RF = 1)	1.5			ns

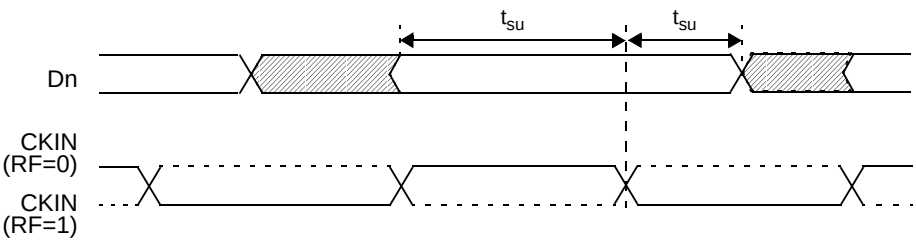
DC CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IT}	Input threshold voltage		-	1.4	-	V
$\lvert V_{OD} \rvert$	Differential steady-state output voltage magnitude	RL = 100Ω	247	340	454	mV
$\Delta \lvert V_{OD} \rvert$	Change in the steady-state differential output voltage magnitude between opposite binary states		-	10	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		1.125	-	1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		-	80	150	mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$	-	-	20	µA
I_{IH}-$\overline{SHTDN}$	High level input current for $\overline{SHTDN}$ pin	$V_{IH} = V_{CC}$	-	-	10	µA
I_{IL}	Low-level input current	$V_{IL} = 0$	-	-	±10	µA
I_{OS}	Short-circuit output current	$V_{O(Yn)} = 0$	-	-	±24	mA
		$V_{OD} = 0$	-	-	±12	mA
I_{OZ}	High-impedance output current	V_O = 0 to V_{CC}	-	-	±10	µA
$I_{CC(AVG)}$	Quiescent supply current (average)	Power down SHTDN = 0	-	-	250	µA
		Enabled, R_L = 100Ω (4 places) Gray_scale pattern V_{CC} = 3.3V, t_C = 15.38ns	-	40	60	mA
		Enabled, R_L = 100Ω (4 places) Worst_case pattern t_C = 15.38ns	-	50	75	mA
C_I	Input capacitance		-	3	-	pF

Note: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

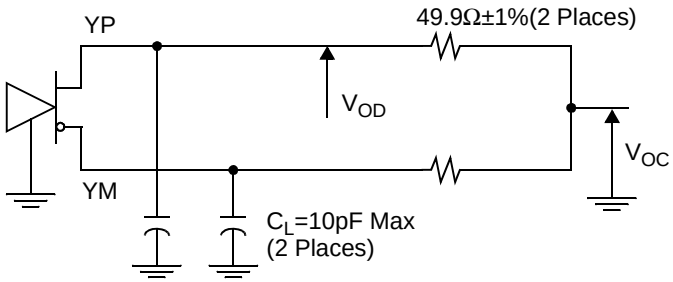
AC CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_0	CKO↑ to bit 0	T_c= 15.38 ns	-0.2	0	0.2	ns
t_1	CKO↑ to bit 1		$1/7t_c$-0.2	-	$1/7t_c$+0.2	ns
t_2	CKO↑ to bit 2		$2/7t_c$-0.2	-	$2/7t_c$+0.2	ns
t_3	CKO↑ to bit 3		$3/7t_c$-0.2	-	$3/7t_c$+0.2	ns
t_4	CKO↑ to bit 4		$4/7t_c$-0.2	-	$4/7t_c$+0.2	ns
t_5	CKO↑ to bit 5		$5/7t_c$-0.2	-	$5/7t_c$+0.2	ns
t_6	CKO↑ to bit 6		$6/7t_c$-0.2	-	$6/7t_c$+0.2	ns
t_{skew}	Output skew		-0.2	-	0.2	ns
$\Delta t_c(o)$	Cycle time, Output clock jitter		-	±100	-	ps
t_w	Pulse duration, high-level output clock		-	$4/7t_c$	-	ns
t_t	Transition time, differential output voltage (t_r or t_f)		260	700	1500	ps
t_{enable}	Enable time, SHTDN↑ to phase lock (Yn valid)		-	1	-	ms
$t_{disable}$	Disable time, SHTDN↓ to off state (CKO low)		-	250	-	ns

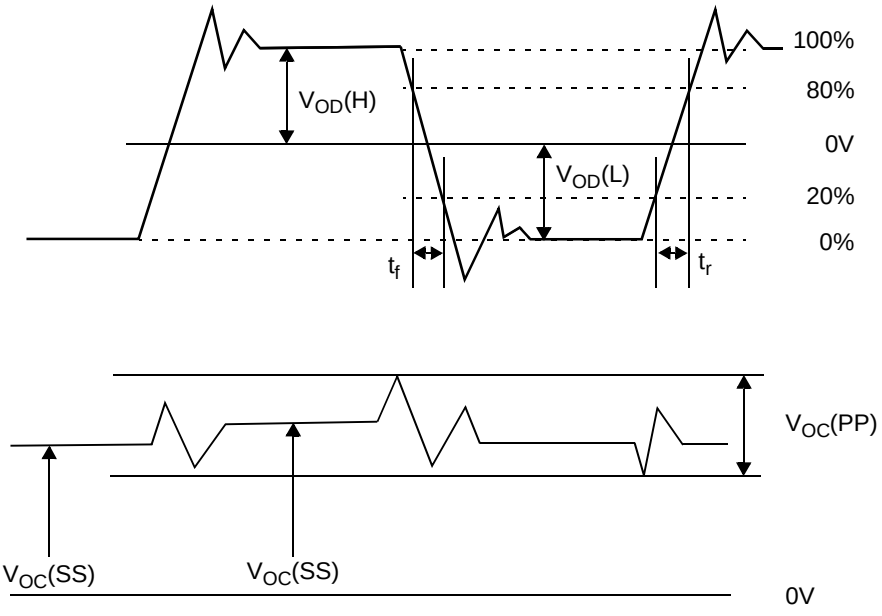


Note: Maximum value of t_r, t_f = 5ns

Figure-2 Setup and Hold Time Definition



(a) SCHEMATIC



(b) WAVEFORMS

Figure-3 Test Load and Voltage Definitions for LVDS Outputs

TEST PATTERN

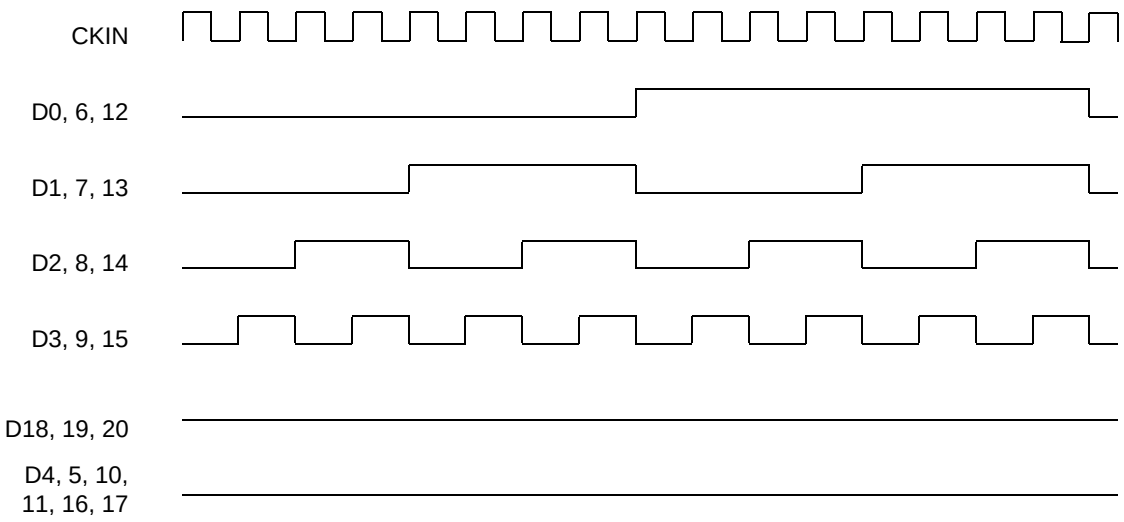


Figure-4 16-Grayscale Testing Pattern Waveforms

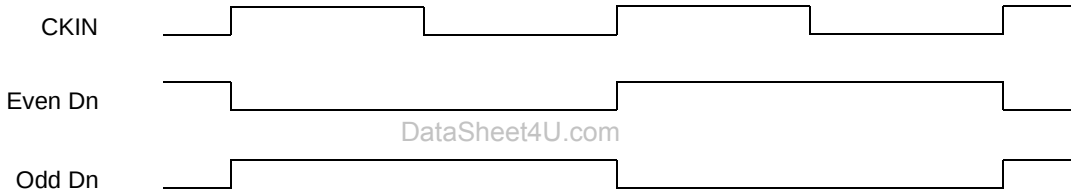


Figure-5 The Worst-case Testing Pattern Waveforms

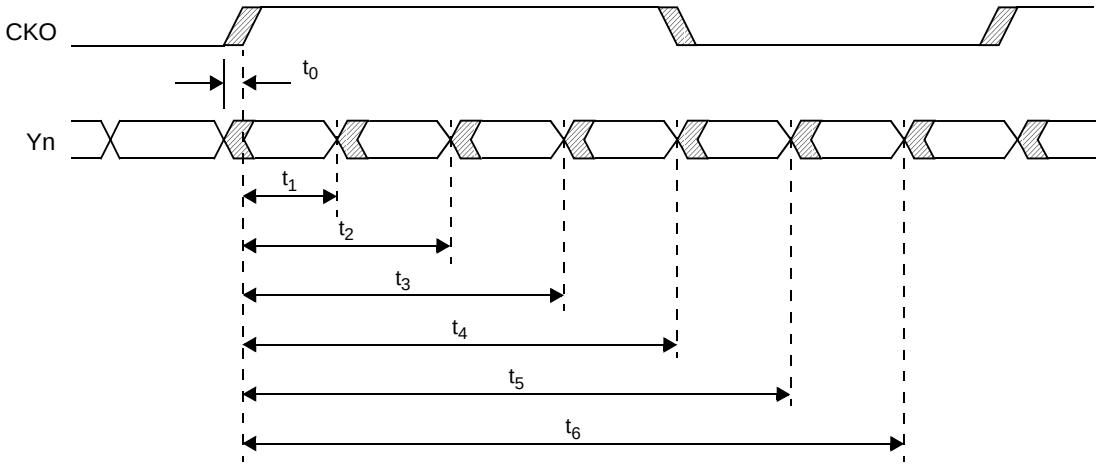
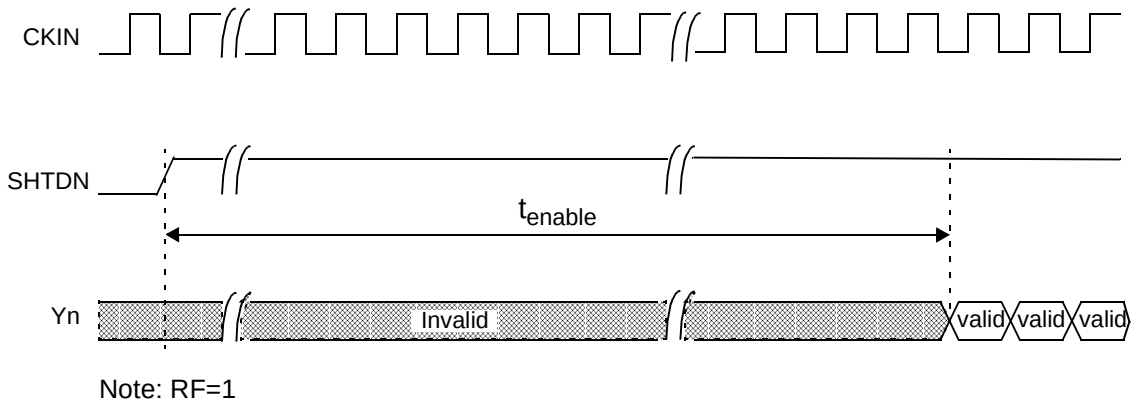


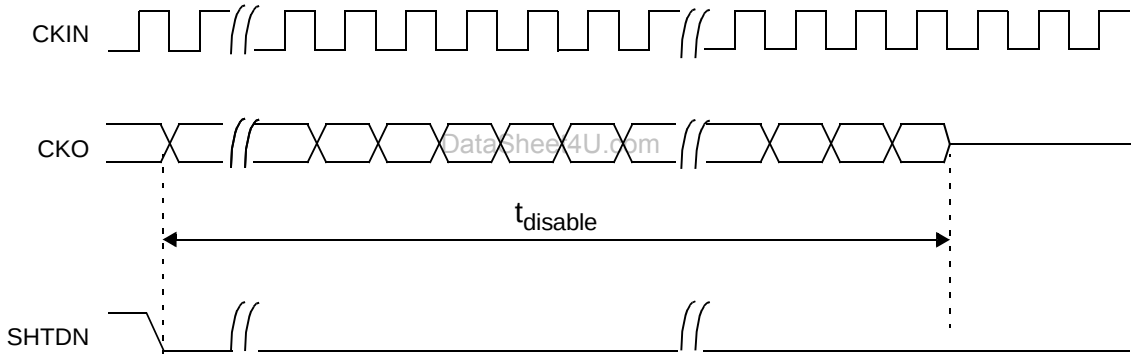
Figure-6 Timing Waveform's Definitions

TYPICAL CHARACTERISTICS



Note: RF=1

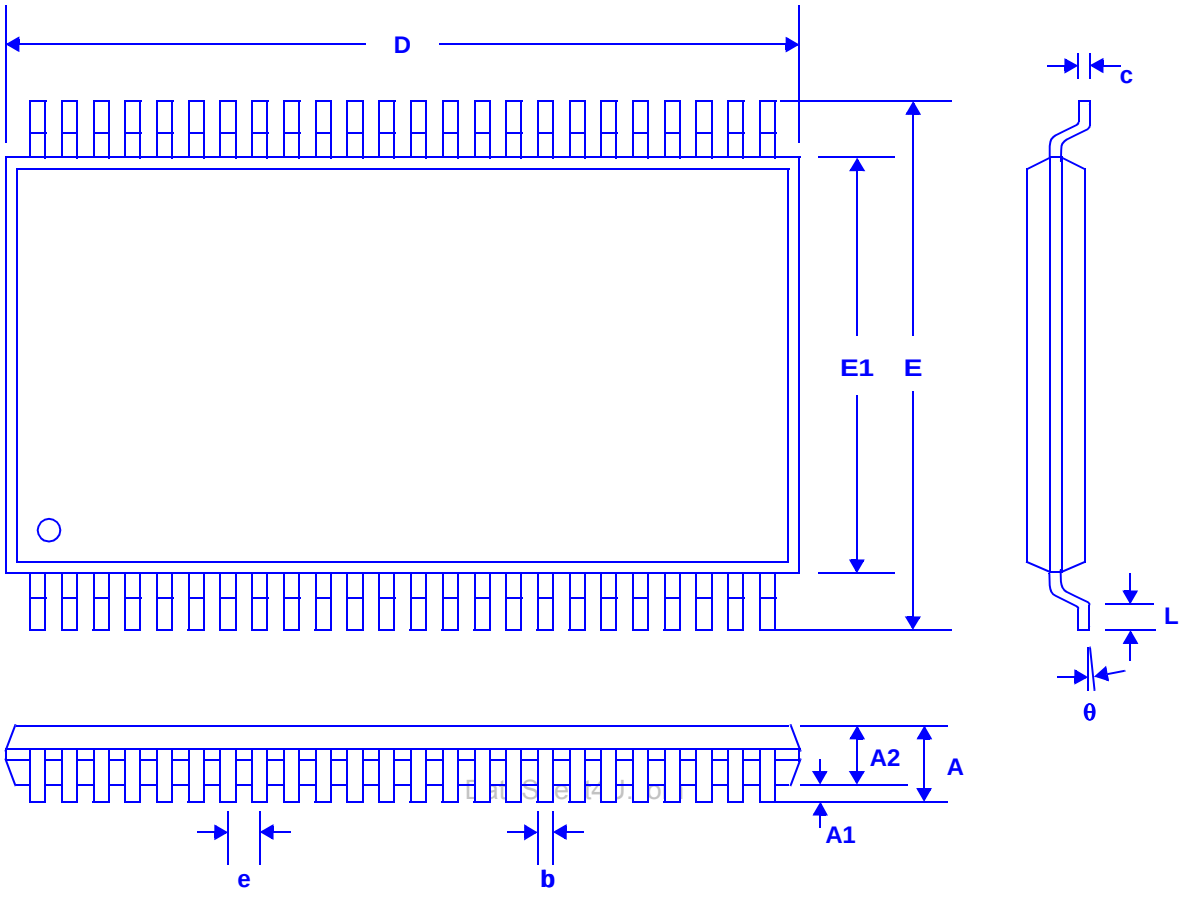
Figure-7 Enabled Time Waveforms



Note: RF=1

Figure-8 Disabled Time Waveforms

PACKAGE OUTLINE (48-pin TSSOP)



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	-	1.20	0.04	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	-	0.90	-	-	0.035	-
b	0.17	0.20	0.27	0.007	0.008	0.010
c	0.09	0.15	0.20	0.004	0.006	0.008
D	12.40	12.50	12.60	0.488	0.492	0.496
E	7.80	8.10	8.40	0.307	0.319	0.330
E1	6.00	6.10	6.20	0.236	0.240	0.244
e	-	0.50	-	-	0.0197	-
L	0.50	-	0.75	0.020	-	0.030
θ	0°	-	7°	0°	-	7°

APPLICATION CIRCUIT SCHEMATICS

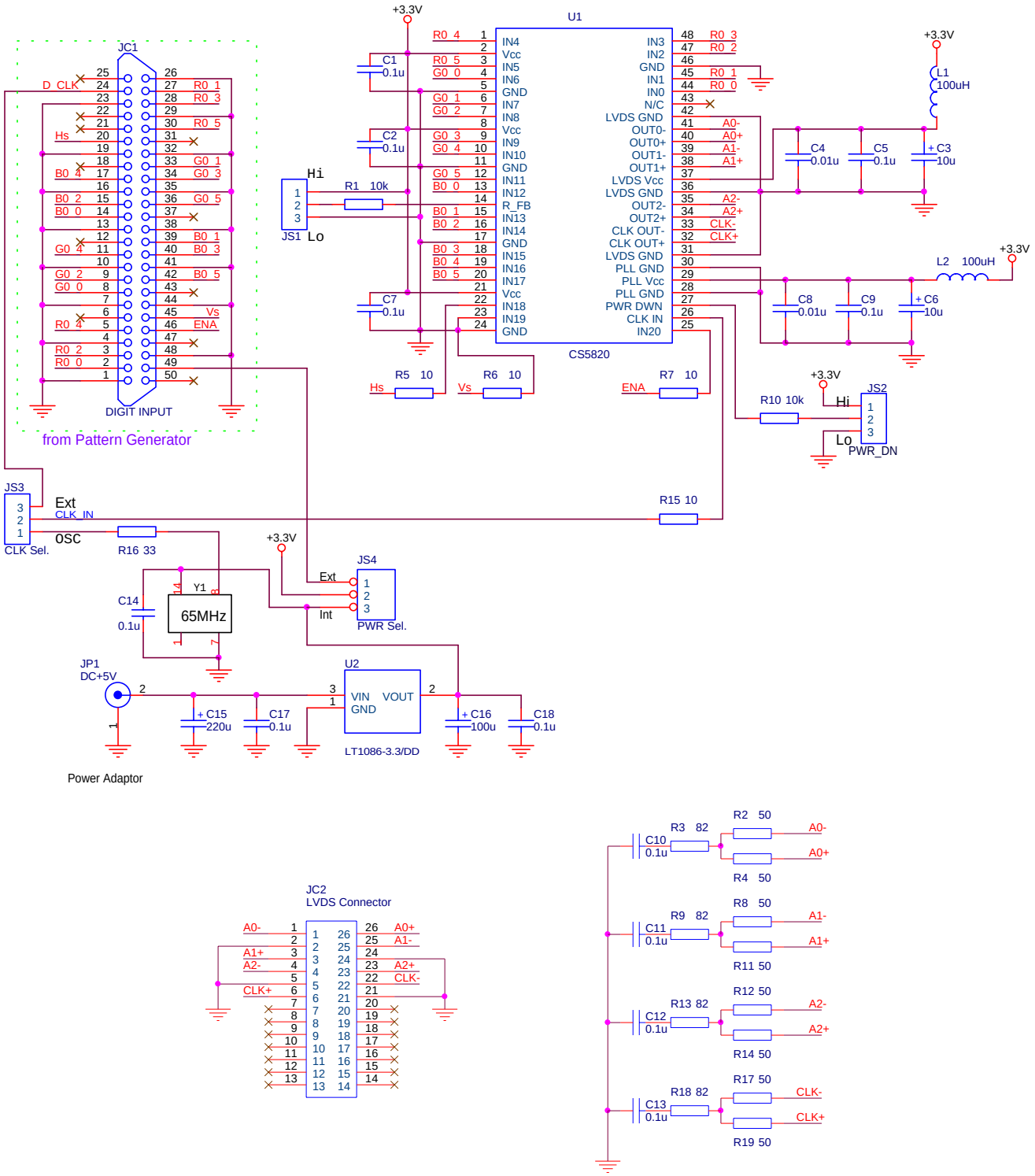


Figure-9 Using 48-pin TSSOP package