LCD Panel Timing Controller (14")

GENERAL DESCRIPTION

CS5841 is a TFT-LCD timing controller, which is applicable to 6-bit data XGA (1024*768), SXGA (1280*1024) and SVGA (800*600).

CS5841 can update the response timing for display mode of XGA, SXGA and SVGA automatically.

CS5841 provides a selectable polarity check function to inverse output data for EMI reducing,

FEATURES

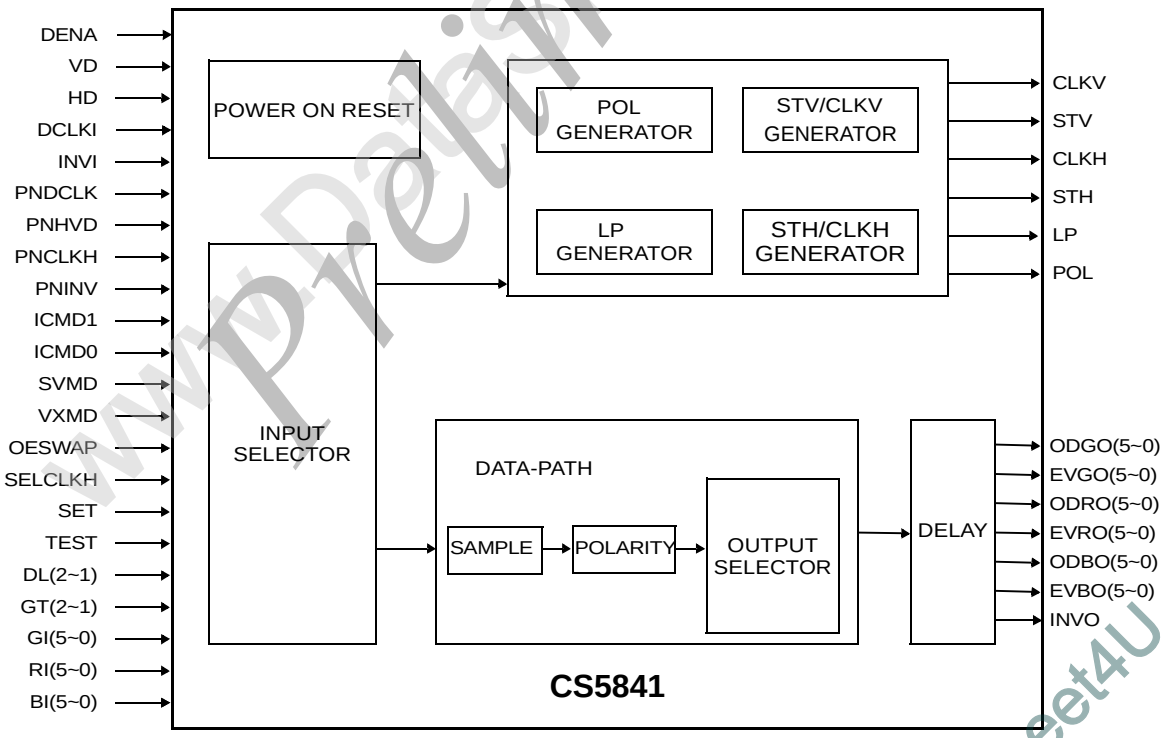
- Interface (5V/3.3V[CMOS] input, 3.3V[CMOS] output)
- 6-bit data single-port input, dual-port output.
- Timing adjustable for horizontal clock output
- Odd pixel, even pixel RGB data out switchable
- Correspondent to control timing & specific resolution for different Driver IC by changing a Mask:

FEATURES (continued)

1. can vary the pulse width & starting position of LP signal and POL signal polarity position changed along with LP signal
2. can vary the pulse width & starting position of CLKV signal and $CLKV_W$ time

- Control ASIC output timing design is based on Data Enable signals
- Resolution Auto detect for SVGA, XGA and SXGA
- Embedded Power On Reset circuits, Vth=2.1V, tolerance ± 0.3V
- ESD spec. 4KV
- Power On Latch Up 200mA/7.5V
- Single 3.3V supply
- 100-pin TQFP package (same as M65476BFP)

BLOCK DIAGRAM



Century Semiconductor, Inc.
Taiwan:
No. 2, Industry East Rd. 3rd,
Science-Based Industrial Park, Hsin-Chu, Taiwan
Tel: 886-3-5784866 Fax: 886-3-5784349

USA:
1485 Saratoga Ave. #200
San Jose, CA, 95129
Tel: 408-973-8388 Fax: 408-973-9388

Sales@century-semi.com
Sales@century-semi.com.tw
www.century-semi.com

PIN CONNECTION DIAGRAM

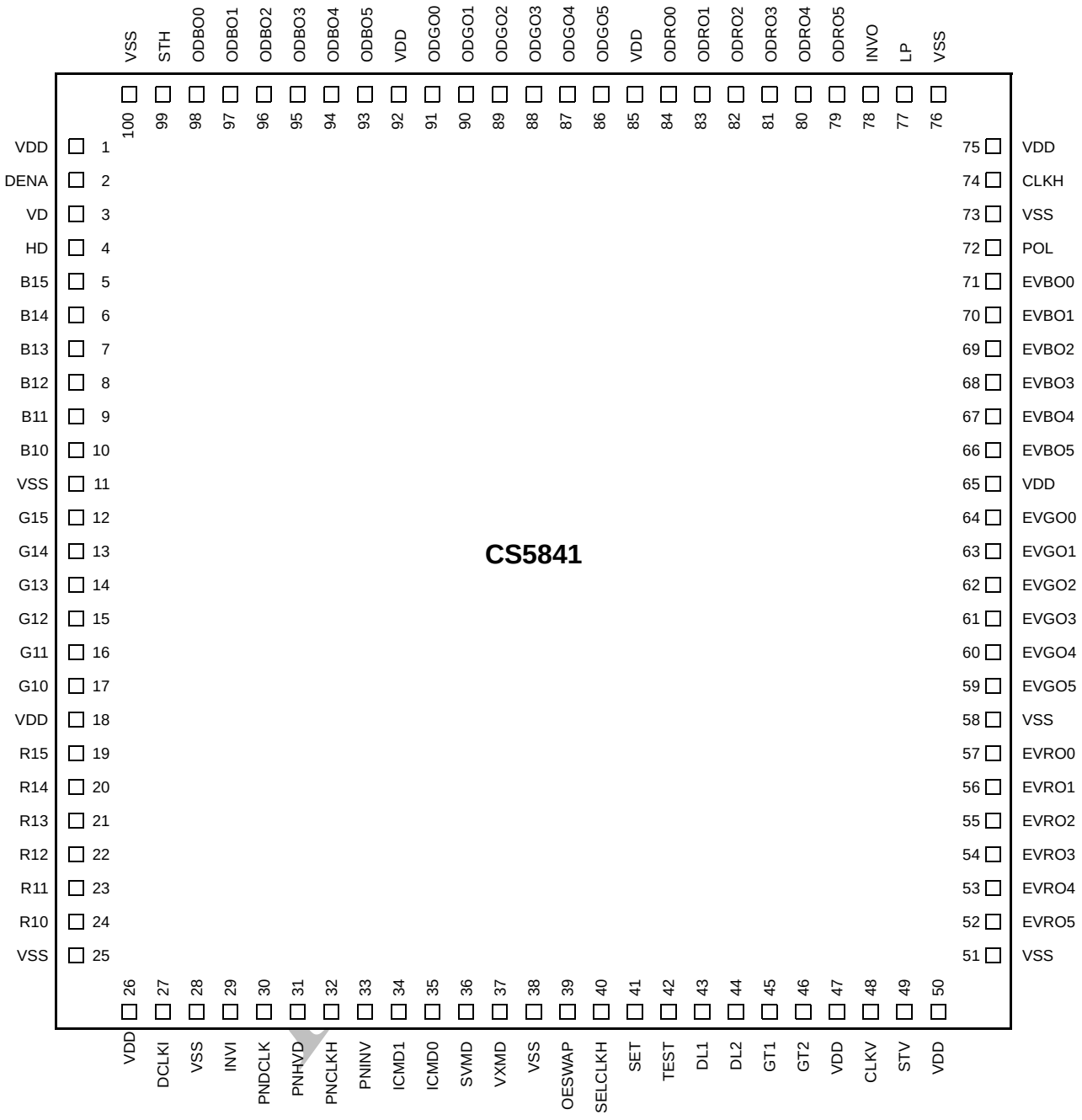


Figure-1 100-pin TQFP

PIN DESCRIPTION

Pin	I/O	Pin Count	Description	Note
DENA (Pin 2)	I	1	Data Enable input. “H” = Input data valid.	48.5KHz
VD (Pin 3)	I	1	Vertical sync signal input.	60Hz
HD (Pin 4)	I	1	Horizontal sync signal input.	48.5KHz
BI(0~5) Pin 10~5	I	6	Blue pixel data input.	32.5MHz
GI(0~5) Pin 17~12	I	6	Green pixel data input.	32.5MHz
RI(0~5) Pin 24~19	I	6	Red pixel data input.	32.5MHz
DCLKI (Pin 27)	I	1	Dot Clock input.	65MHz
INVI (Pin 29)	I	1	RGB data inverse control signal input “H” means RGB data input to ASIC has been inverted. “L” means non-inverted.	32.5MHz
PNDCLK (Pin 30)	I	1	Dot Clock (DCLK) polarity setting control input “L” = DCLK rising edge Latch input data. “H” = Falling edge Latch input data.	DC Pull-Up
PNHVD (Pin 31)	I	1	Horizontal & vertical sync signal polarity setting “L” means HD, VD are active low. “H” means HD, VD are active high.	DC Pull-Up
PNCLKH (Pin 32)	I	1	Setting latching edges for Source driver “L” = CLKH falling edge Latch output data. “H” = CLKH rising edge Latch output data.	DC Pull-Up
PNINV (Pin 33)	I	1	Polarity Function calculation set. “H” = calculated, “L”= un-calculated.	DC Pull-Up
ICMD1 (Pin 34)	I	1	Driver selection	DC Pull-Up
ICMD0 (Pin 35)	I	1		DC Pull-Up
SVMD (Pin 36)	I	1	No connection	DC Pull-Up
VXMD (Pin 37)	I	1	Data output buffer drive circuit switch select. “L” ⇒ I_{OL} = 4mA Normal. “H” ⇒ I_{OL} = 6mA Normal.	DC Pull-Up
OESWAP (Pin 39)	I	1	Odd pixel, even pixel RGB data output exchange select. “L” = ODD (RO, GO, BO) output even pixel RGB Data. EVEN (RO, GO, BO) output odd pixel RGB Data. “H” = ODD (RO, GO, BO) output odd pixel RGB Data. EVEN (RO, GO, BO) output even pixel RGB Data.	DC Pull-Up
SELCLKH (Pin 40)	I	1	CLKH output buffer drive circuit switch select. “L” ⇒ I_{OL} = 6mA Normal. “H” ⇒ I_{OL} = 10mA Normal.	DC Pull-Up

ICMD 1	ICMD0	Corresponding Driver IC
H	H	Hitachi HD66322
H	L	TI TMC57561 (Sharp L168)
L	L	Matsushita MN838814

Pin	I/O	Pin Count	Description	Note
SET (Pin 41)	I	1	ASIC internal reset setting input, is usually open.	DC Pull-Low
TEST (Pin 42)	I	1	TEST pin, usually open.	DC Pull-Low
DL(1~2) (Pin 43,44)	I	2	Adjust Clock Timing (CLKH) for Source Driver. 4 steps: 2.5ns each step, 0~7.5ns.	DC Pull-Up
GT(1~2) (Pin 45,46)	I	2	Adjust Clock Timing (CLKV) for Gate Driver. 4 steps: 0.5us each step, 1.5~3.0us.	DC Pull-Up
CLKV (Pin 48)	O	1	Output clock for Gate Driver. I_{OL} = 3mA Normal	48.5KHz 24pf
STV (Pin 49)	O	1	Output Start Pulse for Gate Driver input. I_{OL} = 3mA Normal	60Hz 66pf
EVRO(0~5) (Pin 57~52)	O	6	Red even pixel output. I_{OL} = 6mA Normal	16.25MHz 60pF
EVGO(0~5) (Pin 64~59)	O	6	Green even pixel output. I_{OL} = 6mA Normal	16.25MHz 60pF
EVBO(0~5) (Pin 71~66)	O	6	Blue even pixel output. I_{OL} = 6mA Normal	16.25MHz 60pF
POL (Pin 72)	O	1	Polarity reversed signal output for Source Driver output, used for Dot reversion. I_{OL} = 3mA Normal	24.25KHz 60pF
CLKH (Pin 74)	O	1	Output Clock for Source Driver. SELCLKH = "L" I_{OL} = 6mA Normal, SELCLKH = "H". I_{OL} = 10mA	32.5MHz 60pF
LP (Pin 77)	O	1	Source Driver output control. I_{OL} = 3mA Normal	48.5KHz 60pF
INVO (Pin 78)	O	1	DATA Polarity control signal output. "H" means ASIC output RGB data has been reversed. "L" means unreversed. I_{OL} = 6mA Normal	16.25MHz 60pF
ODRO(0~5) (Pin 84~79)	O	6	Red odd pixel output. I_{OL} = 6mA Normal	16.25MHz 60pF
Pin	I/O	Pin Count	Description	Note
ODGO(0~5) (Pin 91~86)	O	6	Green odd pixel output. I_{OL} = 6mA Normal	16.25MHz 60pF
ODBO(0~5) (Pin 98~93)	O	6	Blue odd pixel output. I_{OL} = 6mA Normal	16.25MHz 60pF
STH (Pin 99)	O	1	Source Driver IC Start Pulse output. I_{OL} = 3mA Normal	48.5KHz 60pF
VDD(Pin 1, 18, 26, 47, 50, 65, 75, 85, 92)	V		Supply 3.3V ± 10%.	
VSS (Pin 11, 25, 28, 38, 51, 58, 73, 76, 100)	G		GND.	

Operating Environment

Maximum operating frequency: 80MHz
Clock duty: 50 ±10%
Voltage range: 3.3 ± 0.3V
Operating temperature range: -25~75°C (storage temperature range: -55~150°C).

ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings:

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power supply	-0.3		6.0	V
V_I	Signal input voltage	-0.3	-	V_{CC}+0.3	V
V_O	Signal output voltage	-0.3	-	V_{CC}+0.3	V
T_A	Operating ambient	-25	-	85	°C
T_{STG}	Storage temperature	-55	-	150	°C
P_{PD}	Power dissipation	-	-	1	Ω

Note: The component will be damaged if exceed the absolute maximum condition. Normal function operating condition is as below:

2. Normal operating condition:

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supporting voltage	3.0	3.3	3.6	V
T_A	Operating ambient	0	25	75	°C

Note: Under normal operation, the function of ASIC IC must be normal.

3. DC Characteristic
Signal DC specification (according to normal operating condition)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output voltage high		2.4	-	-	V
V_{OL}	Output voltage low		-	-	0.2	V
I_{IL}	Input leakage current		-10	-	10	µA
I_{OL}	Output leakage current	High impedance	-100	-	100	µA
I_{OH}	Output High current (CCK)	$V_{OUT}=V_{OH}$				mA
I_{OL}	Output Low current (CCK)	$V_{OUT}=V_{OL}$		6(10)		mA
I_{OH}	Output High current (all others)	$V_{OUT}=V_{OH}$				mA
I_{OL}	Output Low current (all others)	$V_{OUT}=V_{OL}$		6		mA
I_{CCR}	Current consumption @3.3V V_{CC}	DCLK=65MHz	-	80	100	mA
I_{PD}	Power off current	Note 1			1.2	mA

Note: 1. Power off minimum current, all inputs must be V_{CC} or GND.

Note: 2. Testing consumption current I_{CCR} Output cascade 1kΩ & 60pF capacitor (one end grounded).

Input Timing Specificaiton

Symbol	Item	Specification			Unit
		Min	Typ	Max	
	Input Clock	-	65	80	MHz
t(DCLKI)	Input Clock period	12		-	ns
twL(DCLKI)	Input Clock High time	5	-	-	ns
twH(DCLKI)	Input Clock Low time	5	-	-	ns
tst(DI)	Input Data Setup time	3	-	-	ns
thd(DI)	Input Data Hold time	2	-	-	ns
tst(INVI)	Input Data reverted control signal Setup time	3	-	-	ns
thd(INVI)	Input Data reverted control signal Hold time	2	-	-	ns
tst(DENA)	Input Data Enable Setup time	3	-	-	ns
thd(DENA)	Input Data Enable Hold time	2	-	-	ns
tst(HD)	Horizontal Sync signal Setup time	3	-	-	ns
thd(HD)	Horizontal Sync signal Hold time	2	-	-	ns
tst(VD)	Vertical Sync signal Setup time	3	-	-	ns
tht(VD)	Vertical Sync signal Hold time	2	-	-	ns
tbh(DENA)	Input Data Enable width (“H”)	800	1024	1280	CLK
	Input Data Enable horizontal Blanking time	50	-	-	CLK
	Horizontal Sync signal width (“L”)	1	-	-	CLK
	Horizontal front porch	0	-	-	CLK
	Horizontal pack porch	1	-	-	CLK
	Input Data vertical Blanking time	3	-	-	H
	Vertical Sync signal width (“L”)	1	-	-	H
	Vertical front porch	2	-	-	H
	Vertical pack porch	1	-	-	H

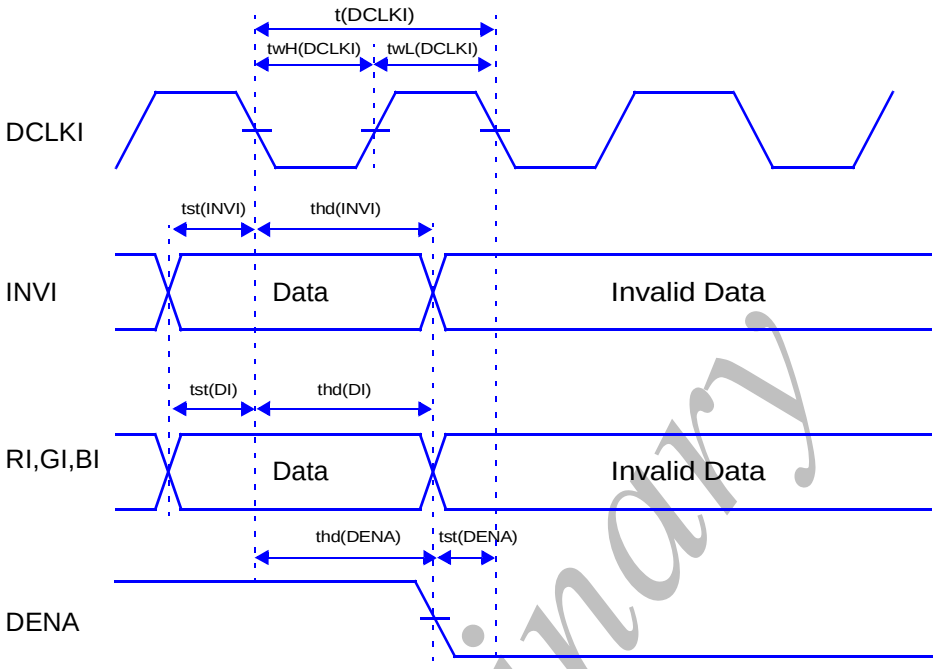


Figure-2

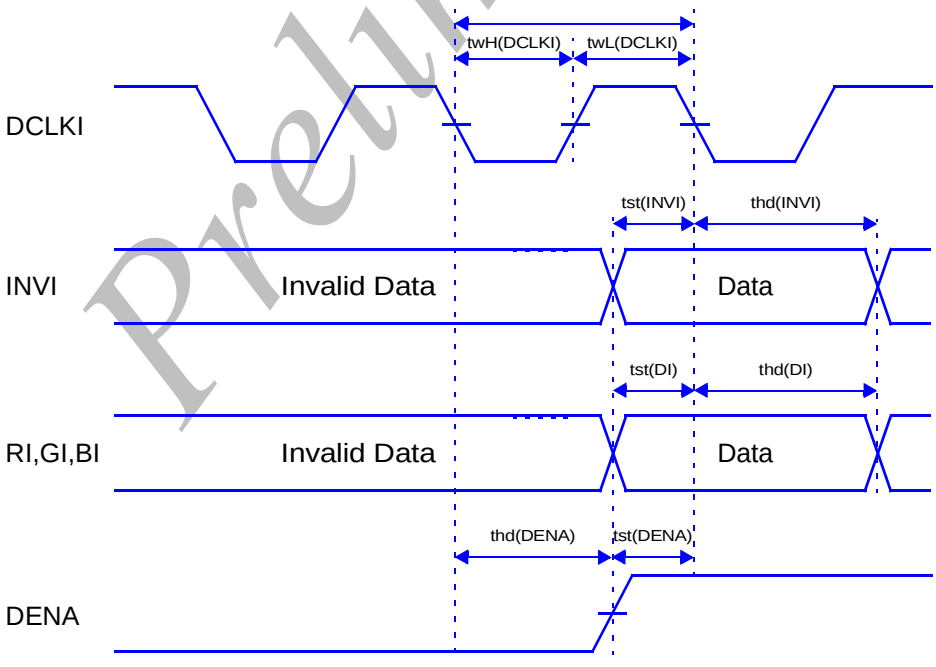


Figure-3

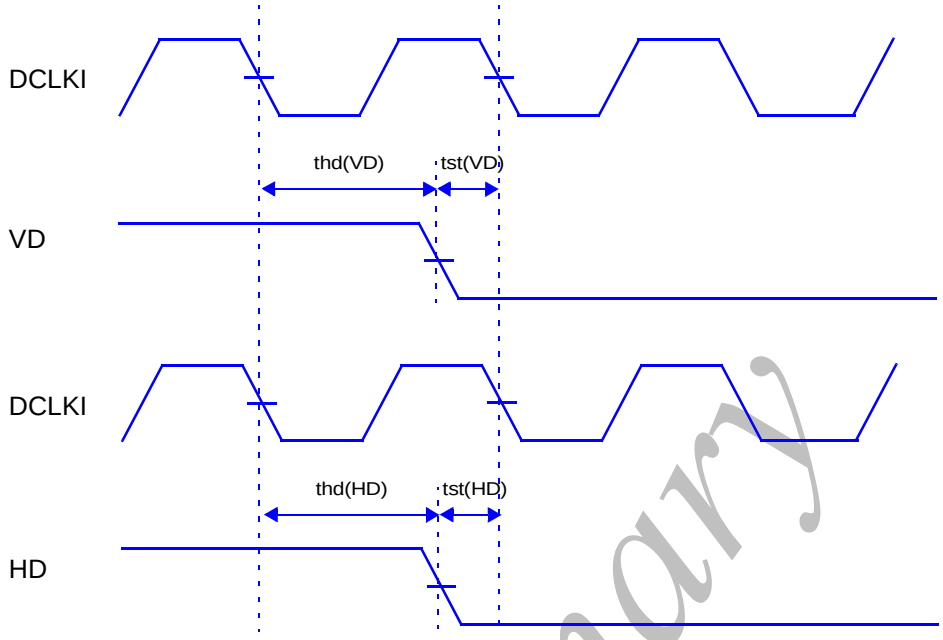


Figure-4

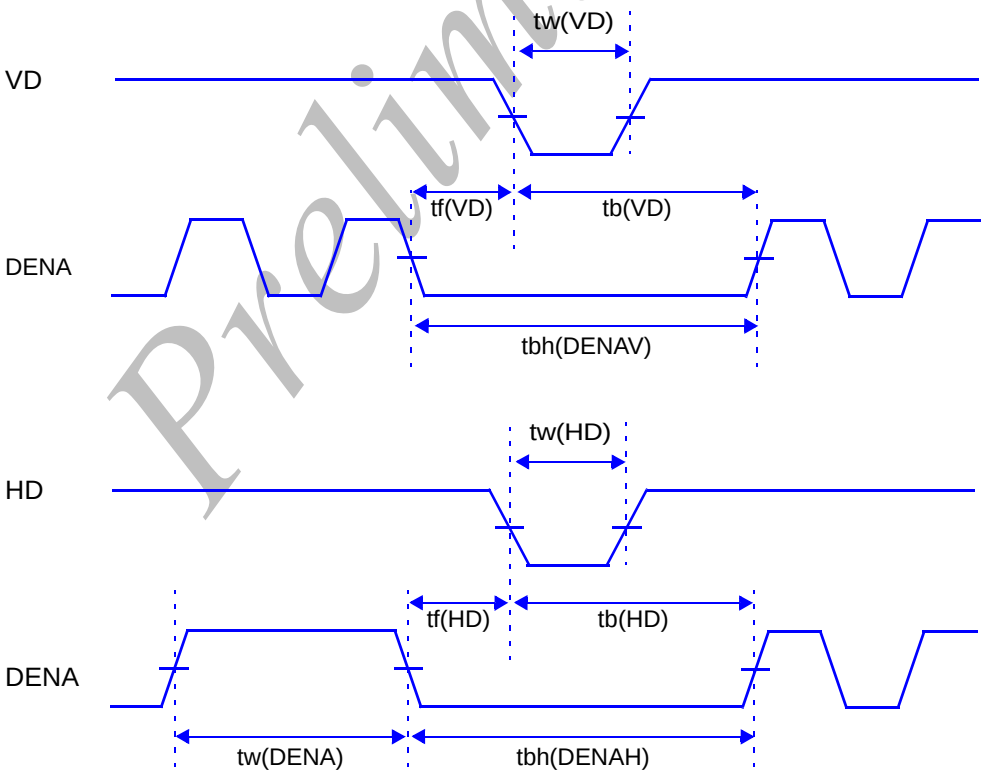


Figure-5

Horizontal Output Specification 1-1

ICMD0 = ”H”(OPEN)-Hitachi HD66322 PNDCLK, PNHVD = ”H”, PNCLKH = ”L”, ICMDI = ”H”(OPEN)

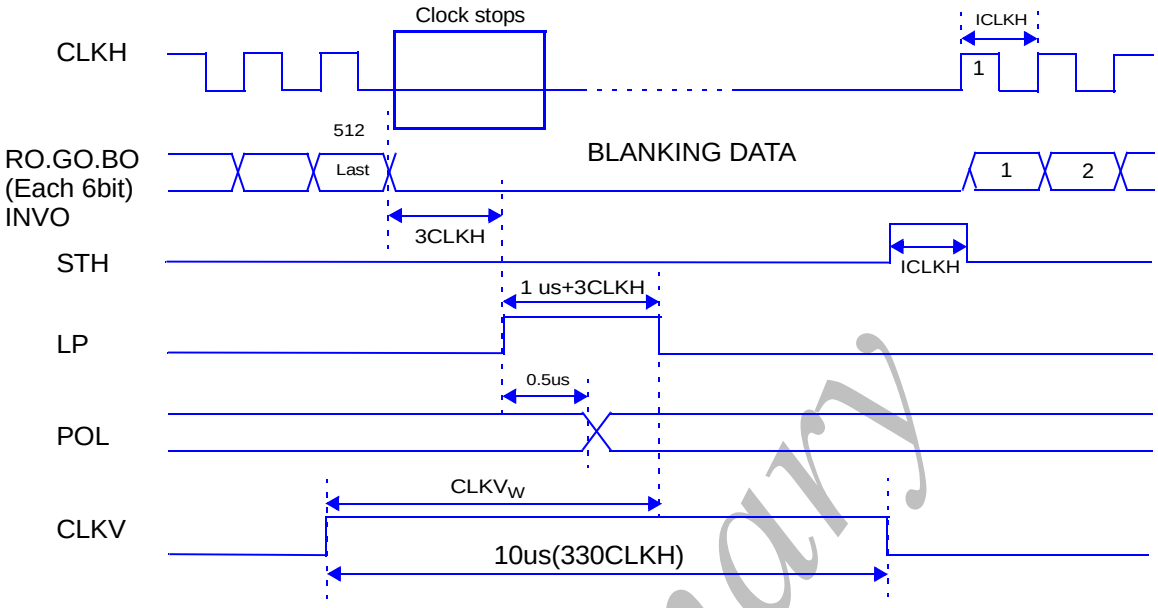


Figure-6

$CLKV_W$: 1.5us ~3.0us (0.5us pitch)

$CLKV_W$ = 1.5us GT2 = L, GT1 = L $CLKV_W$ = 2.0us GT2 = L, GT1 = H.
$CLKV_W$ = 2.5us GT2 = H, GT1 = L $CLKV_W$ = 3.0us GT2 = H, GT1 = H.
Note: 1us = 33CLKH = 66DCLK, at 65MHz: input Clock.

Horizontal Output Specification 1-2

ICMD0 = ”L”(TI TMS57561) PNDCLK, PNCLKH, PNHVD = ”H”, ICMDI = "H"

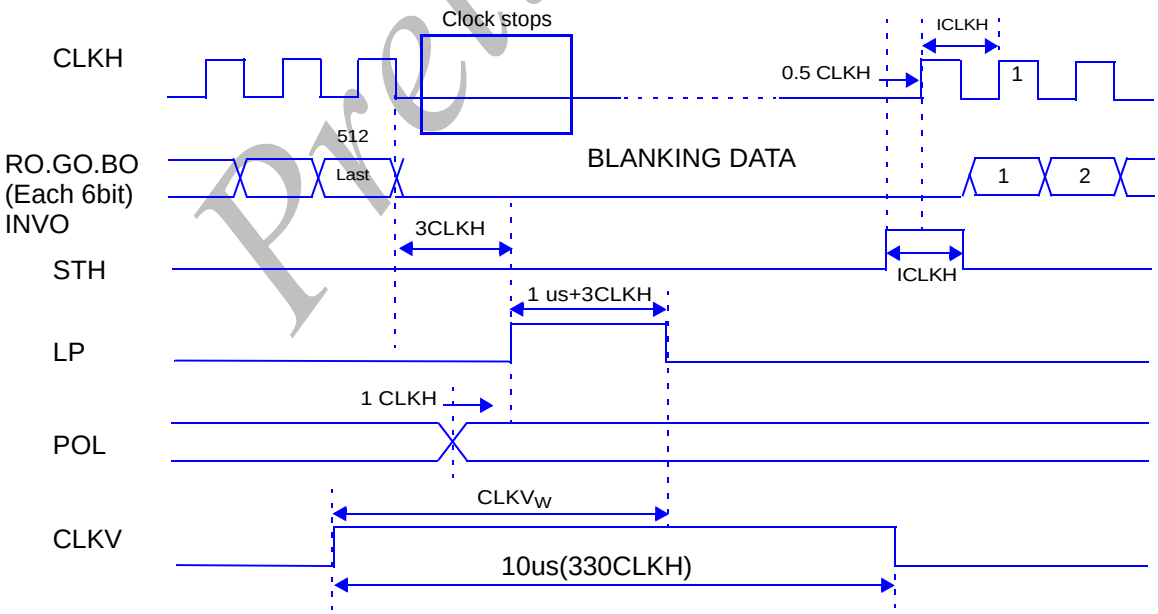


Figure-7

Horizontal Output 1-3

ICMD0="L--(**Matsushita MN838814**) PNDCLK, PNCLKH, PNHVD="H", ICMDI="L

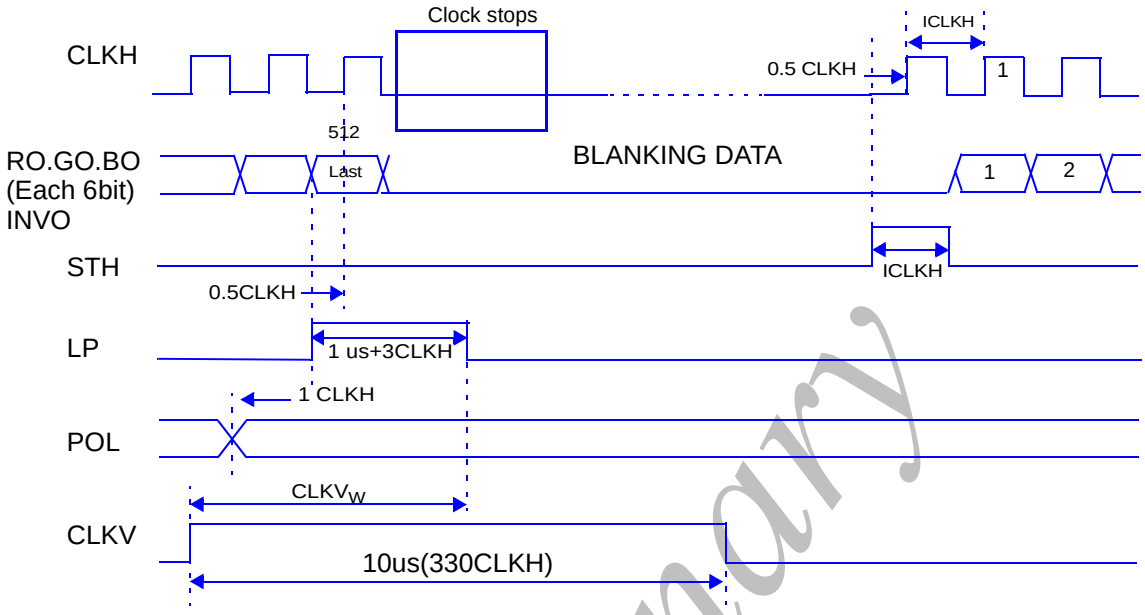


Figure-8

Horizontal Output 2-1 (Data output specification)

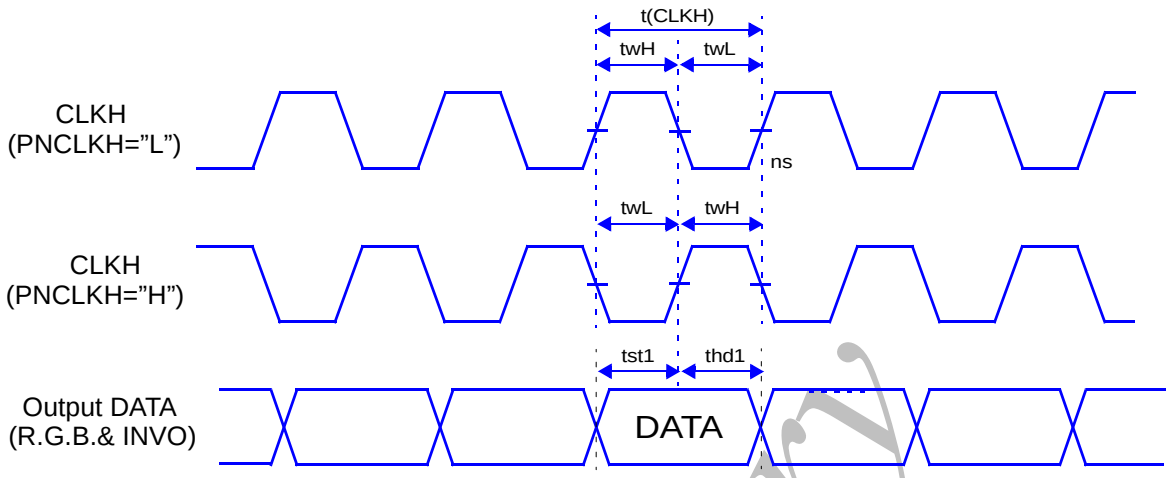


Figure-9

Symbol	Item	Specification			Unit
		Min	Typ	Max	
t(Clkh)	Horizontal output Clock period	25			ns
twh	Horizontal output Clock High time	10			ns
twL	Horizontal output Clock Low time	10			ns
tst1	Output data Set-up time	6			ns
thd1	Output data Hold time	6			ns

Vertical Output specification

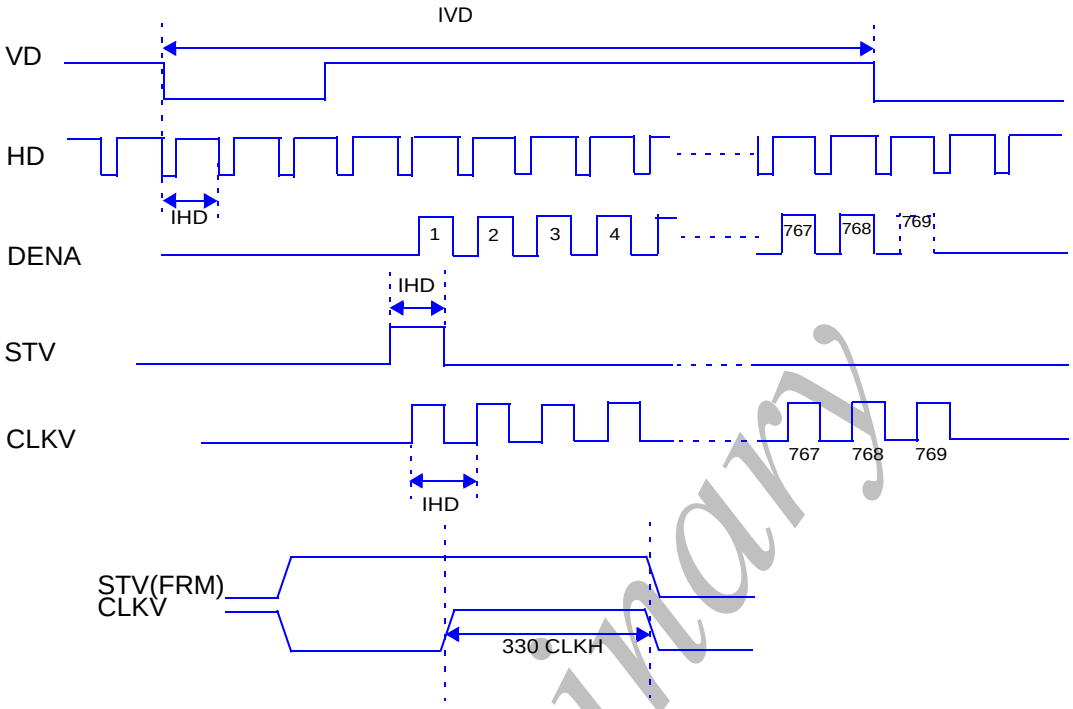


Figure-10

CLKV, STV Timming Specification

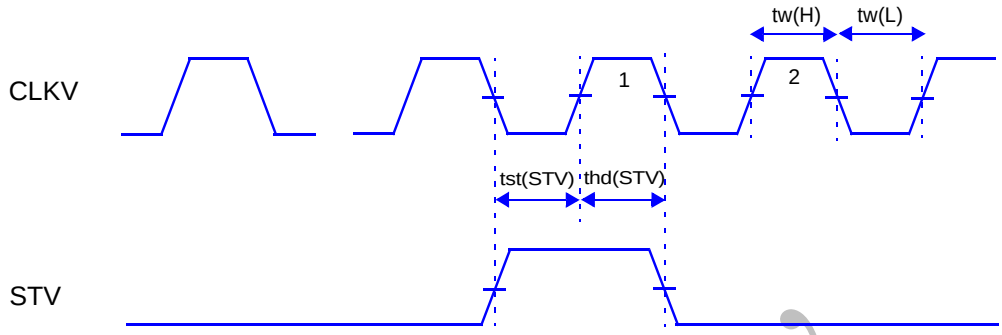


Figure-11

AC timing:

Symbol	Item	Specification			Unit
		Min	Typ	Max	
tst(STV)	STV set-up time	3			µs
thd(STV)	STV hold time	3			µs
tw(H)	CLKV High	10			µs
tw(L)	CLKV Low	5			µs

Data Polarity

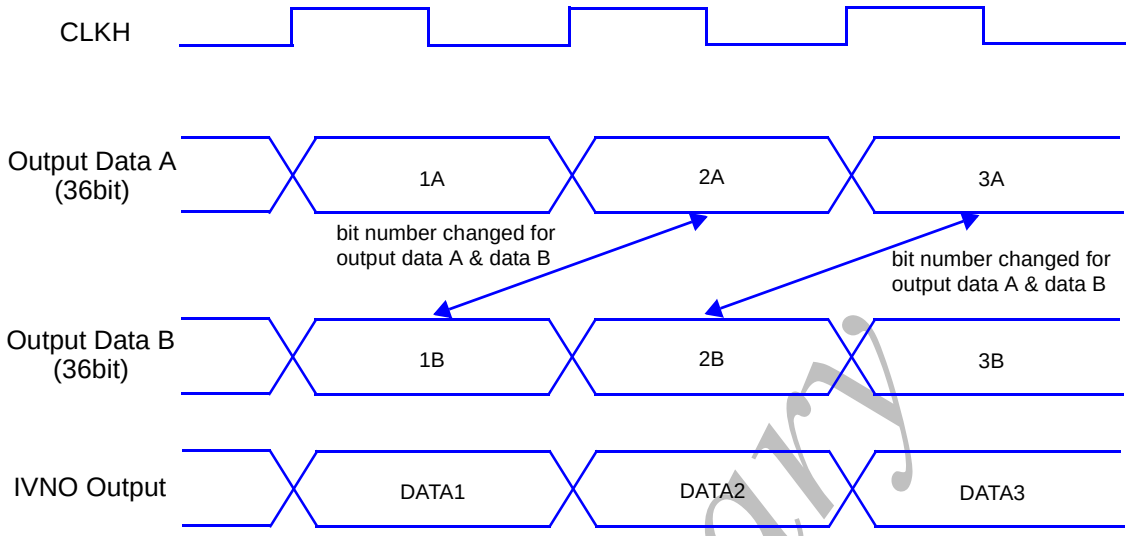


Figure-12

As PHINV presents “H”, Polarity starts to work. ASIC will compare with previous data output before outputting R.G.B data (Even, Odd 36 bit). As the number of bits changed exceeds 18, ASIC will invert R.G.B data, then outputs the inverted data, and ultimately eliminates EMI by reducing the bit numbers changed between two ASIC’s outputs and keeping the bit numbers changed below half of total data output.

Above is the Polarity diagram, Output Data A implies: the original output data has not been calculated by Polarity, including R.G.B. Even & Odd data, each 18 bits. Output Data B implies the actual data has been Polarity calculated. INVO output indicates whether the process (from Data A converted to Data B) has been inverted. Driver IC can convert the received Data B to the original Data A by using INVO signal. Below is the Polarity chart:

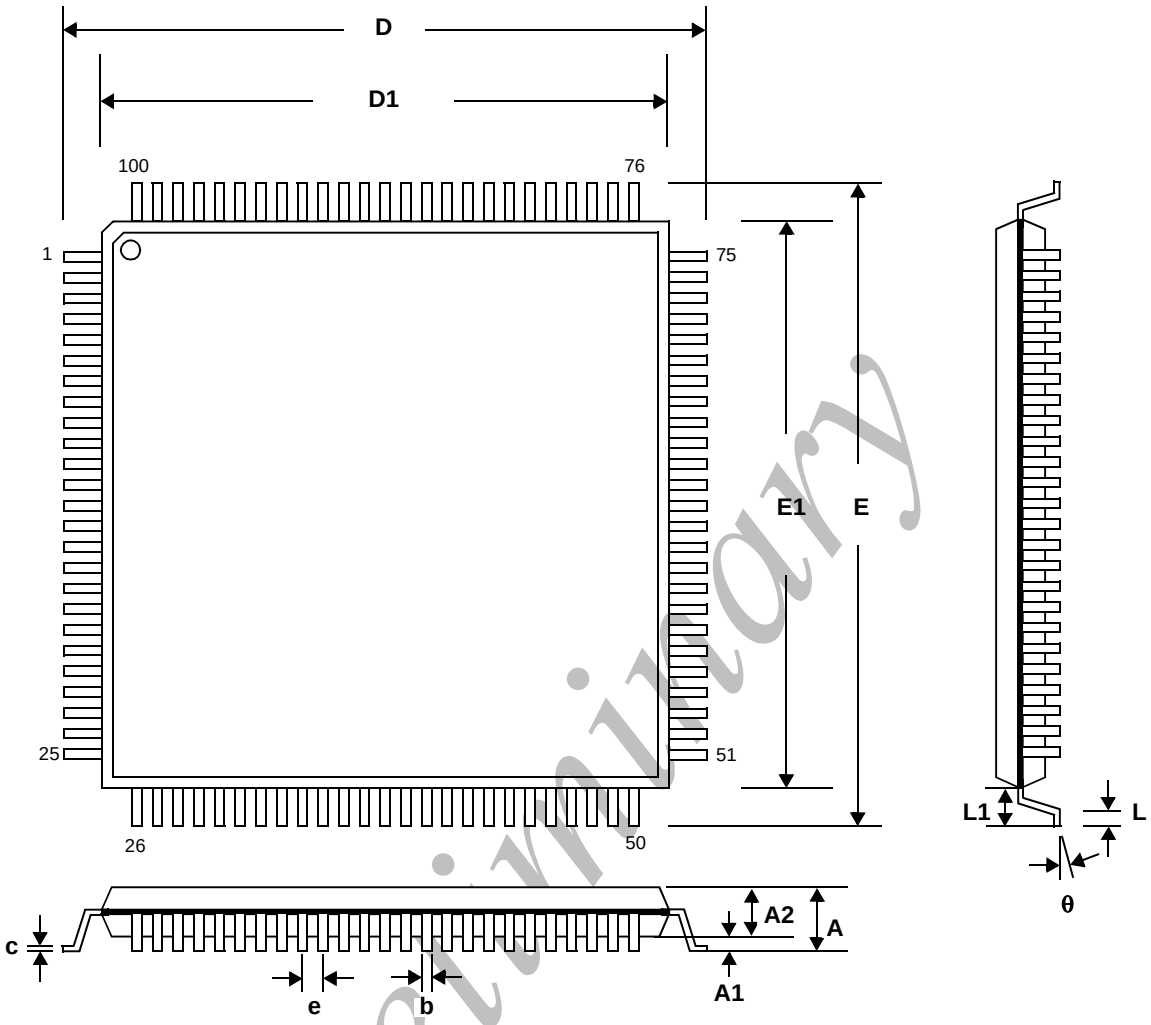
bit numbered changed	INVO Output	Output Data B
19 bit and above	H	Data A inverted
18 bit below	L	Data A non-reverted

Data Output:

1. The Rise Time of Data output from Low (10% VDD) to High (90%VDD): 4ns

2. ODD RO (0~5) and INVO delay 0ns,
EVEN RO (0~5) delay 1ns,
ODD GO (0~5) delay 2ns,
EVEN GO (0~5) delay 3ns,
ODD BO (0~5) delay 4ns,
EVEN BO (0~5) delay 5ns,
R.G.B. data output group has time difference during output.

PACKAGE OUTLINE (100-pin TQFP)



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.2	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1	0.15	0.037	0.039	0.041
b	0.13	0.16	0.23	0.005	0.006	0.009
c	0.09	-	0.2	0.004	-	0.008
D	-	14	-	-	0.551	-
D1	-	12	-	-	0.472	-
E	-	14	-	-	0.551	-
E1	-	12	-	-	0.472	-
e	-	0.40	-	-	0.016	-
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	-	1	-	-	0.039	-
θ	0	3.5°	7°	0	3.5°	7°

APPLICATION CIRCUIT SCHEMATIC

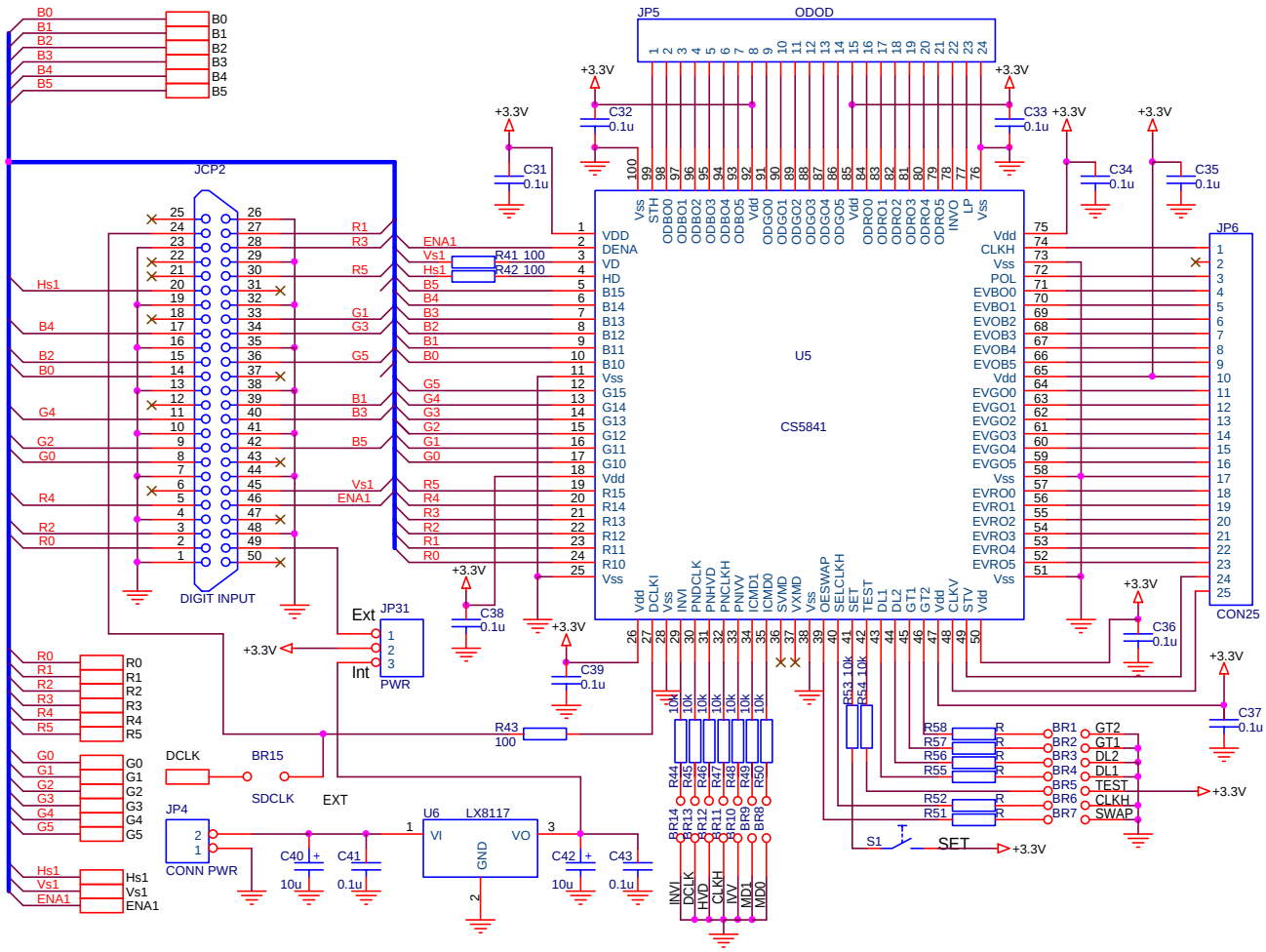


Figure-13 Using 100-pin TQFP package