32-Bit MCU for Motor Control

GENERAL DESCRIPTION

CS6257 is a 32-Bit MCU with embedded Flash designed for motor control applications. The CPU is MIPS-X core with enhanced DSP instructions and accelerator and can run up to 125MHz. There are on-chip 64KB SRAM and embedded 128KB Flash memory. The flash memory is accessed through a cache controller which is shared with external SPI flash memory controller. This external SPI flash memory can be used to further expand the program and data memory space. Combining the CPU and flexible memory structure, CS6257 provide a powerful computing platform and execution unit for various motor control requirements.

The motor controller consists of a 16-bit programmable counter which drives three synchronous 16-bit PWM channels. The counter also includes six pointers to trigger ADC synchronization and software interrupt. Each channel of PWM has two outputs that control upper and lower driver of the motor winding. There are flexible controls of these outputs including polarity, default drive level, as well as dead time control of rising and falling edges individually. The overload detection and protection circuits can accept external inputs or the output of analog comparators for activation of protection. Coupled closely with the motor controller are a fast 12-Bit pipeline ADC. The ADC has a conversion rate of 1Mbps and has 3 channels of Track and Hold as front-end. There are also 3 pairs of analog comparators with programmable threshold that can be used for current and phase detection of the drive currents.

Other on-chip peripherals include another 8-channel 12-Bit SAR ADC, I^2C controller, UART/LIN interface, and SPI controller, and CAN controller. These interfaces share the connection with GPIO ports of the CPU. The GPIO ports also can be used for external interrupt.

CS6257 also includes power-on reset circuits and low-voltage detecting circuit. The embedded flash controller has built-in protection to prevent data and program loss by accidents. It also handles code security to protect unauthorized access of the contents of the embedded flash. An E-JTAG interface is used for debug and ISP purpose. CS6257 requires only single 5Vsupply with a built-in 1.8V regulator for core logic. The regulator requires an external NPN transistor for reducing the power dissipation on chip.

The IDE (Integrated Development Environment) includes Debugger, C-compiler, Assembler and Linker. The library also include real time OS (uC-OS and NNOS) and binary functional calls as well as communication stacks.

FEATURES

CPU

- RISC core with unified DSP instructions 125MIPS
- Clock sources
  - Crystal Oscillator 8MHz – 16MHz
  - Programmable PLL up to 125MHz
- 32-Bit Watch-Dog Timer
- Programmable interrupt controller /w 32 interrupt sources
- E-JTAG debug and ISP interface

Memory

- 24-bit addressing space up to 14MB
- 64KB on-chip SRAM with 4-Way interleave
- Cache controller with 16KB Cache for embedded flash and external memory with Burst Read and Write Through
- 128KB embedded Flash with Flash Controller
  - Write protection and access control
  - 10K Endurance and 10 years Retention
- External SPI Flash memory for expansion

Motor Control

- 16-Bit Programmable Counter Array
  - 6 programmable pointers for ADC triggering and interrupts
- 3 16-Bit complementary PWM channels
  - Polarity and drive control with dead time
  - Overload and protection circuits

PFC Control

- 16-Bit Sub Programmable Counter Array
  - Synchronized with Motor PCA
  - 2 programmable pointers for ADC triggering and interrupts
- 2 channel 16-Bit PWM

High Speed 12-Bit Pipeline ADC

- 5 channel S/H for ADC input sampling
- 5 channel analog window comparators with two sets of compare thresholds
- 3usec conversion time for 5 channels

Other Analog Peripherals

- 8 channel 12-Bit SARADC 10usec conversion time
- On-chip temperature sensor
- Low voltage detect and reset

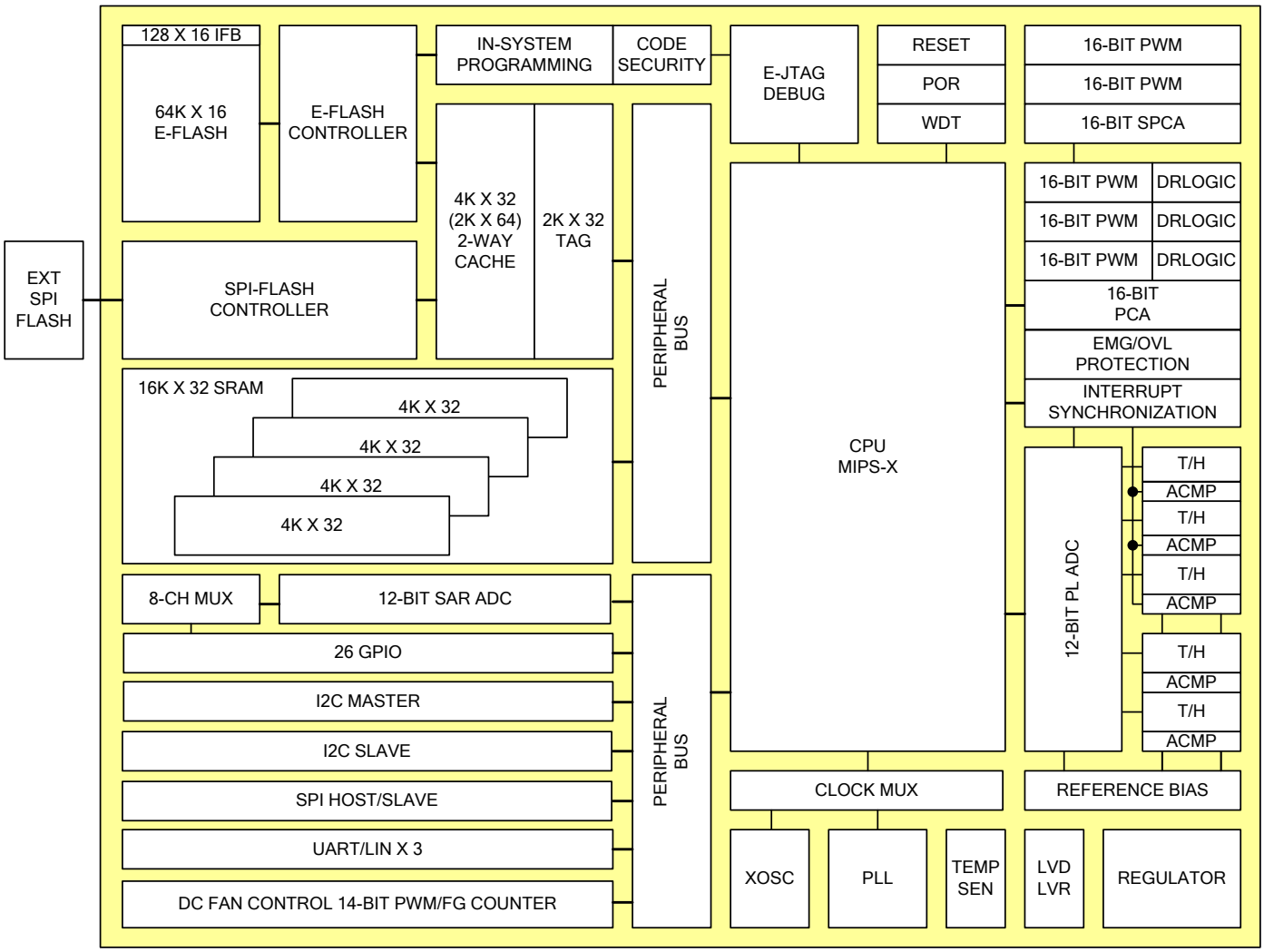
Other Digital Peripherals

- One I^2C Master and One I^2C Slave Controller
- Three UART/LIN Controller
- SPI Host/Slave Controller
- Up to 14 GPIO (48 Pin) and 29 GPIO (64 Pin) with programmable configuration

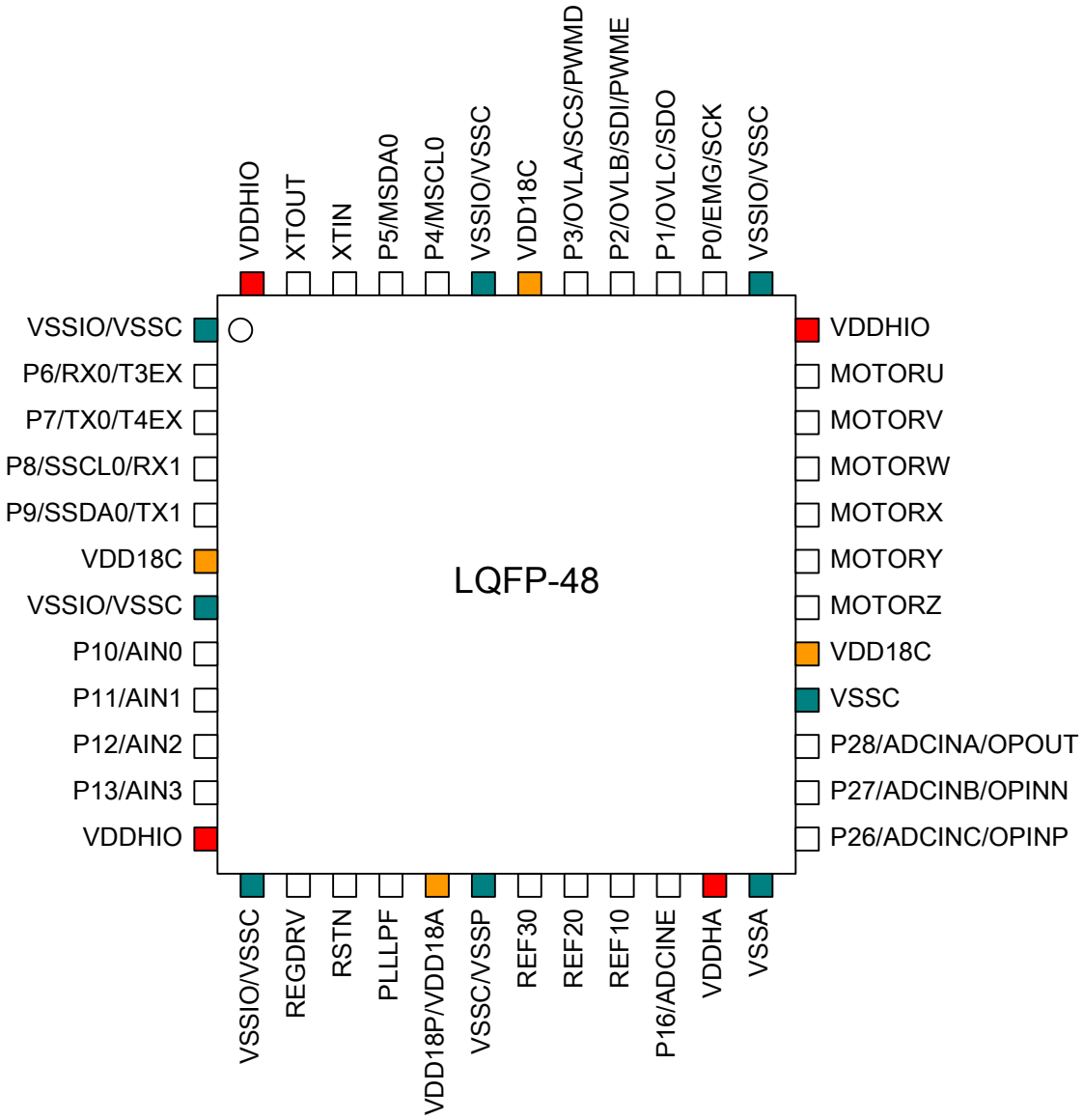
Miscellaneous

- 4.5V to 5.5V single supply
- Operating temperature -40℃ – 85℃
- LQFP-64/LQFP-48 package and RoHS compliant

BLOCK DIAGRAM

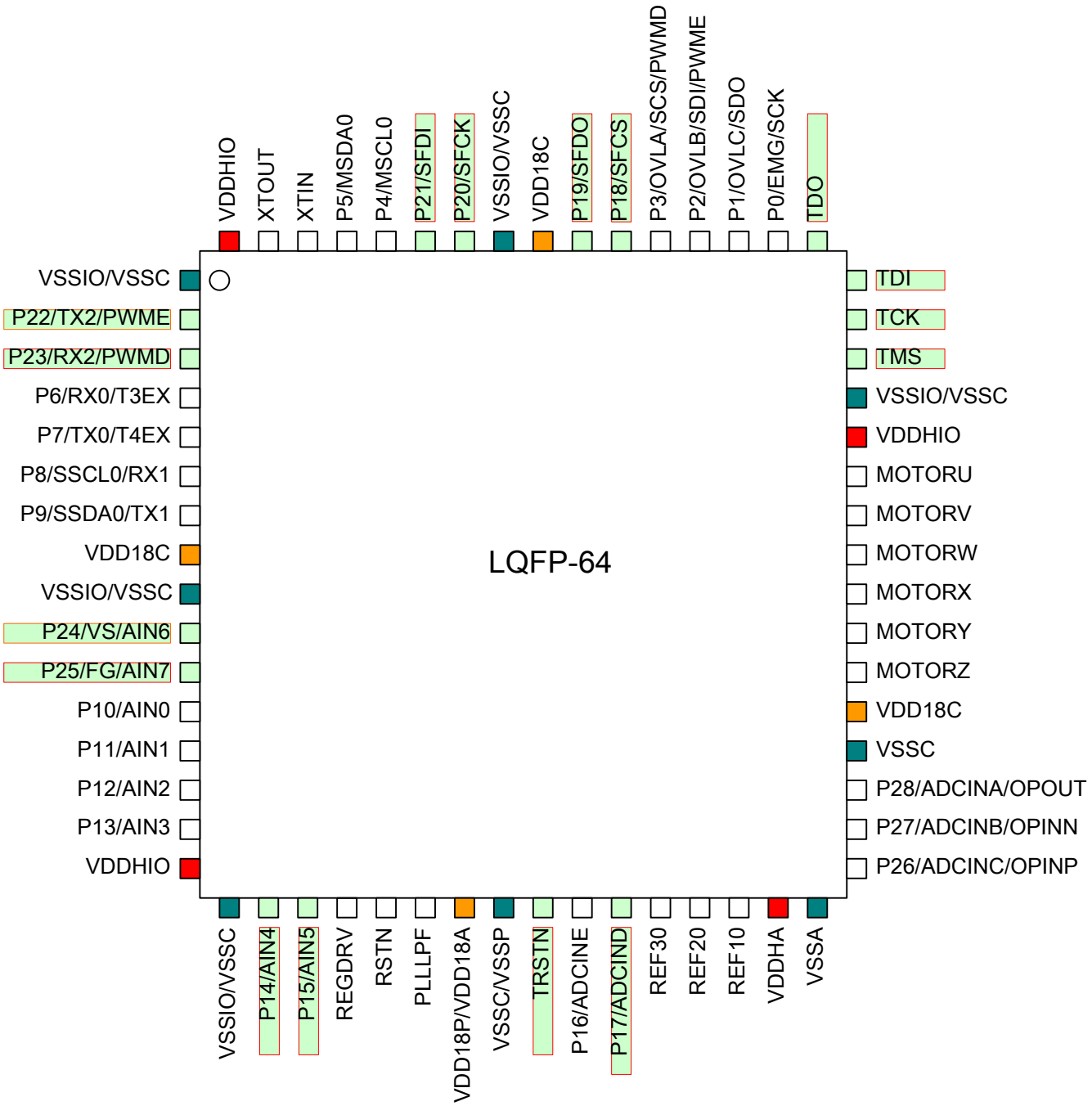


PIN CONNECTION



NOTE:

1. *VDDHIO is 3.0V – 5.5V, and VDDHA are 4.5V – 5.5V. VDD18 are 1.8V and are supplied externally by internal regulator through an external PNP or PMOS transistor.*
2. *Most of VSS pins are double bonded.*
3. *No EJTAG is available. The programming of flash is through WRITER MODE. The device must be programmed using a PROGRAMMER before mounting on the target board.*



NOTE:

1. *Those Pins in text box are not available in LQFP-48.*

PIN DESCRIPTIONS

NAME	TYPE	L64	L48	DESCRIPTION
P0	IO			GPIO P0
				EMG External EMG input for protection logic
				SCK SPI Interface Clock
P1	IO			GPIO P1
				OVLC External Overload Channel C input for protection logic
				SDO SPI Interface Data Out
P2	IO			GPIO P2
				OVLB External Overload Channel B input for protection logic
				SDI SPI Interface Data Out
				PWME PWM Channel E of SPCA Output
P3	IO			GPIO P3
				OVLA External Overload Channel A input for protection logic
				SCS SPI Interface Chip Select
				PWMD PWM Channel D of SPCA Output
P4	IO			GPIO P4
				MSCL0 I^2C Master 0 Clock. It should be configured as open-drain. The voltage on this pin must not be higher than VDDHIO as open-drain to prevent reverse injection.
P5	IO A			GPIO P5
				MSDA0 I^2C Master 0 Data. It should be configured as open-drain. The voltage on this pin must not be higher than VDDHIO as open-drain to prevent reverse injection.
P6	IO			GPIO P6
				RX0 UART 0 Receive Data In.
				T3EX Timer 3 External Input
P7	IO			GPIO P7
				TX0 UART 0 Transmit Data Out.
				T4EX Timer 4 External Input
P8	IO			GPIO P8
				SSCL0 I^2C Slave 0 Clock. It should be configured as open-drain. The voltage on this pin must not be higher than VDDHIO as open-drain to prevent reverse injection.
				RX1

NAME	TYPE	L64	L48	DESCRIPTION
				UART 1 Receive Data In.
P9	IO			GPIO P9
				SSDA0 I²C Slave 0 Data. It should be configured as open-drain. The voltage on this pin must not be higher than VDDHIO as open-drain to prevent reverse injection.
				TX1 UART 1 Transmit Data Out.
P10	IO A			GPIO P10
				AIN0 SAR ADC Input Channel 0. When used as ADC input, the corresponding GPIO function must be off with not driving, and its ANEN must be on.
P11	IO A			GPIO P11
				AIN1 SAR ADC Input Channel 1. When used as ADC input, the corresponding GPIO function must be off with not driving, and its ANEN must be on.
P12	IO A			GPIO P12
				AIN2 SAR ADC Input Channel 2. When used as ADC input, the corresponding GPIO function must be off with not driving, and its ANEN must be on.
P13	IO A			GPIO P13
				AIN3 SAR ADC Input Channel 3. When used as ADC input, the corresponding GPIO function must be off with not driving, and its ANEN must be on.
REGDRV	A			REGDRV This is the pre-driving output of the 1.8V regulator. It should be connect to the base of an external NPN transistor to provide overall 1.8V supply to all VDDC pins.
RSTN	I/OD			RESETN This pin serves as external reset input. It is low assertion. Typically, it needs to be connected to VDDH through a resistor and with a capacitor connected to ground. This RC time constant will determine the reset period. When other reset condition occurs, such as WDT, LVR, this pin will also be forced low by internal driver. This ensures all reset conditions go through same process and duration.
PLLLPF	A			PLL Loop Filter This pin should be connected to VSSP through a capacitor to provide loop time constant of the phase lock loop. The ESD diodes are connected to VDDHR and VSSP.
				TESTHH When this pin is forced to be higher than 3.5V, it enters the factory test mode. It is prohibited to allow this pin to exceed more than 2.0V for normal mode.
REF10	A			PL ADC Low Reference This is for low reference of PL ADC. It should be decoupled soundly with VSSA. Typical level is 1.0V.
REF20	A			PL ADC Mid Reference This is for middle reference of PL ADC. It should be decoupled soundly with VSSA. Typical level is 2.0V.
REF30	A			PL ADC High Reference This is for high reference of PL ADC. It should be decoupled soundly with VSSA. Typical level is 3.0V.
ADCINC	A			PL ADC Channel C Input This connects to ADC channel C input T/H. It also connects to the channel C

NAME	TYPE	L64	L48	DESCRIPTION
				window comparators.
ADCINB	A			PL ADC Channel B Input This connects to ADC channel C input T/H. It also connects to the channel C window comparators.
ADCINA	A			PL ADC Channel A Input This connects to ADC channel C input T/H. It also connects to the channel C window comparators.
MOTORZ	O			Motor Driver Z Output Motor Controller Channel C lower arm driver output.
MOTORY	O			Motor Driver Y Output Motor Controller Channel B lower arm driver output.
MOTORX	O			Motor Driver X Output Motor Controller Channel A lower arm driver output.
MOTORW	O			Motor Driver W Output Motor Controller Channel C upper arm driver output.
MOTORV	O			Motor Driver V Output Motor Controller Channel B upper arm driver output.
MOTORU	O			Motor Driver U Output Motor Controller Channel A upper arm driver output.
P14	IO A			GPIO P14 AIN4 SAR ADC Input Channel 4. When used as ADC input, the corresponding GPIO function must be off with not driving, and its ANEN must be on.
P15	IO A			GPIO P15 AIN5 SAR ADC Input Channel 5. When used as ADC input, the corresponding GPIO function must be off with not driving, and its ANEN must be on.
P16	IO A			GPIO P16 This pin use VDDHA as IO supply. It is recommended used as input only. ADCINE Pipeline ADC channel E input. When used as ADC input, the corresponding GPIO function must be off with no driving, and its ANEN must be on.
P17	IO A			GPIO P17 This pin use VDDHA as IO supply. It is recommended used as input only. ADCIND Pipeline ADC channel D input. When used as ADC input, the corresponding GPIO function must be off with no driving, and its ANEN must be on.
P18	IO			GPIO P18 SFCS SPI Flash Interface CS output.
P19	IO			GPIO P19 SFDO SPI Flash Interface DO output
P20	IO			GPIO P20 SFCK SPI Flash Interface CK output.
P21	IO			GPIO P21 SFDI SPI Flash Interface DI input

NAME	TYPE	L64	L48	DESCRIPTION
P22	IO			GPIO P18 TX2 EUART 2 Transmit Data Out. PWMD Output of PWM channel D.
P23	IO			GPIO P21 TX2 EUART 2 Receive Data In. PWME Output of PWM channel E.
P24	IO A			GPIO P24 AIN6 SAR ADC Input Channel 6. When used as ADC input, the corresponding GPIO function must be off with not driving, and its ANEN must be on.
P25	IO A			GPIO P25 AIN7 SAR ADC Input Channel 7. When used as ADC input, the corresponding GPIO function must be off with not driving, and its ANEN must be on.
VDD18C	P			Power Supply for Core This is 1.8V supply for core logic. It should be connected to the external regulator transistor output. It should be decoupled to VSSC. All VDD18C are shorted internally.
VDD18P	P			Power Supply for PLL This is 1.8V supply for core logic. It should be connected to the external regulator transistor output. It should be decoupled to VSSP. VDD18P isolated from VDD18C and is shorted to VCC18C through bonding.
VSSC	G			Ground Supply for Core Should be decoupled to VDD18C.
VSSP	G			Ground Supply for PLL Circuits Should be decoupled to VDD18P.
VSSA	G			Ground Supply for Analog Circuits Should be decoupled to VDDHA.
VSSIO	G			Ground Supply for I/O Should be decoupled to VDDHIO.
VDDHA	P			Power Supply for Analog Circuit This is positive supply for analog circuit. It should be connected to 4.5V – 5.0V external supply through good L-C decoupling. It should be decoupled to VSSA. VDDHA is isolated from other VDDH on chip.
VDDHR	P			Power Supply for Regulator and SAR ADC This is positive supply for internal regulator and SAR ADC. It should be connected to 4.5V – 5.0V external supply. It should be decoupled to VSSC. VDDHR is isolated from other VDDH and is shorted to VDDHIO through bonding.
VDDHIO	P			Power Supply for I/O This is positive supply for I/O cell. It should be connected to 4.5V – 5.0V external supply. It should be decoupled to VSSIO. All VDDHIO are shorted internally.
TRSTN	TI PD			EJTAG Test Port Reset This is low assertive. It has internal pull-down resistor, and should be tied to low if the EJTAG is not used.
TMS	TI PU			EJTAG Test Mode Select It has internal pull-up resistor and should be tied to high if the EJTAG is not used.

NAME	TYPE	L64	L48	DESCRIPTION
TCK	TI PD			EJTAG Test Clock It has internal pull-down resistor and should be tied to low if the EJTAG is not used.
TDI	TI PD			EJTAG Test Data In It has internal pull-down resistor and should be tied to low if the EJTAG is not used.
TDO	TO			EJTAG Test Data Out It is a output pin. If EJTAG is not used, it should be left floating.

Note: "P" denotes power supply pins
"G" denotes ground pins
"O", "IO", "A" denotes output only, input/output, and analog types.
"PU" and "PD" denotes pins with internal pull-up or pull-down.
"TI" and "TO" denotes testing only input or output pins..

1. Introduction

CS6257 is a highly integrated 32-Bit MCU for motor control applications. It includes a high performance RISC CPU with five stages of pipelines and running up to 125MIPS. There are flexible clocking schemes with on-chip crystal oscillator, and an on-chip phase-locked loop to generate system clock.

The CPU has 24-bit addressing and implements a unique memory structure that allows high performance operations. The total 64KB SRAM is partitioned into four 4KBx32 slices and arranged in interleaved fashion. This avoids any memory bandwidth bottleneck and allows simultaneous completion of instruction and data fetches in one cycle. CS6257 also includes an on-Chip 128KB embedded Flash memory (E-Flash) organized as 64K X 16 and an on-chip SPI-Flash Controller. The CPU accesses E-FLASH and SPI-Flash through a common 2-Way Set-Associative Cache. Cache size is 2K X 64 (16KB) Cache RAM with Tag RAM of 2K X 32 (8KB). The existence of the cache significantly reduces the impact of slow Flash access time when program must be run from Flash while maintaining the CPU running at its maximum clock rate.

The motor controller is a 16-bit Programmable Counter Array (PCA) driving 3 channels of 16-bit PWM with complementary outputs. The PCA can operate under either symmetrical or asymmetrical modes and has flexible interrupt and ADC triggering setting to synchronize with CPU and ADC. Each PWM channel provides complementary drive to the external motor winding driver and the setting of the PWM channels include edge dead times, driving polarity. A protection logic tightly coupled with the PWM channels is used to handle emergency condition. The overload signaling can either come from external pin input or from on-chip analog window comparators for sensing of winding current. An additional 16-bit Sub Programmable Counter Array (SPCA) is used for power factor control (PFC). SPCA is synchronized with main motor PCA and has separate interrupt and ADC triggering settings. This synchronization can maintain coherent software processing of motor control and PFC control. SPCA drives two 16-bit PWM channels. And each PWM is also coupled with overload detection of on-chip analog window comparators for protection purpose.

CS6257 implements a high-speed 12-bit pipeline ADC running at 2MBPS. The ADC has 5 channels of inputs each with individual track and hold (T/H) circuit. The T/H circuit ensures simultaneous signal sampling avoiding any cascading sampling time delay among channels. Three of the ADC channels (Channel A, B and C) can be used for motor phase current sensing and two of the channels (Channel D and E) can be used for PFC line current/voltage sensing. The total elapse time of conversions is less than 4 usec for five channels. Each ADC input is also connected to a window comparator. The window comparator detects out of range condition of the input level and triggers overload protections. Channel A, B, and C share a set of on-chip threshold for minimum and maximum voltage level while Channel D and E share a set of threshold setting.

A separate 12-bit Successive Approximation ADC is also present in CS6257. The SAR ADC has 8 input channels which are shared with GPIO port pins. The SAR ADC can be used for measurement of temperature of motor and environment, or other external analog levels. This decouples the tasks PLADC of motor and PFC control. There is also on-chip temperature sensor and can be read from SAR ADC providing protection against thermal breakdown of CS6257.

Up 26 GPIO ports are available for CS6257 each with programmable drive and input configurations. These GPIO pins have multifunction and share with other peripherals. CS6257 include three Enhanced UART (EUART) controllers with LIN bus capability, and one I^2C master controller, one I^2C Slave controller, and a SPI host/slave controller. All these peripherals have built-in FIFO thus substantially reduce the software load in handling the interface functions.

The internal core logic and memory is supplied with on-chip regulator with accurate power-on reset circuit. And on-chip Low-Voltage-Detection (LVD) circuit can be used to detect fault in supply voltage. Watch Dog Timer (WDT) and register access protection prevent run-away program executions. The E-Flash controller also includes write-protect zones which can be enabled to maximize the protection of the on-chip program integrity. All these measures ensure CS6257 can operate reliably at harsh environment.

In summary, CS6257 provides an ideal single-chip solution for implementations of enhanced motor control applications. CS6257 is also low cost and is available in small footprint LQFP-48 and LQFP-64 packages.

2. CPU Architecture

The heart of CS6257 is a MIPS-X5 CPU core with enhanced DSP instruction sets. The MIPS-X5 instruction set is a 32-bit DSP-enhanced RISC instruction set. New instructions include 16-bit and 32-bit multiply, multiply-accumulate, sign-extension, low overhead looping, and byte or word load and store. Additional enhancements include simplified exception and break points handling, and CPU address and instruction profiling to help software optimizations. The CPU is fully supported with GNU development environment (C compiler, assembler, linker, GDB source level debugger). There is also available for general C library supports that include optimized DSP function calls. The software library also contains a real-time OS which is uC-OS compatible with enhanced task scheduling and management. A GUI/IDE based environment is provided under Red Hat/Cygnus platform where cycle- and result-accurate simulation tools can be used for software development. The MIPS-X5 is Harvard-architecture RISC microprocessor core. This means that CPU itself has separate instruction and data paths. These buses are fed into memory controller and mapped to a single memory space. The hardware block diagram is shown in the following. The address is 24-bit wide and allows up to 16MB of addressing space.

2.1 CPU

The CPU is a RISC CPU with 5 stage pipeline. This is a common architecture shared among many MIPS based system as shown in the next figure. Each instruction is partitioned into five stages of operations – IF: Instruction Fetch, RF/ID: Register Fetch and Instruction Decode, EXE: ALU or MAC execution, MEM: Memory Operation for read and write, WB: Write Back to register file.

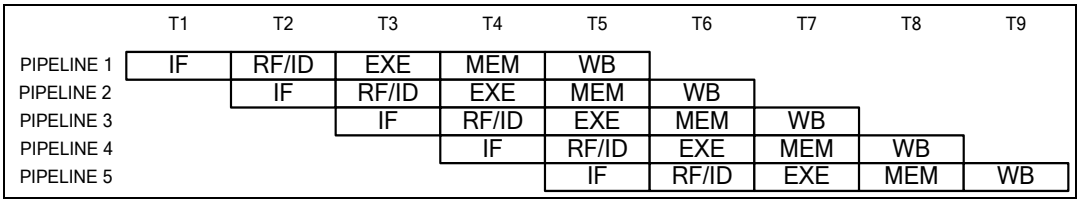
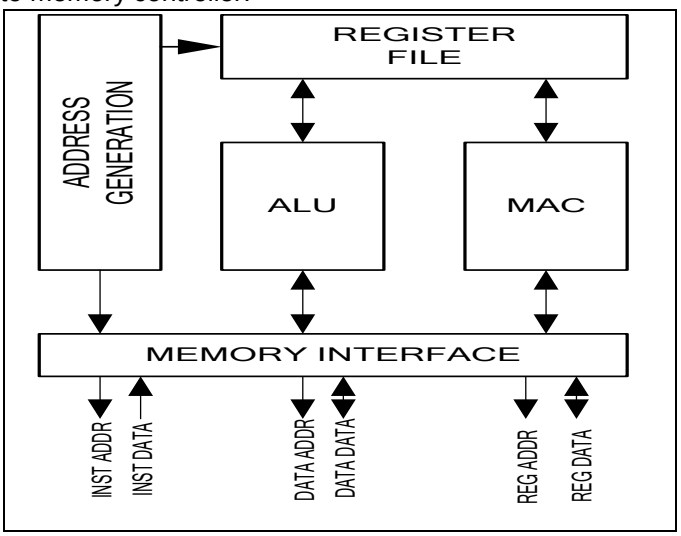


Figure 1 Pipeline Stage

Because of the pipeline stages, there is a need to describe the difference between a blocking and a non-blocking exception. When an exception of blocking type occurs, if there is a branch instruction present in the MEM or WB stage, then the exception will be suppressed until the branch instruction finishes. This greatly simplifies the handling of exception processing and its related restart implementations. On the other hand, a non-blocking type of exception will be processed immediately when it occurs. As a result, if there is branch instructions present in the MEM or WB stages, and a non-blocking exception occurs, it is usually not restart-able. Therefore, non-blocking exception usually are assigned for those requiring immediate attentions, such as Memory Misalignment, WDT, LVR. The architecture of CPU is shown in the following diagram. It contains the two execution units – ALU and MAC, as well as AGU (Address Generation Unit) that generates register and memory address, the memory interface unit passes the address and data bus to memory controller.



The ALU is the base execution unit for the CPU and contains an arithmetic unit, a logical unit, a saturation unit and a shifter. The MAC handles multiplication and division operations and contains a 32-bit by 32-bit multiplication unit, two 40-bit accumulators, a shifter and a saturation unit. The AGU handles instructions with concurrent address pointer operation and performs computation of address for data movement between memory and the register file. Combining AGU with ALU and MAC, allows extensive usage of the multi-ports register file. The AGU provides sustained address pointer calculation every cycle with no latency yet allows easy restart-ability after exception. The MAC unit incorporates a single pipeline register in the calculation of multiplication product and the accumulation loop is contained within a single pipeline stage. However, there is a result latency hazard associated with a multiplication operation that writes back to the register file directly. There is no hardware interlock to prevent the use of the intended destination register for the multiplication product as a source operand for an immediately subsequent instruction. The compiler is aware of this hazard and thus will schedule legal instructions in this result delay slot. If manual assembly code violates this rule, then IRQs must be disabled for safety; otherwise, a taken IRQ could separate these two instructions in the pipeline resulting unexpected behavior.

2.2 CPU Registers

The CPU has 32 general purpose registers in REGISTER FILE. The following table describes the general usage off these registers by software. When creating hand-coded assembly subroutines uses of R1 to R7 is preferred to minimize tool issues.

Register	Description
R0	Hardcode 0
R1	Reserved for assembler use
R2	Function return value
R3	Function return value
R4	1st 32-bit argument for function call
R5	2nd 32-bit argument for function call
R6	3rd 32-bit argument for function call
R7	4th 32-bit argument for function call
R8 - R23	Reserved for compiler use
R24	Read only data segment offset
R25	Data segment offset
R26	ROM text segment offset
R27	Internal programming register base address
R28	Uncommitted
R29	Stack pointer
R30	Uncommitted
R31	Return address

The physical register file is triple port so that two read and one write can occur every cycle concurrently. These general registers are referenced in the instruction as source operand and result operand.

The CPU also defines a number of special registers that gave specific dedicated functions. These registers are used by CPU in certain instructions such as Multiply, Divide, indirect load and store, and can only be accessed through special instructions such as MOVFRS (Move From Special Register), MOVTOS (Move To Special Register). The following table lists the description of these special registers.

SPEC	Register	Description
0x00	-	Reserved
0x01	PSW	Processor Status Word
0x02	DIV	Divide Register. Used in multi-step divide algorithm
0x03	-	Reserved
0x04	PCRS	Program Counter Save/Restore. Used to save and restore the Program Counter for exception
0x05	DEBUG	Debug Register (for compatibility with other product)
0x06	DEPC	Debug Exception Program Counter (for compatibility with other product)
0x07	DESAVE	Debug Scratch Pad Register (for compatibility with other product)
0x08	AD0	Address Register 0. Address Pointer in AGU used in indirect addressing instructions.
0x09	AD1	Address Register 1. Address Pointer in AGU used in indirect addressing instructions.
0x0A	AD2	Address Register 2. Address Pointer in AGU used in indirect addressing instructions.
0x0B	AD3	Address Register 3. Address Pointer in AGU used in indirect addressing instructions.
0x0C	ADINC	Address Increment Register. Address Pointer increment in AGU.
0x0D	AC0	Accumulator 0. Bit 31-0 of 40-bit Accumulator 0 in MAC
0x0E	AC1	Accumulator 1. Bit 31-0 of 40-bit Accumulator 1 in MAC
0x0F	AC0H	Accumulator 0. Bit 39-32 of 40-bit Accumulator 0 in MAC
0x10	AC1H	Accumulator 1. Bit 39-32 of 40-bit Accumulator 0 in MAC
0x11	PC	Program Counter. Address of current CPU instruction being fetched
0x12	PCM1	Program Counter Minus 1. Value of previous PC.
0x13	PCM2	Program Counter Minus 2. Value of previous PCM1.
0x14	PCM3	Program Counter Minus 3. Value of previous PCM2.
0x15	PCM4	Program Counter Minus 4. Value of previous PCM3.
0x16	PCM5	Program Counter Minus 5. Value of previous PCM4.
0x17	PCM6	Program Counter Minus 6. Value of previous PCM5.
0x18	PCM7	Program Counter Minus 7. Value of previous PCM6.

2.2.1 PSW – Processor Status Word

PSW contains machine status information. There are actually two registers contained in PSW: PSW-current and PSW-other. PSW-current contains the current machine status. When an exception (Debug Exception or IRQ or TRAP) occurs, PSW-current is copied to PSW-other so it can be used to save and restore context. Occurrence of a blocking IRQ or TRAP sets the “m” bit (blocking interrupt mask) and clears the “s” bit (PCRS enable). Occurrence of a non-blocking interrupt has the same effect with the addition that the “d” bit (debug PC chain shifting enable) is also set. The JPCRS instruction transfer all PSW-other bits to PSW-current as it completes and forces the “n” bit to 0. Any type of exception takes precedence over a DIRQ, EIRQ, JPCRS, or MOVTOS that writes the PSW. Because the “m” bit does not mask non-blocking IRQ, implementation-defined breakpoint logic can still operate in ISR and OS code where IRQ normally are disabled. The default value of PSW is 0x3A.

Name	Bit	Description
n	6	Non-Blocking Interrupt Status. Read-Only. 1= non-blocking interrupt active.
m	5	Blocking Interrupt Mask in PSW-current.
M	4	Blocking Interrupt Mask in PSW-other.
d	3	Enable shifting of debug PC Chain (PCM3 -> PCM7)
D	2	Enable shifting of debug PC Chain (PCM3 -> PCM7). Saved version in PSW-other.
s	1	Enable saving restart PC into PCRS register. PSW-current is copied to PCRS.
S	0	Enable saving restart PC into PCRS register. Saved version in PSW-other

2.2.2 PCRS – Program Counter Restart/Save

PCRS register samples the PC chain when enabled by the PSW ("s" bit set to 1). It can be used to restart the CPU after servicing the exception. At entry of exception, PCRS register contains the address of the abandoned instruction in the EXE stage of the pipeline. The instruction JPCRS is used to restart the abandoned state, in effect, it causes a jump to PCRS, taking effect in the EXE pipeline state at the same time restore the PSW-other into PSW-current. A TRAP instruction results in the saving of the instruction abandoned in the RF/ID stage into PCRS. Therefore TRAP instruction is not restarted upon return.

2.2.3 PC Chain (PCM1 – PCM7)

The PC chain saves the seven previous PC values In a shift register to track the thread of CPU execution. The development tools use the PC chain to support the hardware breakpoint facilities. Because of the latencies involved in triggering a breakpoint, PCs beyond the end of the pipeline are saved so that triggering instructions can be precisely identified. Because breakpoints use the non-blocking IRQ mechanism, a control flow change can be in pipeline. Software interpretation using the PC chain might be necessary for a clean restart. In addition, alignment exceptions can be tracked to the exact instruction using the PC chain.

2.2.4 Exceptions Handling

It is necessary to discuss the exception handling of CPU because of the pipeline stages. The MIPS-X5 adopts an exception handling mechanism that simplifies and reducing latencies and overhand and removing special processing from ISR. Central to this mechanism is the automatic suppression of most exception processing whenever an instruction identified as a flow control instructions is present in the MEM or WB stages of the pipeline. Exception types subject to suppression are so-called blocking IRQ and TRAP instruction. Suppression eliminates the need to restart multiple instructions explicitly because it guarantees that there is no discontinuity of PC value between the instructions in EXE, RF/ID and IF stages. Thus the instructions in MEM and WB complete if an exception should occurs; after exception processing, the machine can be restarted simply using the instruction that was in EXE at the time exception occurred. JPCRS instruction is used to restart the machine at this address that enables interrupts and returning to user state in the EXE stage. A subsequent immediate exception still allows the last restart instruction to complete because JPCRS masks exception for two further cycles as it is classified as a flow control instruction.

TRAP instruction causes a software interrupt in the EXE stage, the PC of the instruction in RF/ID is saved in PCRS register, this makes the instruction following the TRAP is restart-able. Although no hardware interlock exists, a TRAP in the first delay slot of a taken flow-control instruction is not easily restart-able and must be avoided in normal user code. When a TRAP is in EXE stage, and no flow-control instruction is in MEM or WB stage, and IRQ occurs, the IRQ will have higher priority than TRAP, and after IRQ service the TRP is restarted.

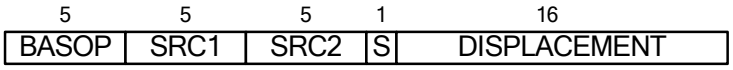
2.3 Instruction Set Summary

Mnemonic	Description	Mnemonic	Description
ABS	Absolute Value	MSUDLA	Multiply-Subtract DSP, Low 16 bits
ADD	Add	MULDD	Multiply DSP, 32 bits
ADDHI	Add High Immediate	MULDEH	Multiply DSP, 32 bits * High 16 bits
ADDI	Add Immediate	MULDEL	Multiply DSP, 32 bits * Low 16 bits
ADDS	Add With Saturation	MULDH	Multiply DSP, High 16 bits
AND	Bitwise AND	MULDL	Multiply DSP, Low 16 bits
ANDI	Bitwise AND Immediate	MULDM	Multiply DSP, High 16 bits * Low 16 bits
ASR	Arithmetic Shift Right By Immediate Value	MULDDA	Multiply DSP, 32 bits to Accumulator
ASRV	Arithmetic Shift Right	MULDEHA	Multiply DSP, 32 bits * Upper 16 bits to Accumulator
BIC	Bitwise Bit Clear	MULDELA	Multiply DSP, 32 bits * Low 16 bits to Accumulator
BEQ	Branch If Equal	MULDHA	Multiply DSP, High 16 bits to Accumulator
BGE	Branch If Greater Or Equal (Signed)	MULDLA	Multiply DSP, Low 16 bits to Accumulator
BHS	Branch If Higher Or Same (Unsigned)	MULDMA	Multiply DSP, High 16 bits * Low 16 bits to Accumulator
BLO	Branch If Less Than (Unsigned)	MULS	32-bit Multiply
BLT	Branch If Less Than (Signed)	NOT	Bitwise Negation
BNE	Branch If Not Equal	OR	Bitwise OR
DIRQ	Disable Interrupts	ORI	Bitwise OR Immediate
DSTEP	Multi-Step Divide Instruction	SATS	Saturate Short
EIRQ	Enable Interrupts	SB	Store Byte
JMPI	Jump Indexed	SHL	Shift Left By Immediate Value
JPCRS	Jump PC And Restore State	SHLV	Shift Left Variable
JSPCI	Jump Indexed And Store PC	SHR	Shift Right By Immediate Value
LB	Load Signed Byte	SHRV	Shift Right Variable
LBU	Load Unsigned Byte	SS	Store Single Word
LD	Load Doubleword	SSH	Store Single Word High
LDA	Load Using Address Registers	ST	Store Doubleword
LOOP	Low Overhead Loop	STA	Store Using Address Registers
LS	Load Signed Single Word	STPA	Store Packed Using Address Registers
LSH	Load Single Word High	SUB	Subtract
LSU	Load Unsigned Single Word	SUBNC	Subtract With No Carry In
MACDDA	Multiply-Accumulate DSP, 32 bits	SUBS	Subtract With Saturation
MACDEHA	Multiply-Accumulate DSP, 32 bits * High 16 bits	SXB	Sign Extend Byte
MACDELA	Multiply-Accumulate DSP, 32 bits * Low 16 bits	SXS	Sign Extend Short
MACDHA	Multiply-Accumulate DSP, High 16 bits	TRAP	Trap Unconditionally
MACDLA	Multiply-Accumulate DSP, Low 16 bits	XOR	Bitwise XOR
MACDMA	Multiply-Accumulate DSP, High and Low 16 bits	XORI	Bitwise XOR Immediate
MOVFRS	Move From Special Register	ZFB	Zero Fill Byte

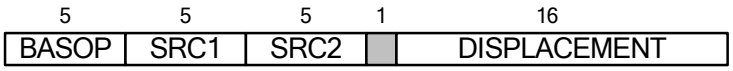
Mnemonic	Description	Mnemonic	Description
MOVTOS	Move To Special Register	ZFS	Zero Fill Short
MSUDHA	Multiply-Subtract DSP, High 16 bits		

Each instruction is in 32-bit length and instructions follow various basic formats. The OPCODE is always 5-bit.
**** Two instructions are added to the above table for the debugging purpose.
**** SDBBP – software debug break exception.
**** DERET – software debug exception return.

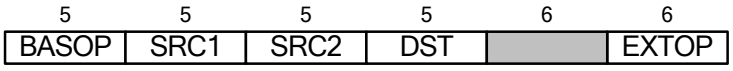
BEW, BGE, BHS, BLO, BLT, BNE:



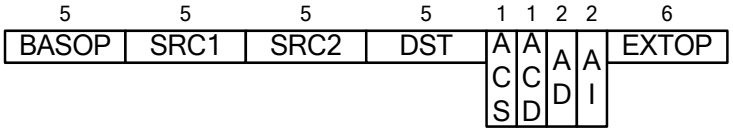
LOOP, ADDHI



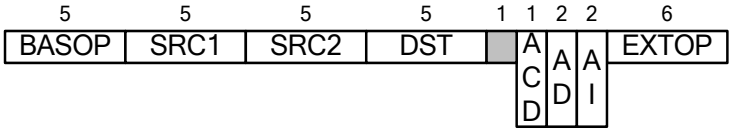
ADD, ADDDS, AND, ASRV, BIC, DSTEP, MULDD, MULDEH, MULDEL, MULDH, MULDL, MULDM, MULS, OR, SHRV, SUB, SUBNC, SUBS, XOR



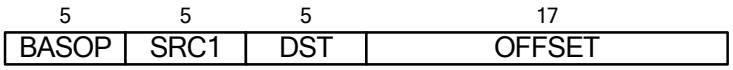
MACxx, MSUDxx



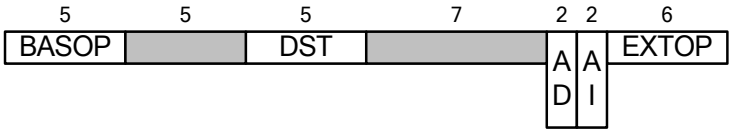
MULxxA



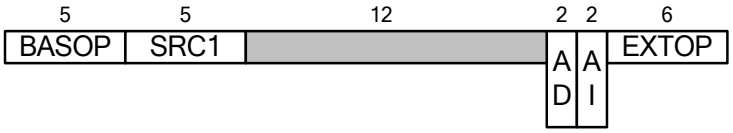
LD, LB, LS, LBU, LSU, LSH, ST, SS, SB, SSH



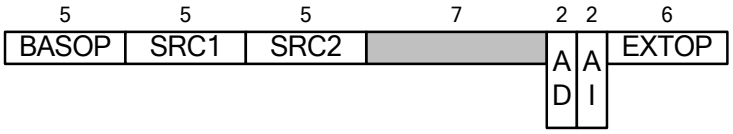
LDA



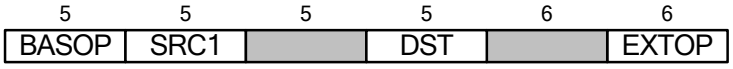
STA



STPA



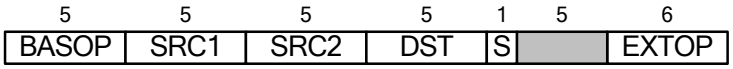
ABS, NOT, SATS, SXB, SXS, ZFS, ZFB



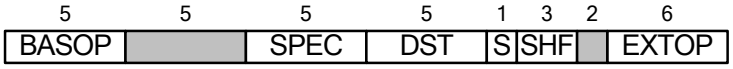
ASR, SHR

SHL

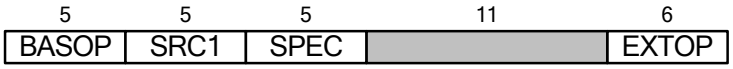
SHLV



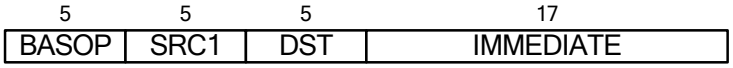
MOVFRS



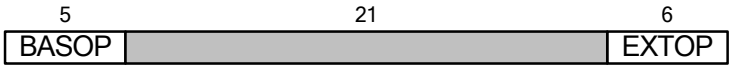
MOVTOS



ADDI, ANDI, ORI, XORI



SDBBP(BASOP=5h1F, EXTOP=6'h36), DBGRET(BASOP=5'h1F, EXTOP=6'h35)



2.4 Register Map Summary

ADDRESS	NAME	RW	P	DESCRIPTION
Register Access Protection				
1F0000	TA	WO	-	Protection Control Register A
1F0004	TB	WO	-	Protection Control Register B
1F0008	TC	WO	-	Protection Control Register C
1F000C	TD	WO	-	Protection Control Register D
Interrupt Controller				
1F0010	IRQBASE	RW	TA	Global IRQ starting address
1F0014	IRQMASK	RW	TA	IRQ mask
1F0018	IRQVECT	RO	-	IRQ encoded priority index vector
1F001C	IRQSTAT	RW	-	IRQ status
Break Point and Debug Control				
1F0020	BRKINST1	RW	-	Instruction Fetch Break Point 1 - Address Value
1F0024	MSKINST1	RW	-	Instruction Fetch Break Point 1 - Address Mask
1F0028	BRKINST2	RW	-	Instruction Fetch Break Point 2 - Address Value
1F002C	MSKINST2	RW	-	Instruction Fetch Break Point 2 - Address Mask
1F0030	DEBUGCTL	RW	TA	Debug Control Register (DCR)
1F0034	DEBUG	RW	TA	Debug Register
1F0038	BPCONTROL	RW	TA	Break Point Control
1F003C	BPSTATUS	RW	TA	Break Point Status
1F0040	BRKDSTA1	RW	-	Data Fetch Break Point 1 - Starting Address Value
1F0044	MSKDSTA1	RW	-	Data Fetch Break Point 1 - Starting Address Mask
1F0048	BRKDEND1	RW	-	Data Fetch Break Point 1 - Ending Address Value
1F004C	MSKDEND1	RW	-	Data Fetch Break Point 1 - Ending Address Mask
1F0050	BRKDVAL1	RW	-	Data Fetch Break Point 1 – Data Value
1F0054	MSKDVAL1	RW	-	Data Fetch Break Point 1 – Data Value Mask
1F0058	BRKDRW1	RW	-	Data Fetch Break Point 1 – Rear or Write Condition
1F005C	DESAV	RW	-	Debug Mode Scratch Pad Register
1F0060	BRKDST2	RW	-	Data Fetch Break Point 1 - Starting Address Value
1F0064	MSKDST2	RW	-	Data Fetch Break Point 1 - Starting Address Mask
1F0068	BRKDEND2	RW	-	Data Fetch Break Point 1 - Ending Address Value
1F006C	MSKDEND2	RW	-	Data Fetch Break Point 1 - Ending Address Mask
1F0070	BRKDVAL2	RW	-	Data Fetch Break Point 1 – Data Value
1F0074	MSKDVAL2	RW	-	Data Fetch Break Point 1 – Data Value Mask
1F0078	BRKDRW2	RW	-	Data Fetch Break Point 1 – Rear or Write Condition
1F007C	DEPC	RO`	TA	Debug Exception Program Counter
Watch Dog Timers				
1F0080	WDTEXP	RW	TA	Watch Dog Expiration Value
1F0084	WDTCNT	RO	-	Watch Dog Current Count
1F0088	WDTCFG	RW	TA	Watch Dog Configuration
1F008C	STACKOVF	RW	TA	Stack overflow detection address register
Timers				
1F0090	TIMER1CMP	RW	-	Timer 1 Compare Register

1F0094	TIMER1CNT	RW	-	Timer 1 Counter
1F0098	TIMER2CMP	RW	-	Timer 2 Compare Register
1F009C	TIMER2CNT	RW	-	Timer 2 Counter
1F00A0	TIMER3	RW	-	Timer 3
1F00A4	TIMER4	RW	-	Timer 4
1F00A8	TIMER34CFG	RW	-	Timer 3 and Timer 4 Configuration
1F00AC	TIMERSTAT	RW	-	Timer Status
Essential Analog Peripherals				
1F00B0	REGTRM	RW	TA	1.8V Regulator Trim
1F00B4	LVDCFG	RW	TA	Low Voltage Detect configuration and status
1F00B8	OSCCFG	RW	TA	IOSC, XOSC and clock select configuration
1F00BC	PLLCFG	RW	TA	PLL configuration
Cache Controller				
1F1000	CACHECFG	RW	TA	Cache Configuration
1F1004	CPFCMD	RW	TA	Cache Profile Indirect Access Command Register
1F1008	CPFDAT	RW	TA	Cache Profile Indirect Access Data Register
1F100C	IPFCOUNT	RW	TA	Instruction Execution Profile Counter.
E-Flash Controller				
1F1100	EFLHCMD	RW	TA	E-Flash Controller Command Register
1F1104	EFLHADDR	RW	-	E-Flash Controller Address Register
1F1108	EFLHDATA	RW	-	E-Flash Controller Data Register
1F1110	EFLHPCT1	RW	TA	E-Flash Protection Zone for 1st 64KB
1F1114	EFLHPCT2	RW	TA	E-Flash Protection Zone for 2nd 64KB
SPI-Flash Controller				
1F1200	SFCCFG	RW	TA	S-Flash Controller Configuration Register
1F1204	SFCCMD	RW	TA	S-Flash Controller Command Register
1F1208	SFCSTAT	RO	-	S-Flash Controller Status
1F1210	SFCARG0	RW	-	S-Flash Controller Command Argument 0
1F1214	SFCARG1	RW	-	S-Flash Controller Command Argument 1
1F1218	SFCARG2	RW	-	S-Flash Controller Command Argument 2
1F121C	SFCSTALLT	RW	TA	S-Flash Controller CPU Stall Time Out Setting
I^2C Master				
1F2100	I2CMCFG0	RW	TB	I^2C Master Configuration and Status
1F2104	I2CMSA0	RW	-	I^2C Master Target Slave Address
1F2108	I2CMBUF0	RW	-	I^2C Master Data Buffer Register
I^2C Slave				
1F2180	I2CSCFG0	RW	TB	I^2C Slave Configuration and Status
1F2184	I2CSBUF0	RW	-	I^2C Slave Data Buffer Register
SPI Controller				
1F2200	SPICFG0		TB	SPI Controller Configuration
1F2204	SPISTA0		-	SPI Controller Status
1F2208	SPIBUF0		-	SPI Data buffer Register
EUART0, EUART1, EUART2				
1F2300	SCONFG0	RW	TB	EUART0 Configuration Register
1F2304	SBAUD0	RW	TB	EUART0 Baud Rate Setting Register

1F2308	SBUF0	RW	-	EUART0 Data Buffer Register
1F230C	SSTAT0	RW	-	EUART0 Status Register
1F2310	SFITIMER0	RW	TB	EUART0 Frame and Idle Timer
1F2320	SCONFG1	RW	TB	EUART1 Configuration Register
1F2324	SBAUD1	RW	TB	EUART1 Baud Rate Setting Register
1F2328	SBUF1	RW	-	EUART1 Data Buffer Register
1F232C	SSTAT1	RW	-	EUART1 Status Register
1F2330	SFITIMER1	RW	TB	EUART1 Frame and Idle Timer
1F2340	SCONFG2	RW	TB	EUART2 Configuration Register
1F2344	SBAUD2	RW	TB	EUART2 Baud Rate Setting Register
1F2348	SBUF2	RW	-	EUART2 Data Buffer Register
1F234C	SSTAT2	RW	-	EUART2 Status Register
1F2350	SFITIMER2	RW	TB	EUART2 Frame and Idle Timer
Motor PWM Controller				
1F2800	PCACFG	RW	TD	PCA Configuration
1F2804	PCACNT	RO	TD	PCA Counter
1F2808	PCAPRD	RW	-	PCA Period Register
1F2810	CMPAS	RW	-	PWM Channel A Compare Set Register
1F2814	CMPAR	RW	-	PWM Channel A Compare Reset Register
1F2818	CHACFG	RW	TD	PWM Channel A Configuration
1F2820	CMPBS	RW	-	PWM Channel B Compare Set Register
1F2824	CMPBR	RW	-	PWM Channel B Compare Reset Register
1F2828	CHBCFG	RW	TD	PWM Channel B Configuration
1F2830	CMPCS	RW	-	PWM Channel C Compare Set Register
1F2834	CMPCR	RW	-	PWM Channel C Compare Reset Register
1F2838	CHCCFG	RW	TD	PWM Channel C Configuration
1F2840	CHFORCE	RW	TD	PWM Channel Force Register
1F2844	CHSTATUS	RO	-	PWM Channel Status Register
1F2848	DEADTIME	RW	TD	Dead Time Duration
1F2850	PRCTCFG	RW	TD	Protection Configuration
1F2854	PRCTSTAT	RW	-	Protection Status
1F2858	PINTCFG	RW	TD	PWM Interrupt and Synchronization Configuration
1F285C	PINTSTAT	RW	-	PWM Interrupt Status
1F2860	ITCMP0	RW	-	Interrupt and Synchronization Compare Register 0
1F2864	ITCMP1	RW	-	Interrupt and Synchronization Compare Register 1
1F2868	ITCMP2	RW	-	Interrupt and Synchronization Compare Register 2
1F286C	ITCMP3	RW	-	Interrupt and Synchronization Compare Register 3
1F2870	ITCMP4	RW	-	Interrupt and Synchronization Compare Register 4
1F2874	ITCMP5	RW	-	Interrupt and Synchronization Compare Register 5
1F2880	PINMOTORU	RW	TD	MOTORU pin configuration
1F2884	PINMOTORV	RW	TD	MOTORV pin configuration
1F2888	PINMOTORW	RW	TD	MOTORW pin configuration
1F2890	PINMOTORX	RW	TD	MOTORX pin configuration
1F2894	PINMOTORY	RW	TD	MOTORY pin configuration
1F2898	PINMOTORZ	RW	TD	MOTORZ pin configuration

1F28A0	SPCACNT	RW	-	SPCA Counter Register
1F28A4	SPCAPRD	RW	-	SPCA Period Register
1F28A8	SCMPDS	RW	-	PWM Channel D Compare Register
1F28AC	SCMPES	RW	-	PWM Channel E Compare Register
1F28B0	SITCMP0	RW	-	SPCA Interrupt and Synchronization Compare Register 0
1F28B4	SITCMP1	RW	-	SPCA Interrupt and Synchronization Compare Register 1
Pipe Line ADC				
1F2900	PADCCFG	RW	TD	Pipe Line ADC Configuration and Status.
1F2904	PADINTF	RW	-	Pipe Line ADC Interrupt Flag
1F2910	PADCDATA0	RO	-	Pipe Line ADC Conversion Result of Trigger 0 by ITCMP0
1F2914	PADCDATA1	RO	-	Pipe Line ADC Conversion Result of Trigger 1 by ITCMP1
1F2918	PADCDATA2	RO	-	Pipe Line ADC Conversion Result of Trigger 2 by ITCMP2
1F291C	PADCDATA3	RO	-	Pipe Line ADC Conversion Result of Trigger 3 by ITCMP3
1F2920	PADCDATA4	RO	-	Pipe Line ADC Conversion Result of Trigger 4 by ITCMP4
1F2924	PADCDATA5	RO	-	Pipe Line ADC Conversion Result of Trigger 5 by ITCMP5
1F2928	PADCDATA6	RO	-	Pipe Line ADC Conversion Result of Trigger 6 by SITCMP0
1F292C	PADCDATA7	RO	-	Pipe Line ADC Conversion Result of Trigger 7 by SITCMP1
Window Comparator				
1F2970	CREFCFG	RW	TD	Comparator Reference Setting
1F2974	CMPCHA	RW	-	Channel A Configuration and Status
1F2978	CMPCHB	RW	-	Channel B Configuration and Status
1F297C	CMPCHC	RW	-	Channel C Configuration and Status
1F2980	CMPCHD	RW	-	Channel D Configuration and Status
1F2984	CMPCHE	RW	-	Channel E Configuration and Status
SAR ADC				
1F2A00	SADCCFG	RW	TD	SAR ADC Configuration and Command Register.
1F2A04	SADCDATA	RO	-	SAR ADC Conversion Result
GPIO				
1F2F00	PORT0	RW	TC	Port 0 Configuration Register
1F2F04	PORT1	RW	TC	Port 1 Configuration Register
1F2F08	PORT2	RW	TC	Port 2 Configuration Register
1F2F0C	PORT3	RW	TC	Port 3 Configuration Register
1F2F10	PORT4	RW	TC	Port 4 Configuration Register
1F2F14	PORT5	RW	TC	Port 5 Configuration Register
1F2F18	PORT6	RW	TC	Port 6 Configuration Register
1F2F1C	PORT7	RW	TC	Port 7 Configuration Register
1F2F20	PORT8	RW	TC	Port 8 Configuration Register
1F2F24	PORT9	RW	TC	Port 9 Configuration Register
1F2F28	PORT10	RW	TC	Port 10 Configuration Register
1F2F2C	PORT11	RW	TC	Port 11 Configuration Register
1F2F30	PORT12	RW	TC	Port 12 Configuration Register
1F2F34	PORT13	RW	TC	Port 13 Configuration Register
1F2F38	PORT14	RW	TC	Port 14 Configuration Register
1F2F3C	PORT15	RW	TC	Port 15 Configuration Register
1F2F40	PORT16	RW	TC	Port 16 Configuration Register

1F2F44	PORT17	RW	TC	Port 17 Configuration Register
1F2F48	PORT18	RW	TC	Port 18 Configuration Register
1F2F4C	PORT19	RW	TC	Port 19 Configuration Register
1F2F50	PORT20	RW	TC	Port 20 Configuration Register
1F2F54	PORT21	RW	TC	Port 21 Configuration Register
1F2F58	PORT22	RW	TC	Port 22 Configuration Register
1F2F5C	PORT23	RW	TC	Port 23 Configuration Register
1F2F60	PORT24	RW	TC	Port 24 Configuration Register
1F2F64	PORT25	RW	TC	Port 25 Configuration Register
1F2F68	PORT26	RW	TC	Port 26 Configuration Register
1F2F6C	PORT27	RW	TC	Port 27 Configuration Register
1F2F70	PORT28	RW	TC	Port 28 Configuration Register
1F2F74	PORT29	RW	TC	Port 29 Configuration Register. Not present in CS6257.
1F2F78	PORT30	RW	TC	Port 30 Configuration Register. Not present in CS6257.
1F2F7C	PORT31	RW	TC	Port 31 Configuration Register. Not present in CS6257.
1F2F80	GPINTCFG1	RW	TC	Port 0-31 High Level Interrupt Enable Register
1F2F84	GPINTCFG2	RW	TC	Port 0-31 Low Level Interrupt Enable Register
1F2F88	GPINTCFG3	RW	TC	Port 0-31 Rising Edge Interrupt Enable Register
1F2F8C	GPINTCFG4	RW	TC	Port 0-31 Falling Edge Interrupt Enable Register
1F2F90	GPINTSTAT	RW	-	Port 0-31 Interrupt Status

NOTE: All register access must be in double word format. No byte or word access is supported.

2.5 CPU Interrupts

The CPU has 32-channel hardware interrupts. When any enabled interrupt occurs, CPU disables interrupts (the hardware will set the m bit in PSW thus mask out all further interrupt). And then CPU jumps to the location specified in the IRQBASE register. This is where a global interrupt service routine resides. The global interrupt service then should use IRQVECT to index a jump table for servicing the highest priority interrupt. The interrupt is enabled (m bit in PSW is cleared by the hardware) when return from interrupt instruction (RETI) is executed. Please note the interrupt disabling only affects the blocking interrupts. A non-blocking interrupt such as memory error or WDT overflow will still interrupt the CPU operations.

The native interrupt hardware described above thus does not support interrupt nesting. It is recommended that the interrupt service routine should be kept as short as possible and should use task threading to service the required peripherals. The nesting of interrupt can be realized by software by manually enabling preserving PCRS, PC chain registers and then enabling the m bit in PSW. Software also need to maintain the level of nesting as well restoring the PCRS, and PC chain when returning from deeper level of interrupt.

There is no hardware differentiation in terms of interrupt priority. The priority of interrupt is up to the implementation in the global interrupt service routine. An indexed vector for the highest assigned channel of interrupt can be obtained from IRQVECT register, and this can be used to index to a jump table for servicing. On the other hand, IRQVECT can be ignored and examine all active interrupt status at IRQSTATUS register and decide which interrupt to service first. The 32 channels of hardware interrupt are assigned in the following table.

IRQCH	TYPE	DESCRIPTION
31	NB	Memory Alignment Error and Stack Overflow Error
30	B	Reserved.
29	B	Reserved
28	NB	Watch Dog Timer. Low Voltage Detect.
27	B	Motor Protection
26	B	SPCA Interrupt including SPCA=0, SITCMP0 and SITCMP
25	B	MPCA Interrupt including ITCMP0 to ITCMP5, and MPCA Zero, Period
24	B	Embedded Flash Controller
23	B	External SPI Flash Controller
22	B	Timer 4
21	B	Timer 3
20	B	Window Analog Comparator
19	B	Reserved
18	B	Pipeline ADC EOC By Trigger 6 and 7 (SPCA Trigger SITCMP0-1)
17	B	Pipeline ADC EOC By Trigger 0 to 5 (MPCA Trigger ITCMP0-5)
16	B	Reserved
15	B	SAR ADC
14	B	Reserved
13	B	Reserved
12	B	Reserved
11	B	Reserved
10	B	Reserved
9	B	External GPIO Port
8	B	CAN Controller
7	B	SPI Controller
6	B	I^2C Master 0
5	B	I^2C Slave 0
4	B	Serial Interface EUART2

IRQCH	TYPE	DESCRIPTION
3	B	Serial Interface EUART1
2	B	Serial Interface EUART0
1	B	TIMER 2 Match.
0	B	TIMER 1 Match.

IRQBASE (Interrupt Service Routine Base Address) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-24	-	-	-	Reserved
23-2	IRQ_BASE [23-2]	RW	0x4000	This defines the starting address for the global interrupt service routine. Each interrupt needs to be indexed by the global service routine.
1:0	IRQ_BASE [1-0]	RO	0x00	Always 0 so the service routine always start at word boundary

This register stores the starting address of the global interrupt service routine. Note this is in double-word boundary and the lower two bits are always 0.

IRQVECT (Interrupt Priority Vector)

BITS	NAME	RW	DEF	DESCRIPTION
31-6	-	-	-	Reserved
5-0	PVECTOR [5-0]	RO	0x00	Encoded active highest priority interrupt. The value is equal to the highest priority interrupt plus 1. This can be used for the global ISR to index to the highest priority interrupt ISR.

IRQMASK (Interrupt Mask) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-0	IRQ_MASK [31-0]	RW	0x0000 0000	Individual bit masks the corresponding IRQ channel. Set the corresponding bit to 1 to enable the corresponding IRQ. Set the bit to 0 will disable the IRQ channel.

IRQSTAT (Interrupt Status)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	IRQ_STATUS [31-0]	RO	0x0000 0000	Indicate the status of corresponding IRQ channels. This register is read only, and the status is cleared when the source of the IRQ is cleared.

One important software error in real-time system is stack overflow. In typical tool chain for software development, CPU general purpose register R29 is used for stack pointer. To ensure CPU get notified when stack overflow, a special interrupt condition is devised that compare R29 value. This interrupt is shared with Memory Alignment IRQ and is non-blocking.

STACKOVF (Stack Overflow Detection Address) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-26	-	-	-	Reserved
25	STKOVF	RW	0	This bit is set to 1 by hardware when R29[23-0] >= STACK_OVF[23-0]. R29 is used as Stack Pointer thus this indicates a stack overflow has occurred. This bit must be cleared by software.
24	STKOVEN	RW	0	Enable the Stack Overflow Detection. Set this bit to 1 will enable the detection and generation of the interrupt. Set this bit to 0 will disable the detection.
23-0	MAXSP[23-0]	RW	0	This defines the maximum Stack Point value for overflow detection.

2.6 Debug Mode

The CPU operates in two modes – normal mode and debug mode. Debug mode is entered when a debug exception occurs and CPU branches to 0xF00200 in EJTAG address space to fetch instruction. Memory space 0xF00000 to 0xFFFFFF is called Debug Memory Segment (DMSEG) and is mapped to ETAG access. The instructions and program execution is thus handed over to a host environment through EJTAG interface. The host debugging environment use debug software (stored in the host) residing in DMSEG to achieve debug operation such as register download, memory dump, and new break point setting. The debug mode is exited upon execution of DBGRET (Debug Mode Return) instruction. During the debug mode, all interrupts (and any further debug exceptions) are disabled. There are five types of debug exceptions as listed in the following table.

Exception Source	DESCRIPTION
Software BP	Software Debug Break Point. This is triggered by executing SDBBP instruction. This is usually used to insert software break point.
Single Step	Single Step Debug. This is triggered for every instruction execution if single step debug is enabled. The exception occurs at each instruction completion of the normal mode.
Data BP	Data Fetch Break Point. This exception is triggered by comparing the CPU data access with a predefined condition. Two data break point conditions can be defined.
Instruction BP	Instruction Fetch Break Point. This exception is triggered by comparing the CPU instruction access with a predefined condition. Two instruction break point conditions can be defined.
EJTAG BP	EJTAG Break Point. This exception is initiated by EJTAG which is normally controlled by the debugging host. This is triggered by host setting the EJTAG ECR[EJTAGBRK] bit.

The following registers are related in Debug Mode and are implemented according to the MIPS EJTAG and Debug specifications. These registers are used by host debugging software to implement the debug service routine (DSR). Please note debugging operation has strong relationship with EJTAG and break point setting. The register definitions in EJTAG and break points should also be considered when using the debug related operations.

DEBUGCTL (Debug Control Register DCR) (MIPS Required)

BITS	NAME	RW	DEF	DESCRIPTION
31-30		RO	0	Reserved and hardwired to 0.
29	ENM	RO	1	Processor Endian. Indicate Endianness of the DUT process is running. MIPS-X runs big Endian. Therefore, this is hardwired to 1.
28-18	-	-	-	Reserved and hardwired to 0.
17	DATABRK	RO	1	Data Break Point Capability. Indicate if Hardware Data Break Point is implemented. This is hardwired to 1.
16	INSTBRK	RO	1	Instruction Break Point Capability Indicate if Hardware Instruction Break Point is implemented. This is hardwired to 1.
15-5	-	RO	0	Reserved and hardwired to 0.
4	INTE	RO	1	This is a mirror of PSW[5] which is the mask bit for blocking interrupts. 1 indicates enable state, and 0 indicates disable state.
3	NMIE	RO	1	This is a mirror of PSW[6] which is the mask bit for non-blocking interrupts. 1 indicates enable state, and 0 indicates disable state.
2	NMIPEND	RO	0	Indicate if there is pending non-blocking IRQ in the normal mode. 1 means pending.
1	-	-	0	Reserved and hardwired to 0.
0	PROBEN	RO	0	Indicate the value of PROBEN bit in the EJTAG Control Register (ECR). This bit only acts a

This register is required and implemented according to MIPS EJTAG debug specifications. This register is used by DSR to control and provide information about debug operations. It allows global control of interrupt enable in the normal mode and also allows DSR to know any pending interrupt. All interrupts (blocking or non-blocking) are always disabled in the debug mode by hardware.

DEBUG (Debug Register) (MIPS Required) TA

BITS	NAME	RW	DEF	DESCRIPTION
31	DBD	RO	0	Indicates whether the latest debug exception that causes the entry into debug mode, or the latest exception occurred in pipeline delay slot of a branch or jump instructions. DBD=1 indicates there is exception occurred during delay slot. DBD=0 indicates there is no exception.
30	DMODE	RO	0	DMODE=1 indicates the processor is in debug mode. DMODE=0 indicates the processor is in normal mode.
29	NODCR	RO	0	NODCR=0 indicates debug segment (F00000 to FFFFFF) is present. This is hardwired to 0.
28	LSNM	RO	0	LSNM=0 indicates debug segment is available for load and store instructions. This is hardwired to 0.
27-26	-	RO	0	Reserved and hardwired to 0.
25	COUNTDM	RW	0	This bit is used to enable the timers (TIMER1, TIMER2, TIMER3, TIMER4, and WDT) in debug mode. If it is 0, the timers stop increment in the debug mode. If it is 1, the timers continue to increment in the debug mode.
24-20	-	RO	0	Reserved and hardwired to 0
19	DDBSIMPR	RO	0	DDBSIMPR=1 indicates a Data Store Break exception has occurred. This is cleared when exiting the debug mode. CS6257 only implements imprecise data break point.
18	DDBLIMPR	RO	0	DDBLIMPR=1 indicates a Data Load Break exception has occurred. This is cleared when exiting the debug mode. CS6257 only implements imprecise data break point.
17-15	VER[2-0]	RO	010	It is hardwired to 010 to indicate EJTAG version 2.6.
14-10	-	RO	0	Reserved and hardwired to 0.
9	NOSST	RO	0	NOSST=0 indicates that single step debug mode is implemented. This is hardwired to 0.
8	SST	RW	0	SST=1 enables single step mode. If SST=1, a single step debug exception is triggered after every instruction completion in normal mode. SST=1 does not generate any further debug exception once in debug mode.
7	-	RO	0	Reserved and hardwired to 0.
6	DLSLOT	RO	0	Indicate which delay slot for the latest exception occurred in the pipeline delay slot of a branch or jump instruction. This is only meaningful if DBD=1. DLSLOT=0 indicates delay slot 1, DLSLOT=1 indicates delay slot 2.
5	-	RO	0	Reserved and hardwired to 0.
4	DIB	RO	0	DIB=1 indicates an Instruction Break Point debug exception has occurred. This is cleared when exiting the debug mode.
3	DDBS	RO	0	CS6257 does not implement precise data break point. This bit is hardwired to 0.
2	DDBL	RO	0	CS6257 does not implement precise data break point. This bit is hardwired to 0.
1	DBP	RO	0	DBP=1 indicates a Software Break debug exception has occurred. This

BITS	NAME	RW	DEF	DESCRIPTION
				is cleared when exiting the debug mode.
0	DSS	RO	0	DSS=1 indicates a Single Step Break debug exception has occurred. This is cleared when exiting the debug mode.

DEPC (Debug Exception Program Counter) (MIPS Required) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-24	-	-	-	Reserved
23-0	DBGRPC [23-0]	RW	0x0000	DBGRPC[23-0] contains the program counter value for last debug exception occurrence. It is reloaded into PC at execution of DERET instruction to return to the exception point. It is modifiable through register access or through MOVTOSF instruction but is strongly recommended not change its value.

DESAV (Debug Mode Scratch Pad 0 Register) (MIPS Required)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	DESAV [31-0]	RW	0x0000	This register is a general purpose R/W register and can be used by the debug service routine. This allows the DSR to preserve the CPU state without using CPU's registers.

2.7 EJTAG Interface

The CPU also includes an EJTAG controller which can be used as a debug and ISP interface with a host. The EJTAG controller implements a standard MIPS EJTAG specification version 2.6. The EJTAG is tightly coupled with break point and debugging features of the CPU, and is also associated with boundary scan. This section describes the EJTAG controller only. The EJTAG has a TAP (Test Access Port) consisting of TCK, TMS, TDI, TDO and TRSTN pins. These pins follow standard JTAG definitions including the state diagram and timing requirement. Each EJTAG transfer between the EJTAG controller and a host is comprised of EJTAG Instruction Register and Data Register transfer. The EJTAG interface is locked at power-on and because the EJTAG interface is used for debug as well as ISP, to ensure code security, the EJTAG is unlocked only if a predefined 8-byte key is matched against an 8-byte security signature stored in the embedded flash location 20_0000 to 20_0007. Under locked condition, only limited instructions can be issued through EJTAG such as IDCODE, and EFCMD (verify or main block erase). The available instruction is shown in the table below. The following EJTAG instructions are implemented, and all instruction code is 8-bit. All these instructions and associated registers are local to EJTAG controller, and are not accessible from CPU side while some of the register bits are mirrored to and from the DCR (Debug Control Register). Also the EJTAG clock (TCK must be kept no higher the one fourth of the system clock). For example, if SYSCLK=8MHz, then the TCK can not exceed 2MHz. Also, please note, after reset, SYSCLK is from XOSC. As a result, in general the EJTAG must not exceed one fourth of the XOSC clock rate.

INST CODE	Y N	INSTRUCTION	DESCRIPTION
0x00	Y	EXTEST	External Pin Test. This instruction causes the TDI and TDO to be connected to the Boundary Scan Chain. The device's pin states are sampled with the 'capture' JTAG state and new values are shifted into the BSR with the 'shift' state; these values are then applied to the pins of the device using the 'update' state.
0x01	Y	IDCODE	Device ID Register This instruction accesses the EJTAG DEVICEID register.
0x02	Y	UNLOCK	Unlock EJTAGEJTAG This instruction is used to unlock the EJTAG. This instruction must be followed by 8-byte of key data that matches with the security signature to unlock the EJTAG. After the 8-byte of key, additional 8 bytes data of “10100101” must be followed to complete the unlock sequence. Flash Mass Erase This instruction can also be used to issue a Flash Mass Erase operation. If the first 8-bytes of key is all “00000000”, and the followed 8-bytes matched “01011010” data exactly, this will initiate an E-Flash Main Memory Mass Erase operation. The host needs to wait at least 100msec to issue any new EJTAG instruction.
0x03	Y	IMPCODE	Implementation Register This instruction access the EJTAG Implementation Register
0x04	N	EFADDATA	E-Flash Data and Address Register. This direct the TAP to E-Flash controller’s data and address register for read and write, as well as sector erase operations. Bit 31-16 Flash controller address Bit 15-0 Flash controller data
0x05	N	EFCMD	E-Flash Control Command Register This directs the EJTAG TAP to E-Flash controller command register. Bit 0: E-Flash MM Word Read Bit 1: E-Flash IFB Word Read Bit 2: E-Flash MM Word Write Bit 3: E-Flash IFB Word Write Bit 4: E-Flash MM Sector Erase Bit 5: E-Flash IFB Erase

INST CODE	Y N	INSTRUCTION	DESCRIPTION
			Other bits are ignored. If more than one bit is set, then the command is not executed and returned with fail status.
0x06	Y	EFSTATUS	EJTAG and E-Flash Status This instruction must be followed by one dummy byte of data. As the data byte is shifted in TDI, the current EJTAG and E-Flash status is also shifted out at TDO. This status is not updated until new command is issued. Bit 0: EJTAG Lock Status. 0 means LOCK, 1 means UNLOCK. Bit 1: E-Flash Busy. 0 means E-Flash is idle. 1 means E-Flash is busy. Bit 2: E-Flash Command Status. 0 means command successful. 1 means failure Bit 3 to 7 are 0.
0x07	Y	SAMPLD	Sample and Preload This instruction causes the TDI and TDO to be connected to the Boundary Scan Chain. However, the device is left in its normal functional mode. During this instruction, the chain can be accessed by a data scan operation to take a sample of the functional data entering and leaving the device. The instruction is also used to preload test data into the BSR prior to loading an EXTEST instruction. And the difference from EXTEST is that it performs sample and shift but not update the chain.
0x08	N	ADDRESS	Address Register used to access the CPU address bus.
0x09	N	DATA	Data Register used to access the CPU data bus.
0x0A	N	CONTROL	EJTAG Control Register (ECR) use for control and status.
0x0B	N	ALL	Access the EJTAG ADDRESS, DATA and CONTROL Registers in one chain.
0x0C	N	EJTAGBOOT	Cause an internal reset flag to be set so the processor take an EJTAP BP exception after manual reset.
0x0D	N	NORMALBOOT	Cause the reset flag to be cleared so the processor will take normal reset execution after manual reset.
0x0E	N	FASTDATA	Select the Data and Fast Data register
0x0F	N	Reserved	
0x10-0x1B	N	Reserved	
0x1F	Y	BYPASS	Select Bypass Register. This is used to

**** The Y/N column indicates if this instruction is available under EJTAG locked state.

IDCODE instruction directs the content of EJTAG Device ID Register to the EJTAG DOUT. Device ID Register is defined as following, and is hardwired and read only. The value is 32h'062576EF.

EJTAG DEVICEID REGISTER

BITS	NAME	RW	DEF	DESCRIPTION
31-28	VERSION	RO	0000	Indicate the version of the device.
27-12	PARTNO	RO	16h'6257	Indicate the device number. It is hardwired to 6257 for CS6257.
11:1	MANUFID	RO	11h'377	Manufacture ID is "011_0111_0111"
0	REQ	RO	1	Always 1.

IMPCODE instruction directs the content of EJTAG Implementation Register to the EJTAG output. This register contains the information of the processor of the device. The value is 32h'40004000

EJTAG IMPLEMENTATION REGISTER

BITS	NAME	RW	DEF	DESCRIPTION
31-29	EJTATVER	RO	3b'010	Indicate the version of the EJTAG. 010 means version 2.6.
28	R4K3K	RO	0	Indicate the device number. It is hardwired to 0 to indicate 3K series.
27-25	-	RO	0	Always 0.
24	DINTSUP	RO	0	Indicate support of DINT signal from EJTAG Probe. This should be 0 because we do not have this
23	-	RO	0	Always 0.
22-21	ASIDSIZE	RO	0	ASID field size. 0 means no ASID is implemented in MIPS-X.
20-17	-	RO	0	Always 0.
16	MIPS16	RO	0	Indicate if MIPS16. 0 for not support
15	-	RO	0	Always 0.
14	NODMA	RO	1	Indicate if EJTAG has DMA support. 1 means no DMA.
13-1	-	RO	0	Always 0
0	MIPS64	RO	0	Indicate MIPS 32-bit or 64-bit. 0 for MIPS-X

CONTROL instruction directs the EJTAG TAP to EJTAG Control Register for read and write from the host. It is the main channels of exchanging status and control between the host and the CPU. The ECR handles the processor reset and soft reset indication, debug mode indication, access start, finish and size as well as read/write indication. ECR also plays the role to interact with CPU for debug exception request.

EJTAG_CONTROL_REGISTER

BITS	NAME	RW	DEF	DESCRIPTION
31	ROCC	R/W 0	1	Set by MIPS-X reset condition. This bit must be cleared by the debugging host to allow any EJTAG operations. Writing 1 by host is ignored. The host must set this bit to 0 in order to modify any bit value in this register.
30-29	PSZ[1-0]	RO	0	Indicate the size of a pending process access. Host reads and interprets this along with the ADDRESS register to support the EJTAG memory access. This field is valid only when a processor is pending. 00: means the pending access is byte 01: means the pending access is word 10: means the pending access is double word
28-23	-	RO	0	Always 0.
22	DOZE	RO	0	Indicates if the processor is in low power mode. MIPS-X does not implement low power mode and it is always 0.
21	HALT	RO	0	Indicates if the system bus in stopped or running. MIPS-X does not have suspended system bus and it is always 0.
20	PERRST	RO	0	Control the peripheral reset. It is not implemented and has no effect.
19	PRNW	RO	0	Indicates read or write of a pending MIPS-X access. This bit is only valid if there is a pending processor access. 0 means a pending MIPS-X read access for a fetch or load. 1 means a pending MIPS-X write access for store.
18	PRACC	R/W 0	0	Indicates a pending MIPS-X access. PRACC is set to 1 by the MIPS-X to let host know there is a pending access. After the access is prepared by the host, the host should write 0 to this bit to complete the transaction. Host can not write 1 into this bit.
17	-	RO	0	Always 0.
16	PRRST	RO	0	Set by host to issue a processor reset. Not implemented and read only with 0.

BITS	NAME	RW	DEF	DESCRIPTION
15	PROBEN	RW	0	This bit is set and cleared by the host. This bit is mirrored to DCR bit 0 as read only so MIPS-X can determine if access to debug segment is available or not.
14	PROBTRAP	RO	0	This bit is set and cleared by the host to control the debug segment address range. In MIPS-X, the debug memory always resides between 0xF00000 – 0xFFFFFF, and this control is not implemented and is read only and always read 0.
13	-	RO	0	Always 0
12	EJTAGBRK	R W1	0	This bit can be set to 1 by the host to initiate a debug exception (EJTAG BP) to the processor. The bit is cleared by CPU hardware automatically after entering debug mode. Writing 1 when already in debug mode is ignored. Writing 0 is also ignored. Reading 0 indicates that there is no pending request. Reading 1 indicates that there is a pending EJTAG BP but debug mode is not entered yet.
11-4	-	RO	0	Always 0.
3	DM	RO	0	This bit is set by the MIPS-X5 hardware when it is in the debug mode. And is cleared by hardware when MIPS-X5 exits the debug mode. The host read this to determine if MIPS-X5 is in the debug mode.
2-0	-	RO	0	Always 0

2.8 Break Point Logic

The break point logic in CPU allows flexible ways in software debugging. All break points are based on value of address and data buses, and can be categorized as either instruction fetch or data fetch. Thus it is referred to INST BREAK or DATA BREAK.

A program instruction fetch will stall CPU and generates an INSTUCTION BREAK POINT match when the following condition is true:

[(PC & MSKINST1) == (BRKINS1 & MSKINST1)] or [(PC & MSKINST2) == (BRKINS2 & MSKINST2)]

MSKINST1 (Mask for Instruction Fetch Address – Instruction Break Point 1)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	MSKINST1 [31-0]	RW	0X000 00000	Mask the address of instruction fetch break point 1.

BRKINST1 (Instruction Fetch Address – Instruction Break Point 1)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	BRKINST1 [31-0]	RW	0X000 00000	Define the matching address of instruction fetch break point 1. This is used to compare with the program counter.

MSKINST2 (Mask for Instruction Fetch Address – Instruction Break Point 2)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	MSKINST2 [31-0]	RW	0X000 00000	Mask the address of instruction fetch break point 2.

BRKINST2 (Instruction Fetch Address – Instruction Break Point 2)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	BRKINST2 [31-0]	RW	0X000 00000	Define the matching address of instruction fetch break point 2. This is used to compare with the program counter.

As the above suggests, there are two program break pointer conditions can be set and either match will trigger an INST break match.

Similarly, data fetch can also be used to trigger a DATA BREAK match. The data fetch break point compare the CPU's data fetching conditions to generate debug exception. The break match condition of data fetch is specified in more complex manner. The addressing range can be specified, and the data value of arbitrary bit pattern can be specified separately. There are two sets of break points can be used and are enabled through break point The matching condition can be expressed in the following condition:

```
[(ADDR & MSKDSTT) >= (BRKDSTT & MSKDSTT)]
        AND
[(ADDR & MSKDEND) >= (BRKDEND & MSKDEND)]
        AND
[(READ & BRKDREN)
        & (DATA & MSKDVAL = BRKDVAL & MSKDVAL)] ||
[WRITE & BRKDWEN)
        & (DATA & MSKDVAL) = BRKDVAL & MSKDVAL)]
```

The first two terms define the range of address for the break condition. The latter two terms defines the match value of the data fetch and whether read or write operation for the match condition. There are two data fetch break point condition can be set. The setting by registers is defined in the following.

MSKDSTT1 (Mask for Data Fetch Starting Address – Data Break Point 1)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	MSKDSTT1 [31-0]	RW	0X000 00000	Set the mask of the starting address of data fetch break point 1

BRKDSTT1 (Starting Address for Data Fetch – Data Break Point 1)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	BRKDSTT1 [31-0]	RW	0X000 00000	Define the starting address of data fetch break point 1

MSKDEND1 (Mask for Data Fetch Ending Address – Data Break Point 1)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	MSKDEND1 [31-0]	RW	0X000 00000	Set the mask the ending address of data fetch break point 1

BRKDEND1 (Ending Address for Data Fetch – Data Break Point 1)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	BRKDEND1 [31-0]	RW	0X000 00000	Define the ending address of data fetch break point 1

MSKDVAL1 (Mask for Data Value – Data Break Point 1)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	MSKDVAL1 [31-0]	RW	0X000 00000	Set the mask for the data value of data fetch break point 1.

BRKDVAL1 (Data Value – Data Break Point 1)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	BRKDVAL1 [31-0]	RW	0X000 00000	Define the compare value of the data fetch break point 1

BRKDRW1 (Read/Write Condition – Data Break Point 1)

BITS	NAME	RW	DEF	DESCRIPTION
31-3	-	-	-	Reserved
2	MISMATCH	RW	0	Set MISMATCH=1 will use value mismatch condition instead of value match condition
1	BRKDR	RW	0	Set BRKDW=1 will enable the data break point comparison for read data. This can coexist with BRKDW=1.
0	BRKDW	RW	0	Set BRKDW=1 will enable the data break point comparison for write data. This can coexist with BRKDR=1.

MSKDSTT2 (Mask for Data Fetch Starting Address – Data Break Point 2)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	MSKDSTT [31-0]	RW	0X000 00000	Set the mask of the starting address of data fetch break point 2

BRKDSTT2 (Starting Address for Data Fetch – Data Break Point 2)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	BRKDSTT2 [31-0]	RW	0X000 00000	Define the starting address of data fetch break point 2

MSKDEND2 (Mask for Data Fetch Ending Address – Data Break Point 2)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	MSKDEND1 [31-0]	RW	0X000 00000	Set the mask the ending address of data fetch break point 1

BRKDEND2 (Ending Address for Data Fetch – Data Break Point 2)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	BRKDEND1 [31-0]	RW	0X000 00000	Define the ending address of data fetch break point 1

MSKDVAL2 (Mask for Data Value – Data Break Point 2)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	MSKDVAL2 [31-0]	RW	0X000 00000	Set the mask for the data value of data fetch break point 2.

BRKDVAL2 (Data Value – Data Break Point 2)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	BRKDVAL2 [31-0]	RW	0X000 00000	Define the compare value of the data fetch break point 2.

BRKDRW2 (Read/Write Condition – Data Break Point 2)

BITS	NAME	RW	DEF	DESCRIPTION
31-3	-	-	-	Reserved
2	MISMATCH	RW	0	Set MISMATCH=1 will use value mismatch condition instead of value match condition
1	BRKDR	RW	0	Set BRKDW=1 will enable the data break point comparison for read data. This can coexist with BRKDW=1.
0	BRKDW	RW	0	Set BRKDW=1 will enable the data break point comparison for write data. This can coexist with BRKDR=1.

The break point logic is configured using RPCONTROL register. To use the break points, individual break point must be enabled in this register. In the break point service routine, it is also necessary to clear the active flag in this register.

BPCONTROL (Break Point Control and Configuration) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-10	-	-	-	Reserved
9	IBP2EN	RW	0	INST Break Point 1 Enable
8	IBP2FCL	W1	0	Write 1 to clear IBP2F. This is kept to remain compatibility with CS6223. Write 0 to IBP2F will also clear IBP2F.
7	EJTAFFCL	W1	0	Write 1 to clear EJTAGF. This is kept to remain compatibility with CS6223. Write 0 to EJTAGF will also clear EJTAGF.
6	-	-	-	Reserved
5	DBP2EN	RW	0	DATA Break Point 2 Enable
4	DBP1EN	RW	0	DATA Break Point 1 Enable
3	IBP1EN	RW	0	INST Break Point 1 Enable
2	DBP2FCL	W1	0	Write 1 to clear DBP2F. This is kept to remain compatibility with CS6223. Write 0 to DBP2F will also clear DBP2F
1	DBP1FCL	W1	0	Write 1 to clear DBP1F. This is kept to remain compatibility with CS6223. Write 0 to DBP1F will also clear DBP1F
0	IBP1FCL	W1	0	Write 1 to clear IBP1F. This is kept to remain compatibility with CS6223. Write 0 to IBP1F will also clear IBP2F.

The break point status can be obtained by BPSTATUS register. This register is read only. The corresponding flag bit is set to 1 when the related break point occurs. Also note the DATA break point flag is further indicated by read or write condition.

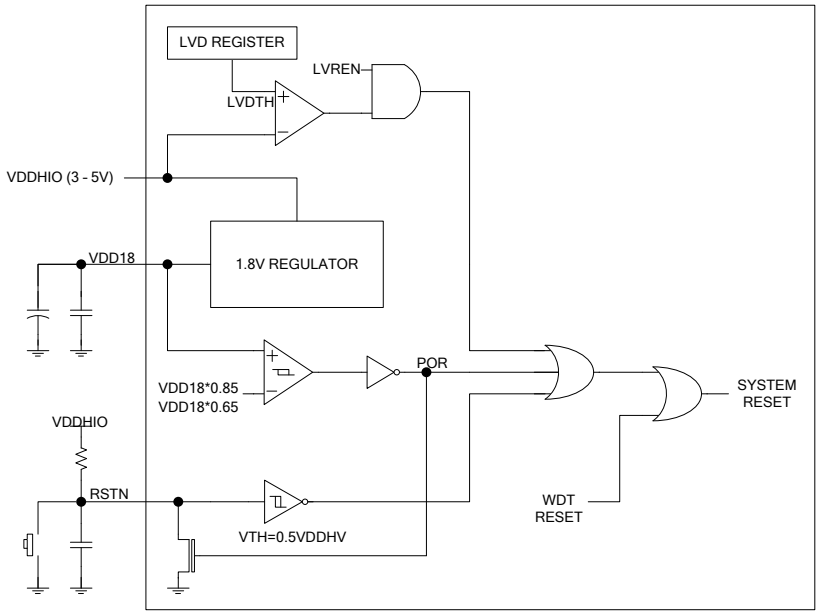
BPSTATUS (Break Point Status and Flag)

BITS	NAME	RW	DEF	DESCRIPTION
31-11	-	-	-	Reserved
9	IBP2F	R W0	0	INST Break Point 2 flag. This bit is set by break point logic when INST BP 2 condition is satisfied. This bit is must be cleared by software by writing 0.
8	EJTAGF	R W0	0	EJTAG BREAK flag. This bit is set by EJTAG logic. This bit is must be cleared by software by writing 0.
7	-	-	-	Reserved
6	DBP2RF	R W0	0	DATA Break Point 2 Reading flag. This bit is set by break point logic when DATA BP 2 with reading condition is satisfied. This bit is must be cleared by software by writing 0.
5	DBP2WF	R W0	0	DATA Break Point 2 Writing flag. This bit is set by break point logic when DATA BP 2 with writing condition is satisfied. This bit is must be cleared by software by writing 0.
4	DBP1RF	R W0	0	DATA Break Point 1 Reading flag. This bit is set by break point logic when DATA BP 1 with reading condition is satisfied. This bit is must be cleared by software by writing 0.
3	DBP1WF	R W0	0	DATA Break Point 1 Writing flag. This bit is set by break point logic when DATA BP 1 with writing condition is satisfied. This bit is must be cleared by software by writing 0.
2	DBP2F	R W0	0	DATA Break Point 2 flag. This bit is set by break point logic when DATA BP 2 with either reading or writing condition is satisfied. DBP2F = (DBP2RF OR DBP2WF).
1	DBP1F	RO	0	DATA Break Point 1 flag. This bit is set by break point logic when DATA BP 1 with reading or writing condition is satisfied. DBPIF = (DBP1RF OR DBP1WF).

BITS	NAME	RW	DEF	DESCRIPTION
0	IBP1F	RO	0	INST Break Point 1 flag. This bit is set by break point logic when INST BP 1 condition is satisfied.

2.9 Reset Conditions

There are several reset sources. The reset circuit block diagram is shown in the following figure. The main reset is from POR (Power On Reset). POR is asserted during power-on process of the 1.8V regulator before it reaches to 85% of its target value. When POR is active, it will also force the RSTN pin to be low, and when POR exits, the reset condition is removed after the external RC time constant on RSTN pin. This ensures a solid reset period before the 1.8V supply voltage is steady. After POR exits, the hysteresis of the comparator shifts the detection threshold to 65% of the target value. There is also low voltage detection on the main supply voltage. The supply voltage range is between 4.5V to 5.5V. The supply voltage detection threshold is programmable from 2.5V to 5.0 in 6-bit precision. The input supply voltage detection can be used as an interrupt or can be configured to generate a reset.



2.10 Watch Dog Timer

The CPU also includes a Watch Dog Timer that can be enabled to ensure that program execution does not enter into dead loop. WDT is clocked by the SYSCLK/256 and is 32-bit wide. When WDT expires, it generates a non-blocking interrupt. If WDT is configured to generate a reset, the reset have the same behavior as the hardware reset. CPU can also access the current count value of WDT.

WDTEXP (Watch Dog Timer Expiration Setting) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-0	WDTEXP [31-0]	RW	0X000 00000	This defines the expiration count of Watch Dog Timer

WDTCNT (Watch Dog Timer Current Count)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	WDTCNT [31-0]	RO	0X000 00000	This reflects current count value of Watch Dog Timer.

WDTCFG (Watch Dog Configuration) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-4	-	-	-	Reserved
3	WDTINTF	WR		WTD IRQ flag. Software must write 0 to clear this flag.
2	WDTCLR	WO		WTD clear. Write 1 to clear the count of WDT. Reading always returns 0.
1	WDTINTEN	RW	0	Interrupt or Reset select. Set this bit to 0 to allow WDT expiration for system reset. Set this bit to 1 to allow WDT expiration to trigger a non-blocking IRQ.
0	WDTEN	RW	0	WDT enable control. Set this bit to 1 to enable WDT counting.

Please note when using WDT enable control, it controls the counting of the WDT. This does not clear the WDT count value. WDT will maintain the count value when transit from enable to disable state. Also, the WDT is forced to stop when entering the break condition.. It is resumed automatically when exiting the break service routine.

2.11 CPU Timers

There are four built-in timers – TIMER1, TIMER2, TIMER3, and TIMER4. These timers can be used to generate interrupts and the interrupt enable mask is controlled in IRQMASK register.

2.11.1 Timer 1 and Timer 2

TIMER1 and TIMER2 are simple free-run timers of 32-bit wide and wrap around automatically when it reaches full count. Both TIMER1 and TIMER2 are clocked by SYSCLK and do not shut down. The interrupt control of TIMER1 and TIMER2 is in the IRQ_MASK register. When corresponding interrupt is enabled, and the count value equal to the trigger value, a timer IRQ is generated. As the timer is continuing incrementing, the trigger condition will only last on cycle of SYSCLK if not latched by other means. For periodic IRQ, the ISR also need to write a new trigger value as the timer is not reset by the trigger condition, or alternatively the counter value can be reset by the software.

TIMER1TRG (Timer 1 Compare Trigger Value)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	TIMER1_TRG [31-0]	RW	0x0000 0000	TIMER1 Trigger When TIMER1CNT[31-0] is equal to TIMER1TRG[31-0], TIMER1 interrupt is generated

TIMER1CNT (Timer 1 Current Count Value)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	TIMER1_CNT [31-0]	RW	0x0000 0000	TIMER1 Count Value When TIMER1CNT[31-0] is equal to TIMER1TRG[31-0], TIMER1 interrupt is generated

TIMER2TRG (Timer 2 Compare Trigger Value)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	TIMER2TRG [31-0]	RW	0x0000 0000	TIMER2 Trigger When TIMER2CNT[31-0] is equal to TIMER2TRG[31-0], TIMER2 interrupt is generated

TIMER2CNT (Timer 2 Current Count Value)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	TIMER2CNT [31-0]	RW	0x0000 0000	TIMER1 Count Value When TIMER2CNT[31-0] is equal to TIMER2TRG[31-0], TIMER2 interrupt is generated

2.11.2 Timer 3

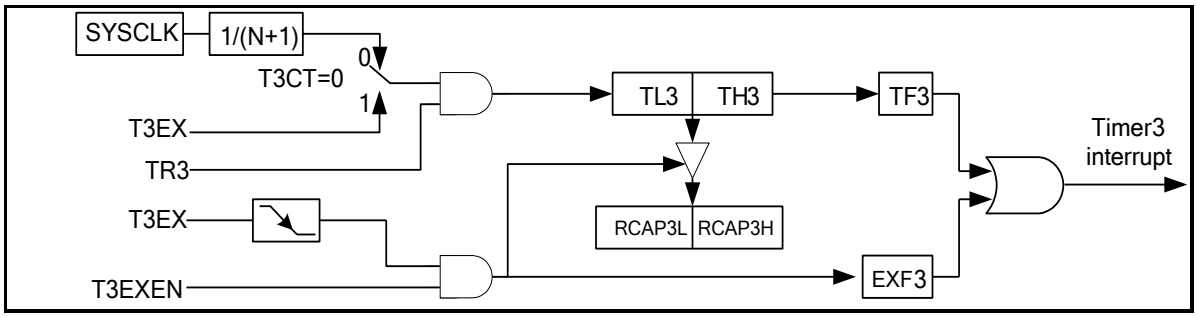
Timer3 is composed of a 16-bit Counter (TH3 and TL3) and a 16-bit Capture Register (RCAP3H and RCAP3L). TIMER3 can be configured for Capture mode which the counter value is captured onto the capture register when external capture event on T3EX occurs. Or it can be configured as a 16-bit Timer/Counter depending on the clock selection of the Counter. When it is used as a Timer, the counter is clocked by SYSCLK/N. When it is used as a Counter, the counter is clocked by the external input T3EX. CT3 bit in the configuration register sets.

TIMER3 (Timer 3 Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-24	TH3[7-0]	RW	0x00	TIMER2 Counter High Byte
23-16	TL3[7-0]	RW	0x00	TIMER2 Counter Low Byte
15-8	RCAP3H[7-0]	RW	0x00	TIMER2 Capture High Byte
7-0	RCAP3L[7-0]	RW	0x00	TIMER2 Capture Low Byte

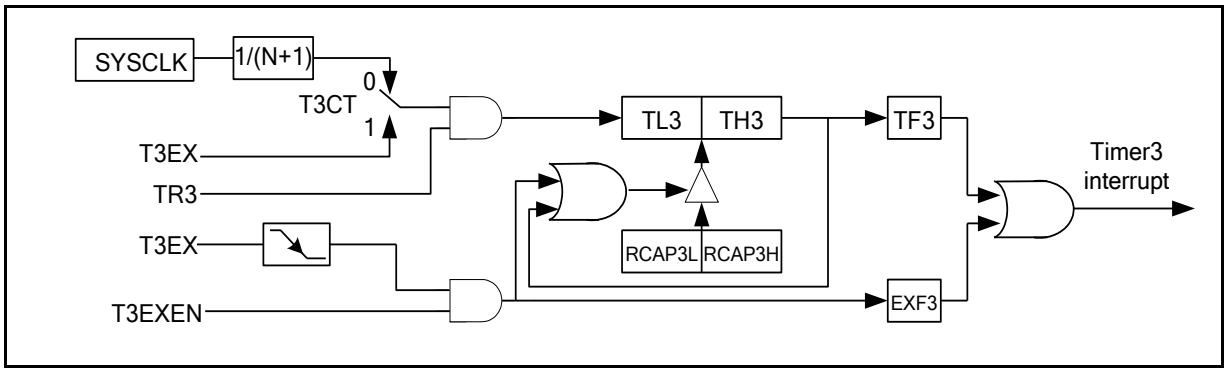
2.11.2.1 16-Bit Capture Mode

This mode is enabled when T3DCEN=X, T3EXEN=1, T3R=1, T3CPRL=1, T3CT=0. Under this mode, the falling edge of the T3EX is used to trigger the capture. At this capture event, the counter value TH3:TL3 is captured onto RCAP3H:RCAP3L. The interrupt is generated at both TH3:TL3 overflow through TF3 or the capture event through EXF3. Since T3EX is used for the triggering, the counter must use SYSCLK/(N+1) as the clock source.



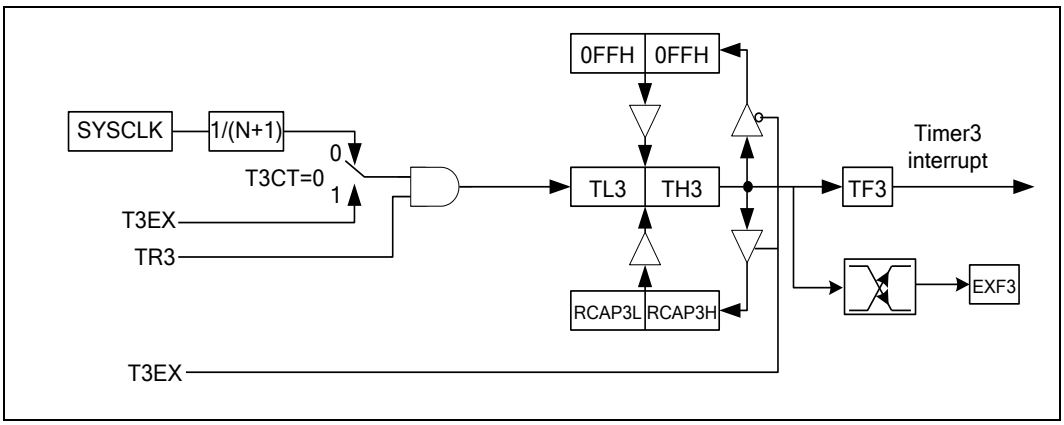
2.11.2.2 16-Bit Auto-Reload UP Timer/Counter Mode

This mode is enabled when T3DCEN=0, T3EXEN=1, T3R=1, T3CPRL=1, T3CT=1/0. In this mode, the counter clock can be selected either as T3EX when T3CT=1, or SYSCLK/(N+1) when T3CT=0. When the counter TH3:TL3 reaches 0xFFFF, it is reloaded with the value in RCAP3H:RCAP3L, TF3 will be set to 1 and interrupt is generated. If the T3EXEN bit is 1 and T3CT=0, the falling edge of T3EX can also be used as a triggering event which causes the reload and interrupt through EXF3.



2.11.2.3 16-Bit Auto Reload UP/DOWN Timer/Counter Mode

This mode is enabled when T3DCEN=1, T3EXEN=1, T3R=1, T3CPRL=1, T3CT=0. This mode is similar to the Auto-Reload UP mode, except that T3EX is used to control the count direction of TH3:TL3 counter, when T3EX=1 is in up-count mode and when T3EX=0 is in down-count mode. Since T3EX is used for direction control, T3CT must be 0 to use SYSCLK/(N+1) as the clock source. When TH3:TL3 is counting up to 0xFFFFh, it is reloaded with RCAP3H:RCAP3L value, in this case, TF3 is set and triggers an interrupt, EXF3 will also be toggled by this event. When TH3:TL3 is counting down to RCAP3H:RCAP3L value, it is reloaded with 0xFFFF, and this set TF3 and also triggers an interrupt, EXF3 will also be toggled by this event.



2.11.3 Timer 4

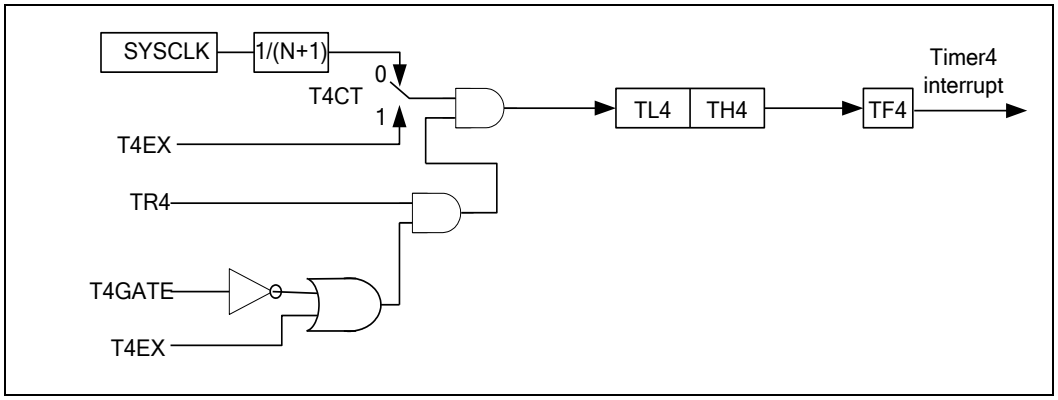
Timer 4 is composed of one 16-bit counter and one 16-bit register/counter. It can be configured either as a cascaded 32-bit Timer/Counter or can be configured as a 16-bit reload timer/counter. The GATEEN input is used to control T4EX when it is used as a counter gating control.

TIMER4 (Timer 4 Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-16	TH4[15-0]	RW	0x00	TH4[15-0]
15-0	TL4[15-0]	RW	0x00	TL4[15-0]

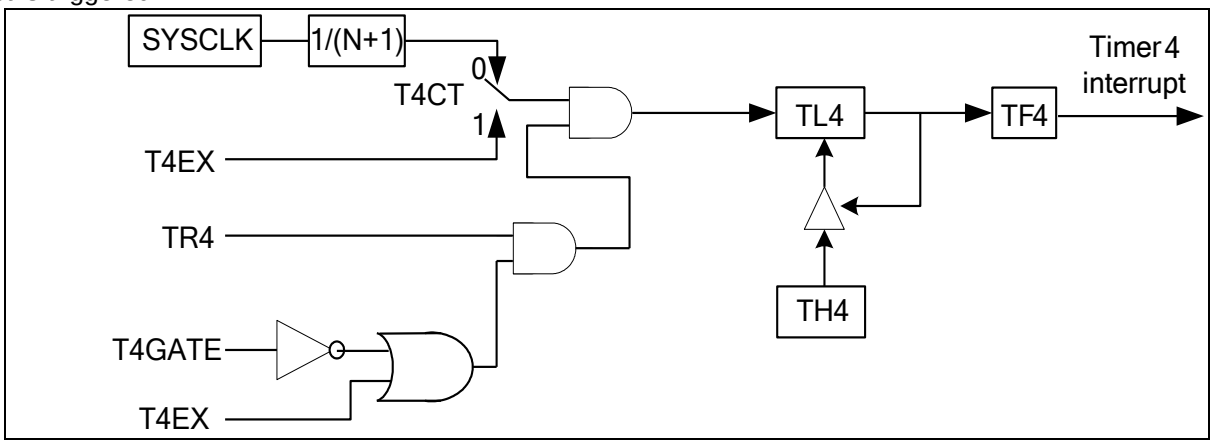
2.11.3.1 32-Bit Timer/Counter

This mode is enabled when T4GATE=0/1, T4R=1, T4RL=0, T4CT=0/1. As a 32-bit Timer/Counter, when the count value overflows from 0xFFFFFFFFh to 0x00000000h, TF4 will be set to 1 and generate an interrupt. In this mode, T4EX can also be used as the gating input and the counter clock source is from SYSCLK/(N+1).



2.11.3.2 16-bit Auto-Reload Timer/Counter

This mode is enabled when T4GATE=0/1, T4R=1, T4RL=1, T4CT=0/1. The counter is in 16-bit mode and is TL4[15-0]. When TL4[15-0] overflow from 0xFFFF, it is reloaded with TH4[15-0] value, and TF4 is set and an interrupt is triggered.



2.11.4 Timer 3 and Timer 4 Configurations And Status Registers

TIMER34CFG (Timer 3/Timer 4 Configuration and Status Register) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-25	-	-	-	Reserved.
24	T4GATE	RW	0	T4 Gate Control This is used to control the T4EX during Timer mode. If T4GATE is set to 0, then T4EX control is disabled.
23	T4CT	RW	0	T4 Counter/Timer Mode Select Setting this bit to 1 selects the T4EX as the clock input and T4 acts in Counter mode. Setting this bit to 0 selects SYSCLK/(N+1) as the clock input and T4 acts in Timer mode.
22	T4RL	RW	0	T4 Reload Mode Select Set this bit to1 configure T4 in 16-bit Reload Timer/Counter Mode. Set this bit to 0 configure T3 in 32-bit Timer/Counter Mode
21	T4R	RW	0	T4 Run/Stop Control Timer 4 Run control. This bit should be set to 1 to allow the counter in T4 counting. When T4R is 0, the counter stops counting and 43R=0 does not clear the counter.
20-13	T4DIV[7-0]	RW	0x00	T4 SYSCLK Divider N SYSCLK is divided by (N+1) as T4's clock
12	T3CT	RW	0	T3 Counter/Timer Mode Select Setting this bit to 1 selects the T3EX as the clock input and T3 acts in Counter mode. Setting this bit to 0 selects SYSCLK/(N+1) as the clock input and T3 acts in Timer mode.
11	T3CPRL	RW	0	T3 Capture or Timer Mode Select Set this bit to 1 configure T3 in Capture Mode. Set this bit to 0 configure T3 in Timer/Counter Mode
10	T3R	RW	0	T3 Run/Stop Control Timer 3 Run control. This bit should be set to 1 to allow the counter in T3 counting. When T3R is 0, the counter stops counting and T3R=0 does not clear the counter.

BITS	NAME	RW	DEF	DESCRIPTION
9-2	T3DIV[7-0]	RW	0x00	T3 SYSCLK Divider N SYSCLK is divided by (N+1) as T3's clock.
1	T3EXEN	RW	0	T3 External Enable. This bit enables the external signal T3EX for gating of the counting
0	T3DCEN	RW	0	T3 Up/Down Count Control. This bit needs to be set to 1 to configure T3 into UP/DOWN counter/timer mode. This bit needs to be set to 0 to configure T3 into UP counter/timer mode. It is ignored in other modes.

TIMERSTAT (Timer Interrupt Flag and Status Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-5	-	-	-	Reserved
4	EXF3	RW	0	TIMER3 External Flag EXF3 is set to 1 by hardware in capture mode when capture event occurred. It is also set to 1 by hardware in timer/counter mode when reload event occurred. Software must write 0 to clear this status bit. Software writing 1 is ignored.
3	TF3	RW	0	TIMER3 Interrupt Flag This bit is set by hardware when TIMER2_CNT is equal to TMER2_VAL. Software must write 0 to clear this status bit. Software writing 1 is ignored.
2	TF4	RW	0	TIMER4 Interrupt Flag This bit is set by hardware when TIMER2_CNT is equal to TMER2_VAL. Software must write 0 to clear this status bit. Software writing 1 is ignored.
1	TF1	RW	0	TIMER1 Interrupt Flag This bit is set by hardware when TIMER1_CNT is equal to TMER2_VAL. Software must write 0 to clear this status bit. Software writing 1 is ignored.
0	TF2	RW	0	TIMER2 Interrupt Flag This bit is set by hardware when TIMER2_CNT is equal to TMER2_VAL. Software must write 0 to clear this status bit. Software writing 1 is ignored.

2.12 Register Access Protection

Contents of some registers are critical for reliable program execution. In order to prevent accidental modification of these registers, the CPU provides register access protections for those critical registers. The access protection is partitioned into four groups using four Protection Register, TA, TB, TC, and TD. All protections are based on a time window that is opened when the particular protection register (TA, TB, TC, and TD) is written with predefined values that match with the protection key. After the protection is unlocked, the modifications of the protected registers are allowed for a predefined period of times. The unlocked state can be terminated by any writing operation to the Protection Register that contains unmatched key. The unlocked state can also be extended (the unlock time be restarted) by a new write to the Protection Register with correct Key. Under special considerations, the protection can also be turned off completely.

TA (TA Register Protection Control Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-4	TA[31-4]	WO	000000	Protection Key. When write into this location, bit[31-4] must match "A55A5AA" to open the lock. If the key is not matched, then TA will be set to locked state. If the key matches, then bit[3-1] of the write operation is also effective.
3	TAON	RW	0	This bit can be modified (cleared to 0) only if the key bit[31-4] matches. If an unmatched key is written, then TAON is automatically set to 1, and TA protection is locked. However, after reset, TA protection is unlocked.
2-1	TATIME[1-0]	WO	00	Token Time Select. The value is determined at last write. 00 – 256 Cycle 01 – 512 Cycle 10 – 1024 Cycle 11 – 2048 Cycle
0	TASTATUS	RO	0	Protection Status. When read as 1, TA is locked. Reading 0 indicate TA is unlocked.

TB (TB Register Protection Control Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-4	TB[31-4]	WO	000000	Protection Key. When write into this location, bit[31-4] must match "A55A5AA" to open the lock. If the key is not matched, then TB will be set to locked state. If the key matches, then bit[3-1] of the write operation is also effective.
3	TBON	RW	0	This bit can be modified (cleared to 0) only if the key bit[31-4] matches. If an unmatched key is written, then TBON is automatically set to 1, and TB protection is locked. However, after reset, TB protection is unlocked.
2-1	TBTIME[1-0]	WO	00	Token Time Select. The value is determined at last write. 00 – 256 Cycle 01 – 512 Cycle 10 – 1024 Cycle 11 – 2048 Cycle
0	TBSTATUS	RO	0	Protection Status. When read as 1, TB is locked. Reading 0 indicate TB is unlocked.

TC (TC Protection Control Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-4	TC[31-4]	WO	000000	Protection Key. When write into this location, bit[31-4] must match "A55A5AA" to open the lock. If the key is not matched, then TC will be set to locked state. If the key matches, then bit[3-1] of the write operation is also effective.
3	TCON	RW	0	This bit can be modified (cleared to 0) only if the key bit[31-4] matches. If an unmatched key is written, then TCON is automatically set to 1, and TC protection is locked. However, after reset, TC protection is unlocked.
2-1	TCTIME[1-0]	WO	00	Token Time Select. The value is determined at last write. 00 – 256 Cycle 01 – 512 Cycle 10 – 1024 Cycle 11 – 2048 Cycle
0	TCSTATUS	RO	1	Protection Status. When read as 1, TC is locked. Reading 0 indicate TC is unlocked.

TD (TD Protection Control Register)

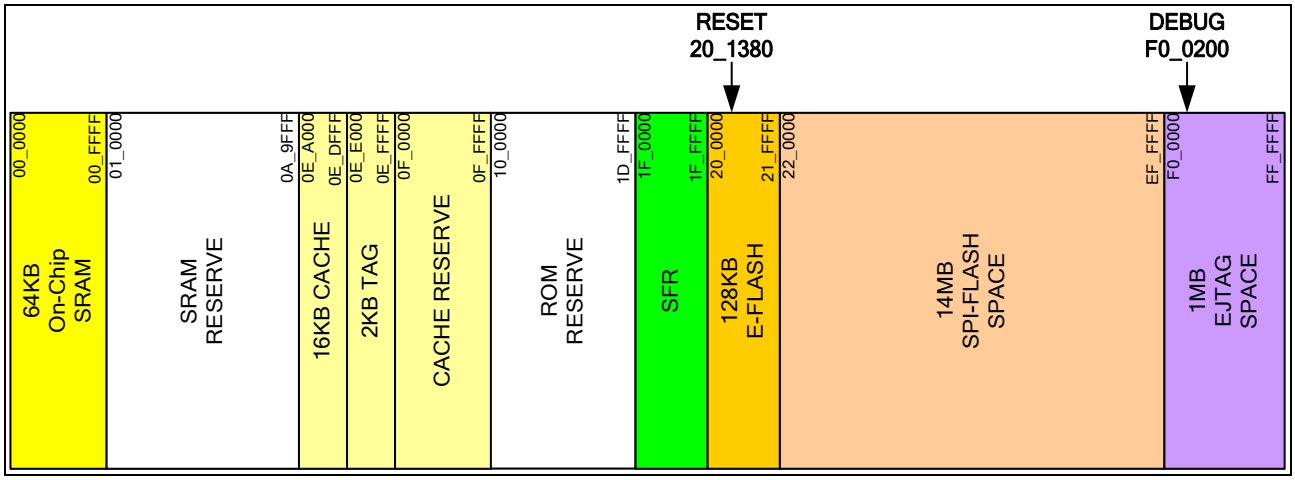
BITS	NAME	RW	DEF	DESCRIPTION
31-4	TD[31-4]	WO	000000	Protection Key. When write into this location, bit[31-4] must match "A55A5AA" to open the lock. If the key is not matched, then TD will be set to locked state. If the key matches, then bit[3-1] of the write operation is also effective.
3	TDON	RW	0	This bit can be modified (cleared to 0) only if the key bit[31-4] matches. If an unmatched key is written, then TDON is automatically set to 1, and TD protection is locked. However, after reset, TB protection is unlocked.
2-1	TDTIME[1-0]	WO	00	Token Time Select. The value is determined at last write. 00 – 256 Cycle 01 – 512 Cycle 10 – 1024 Cycle 11 – 2048 Cycle
0	TDSTATUS	RO	1	Protection Status. When read as 1, TD is locked. Reading 0 indicates TD is unlocked.

3. Memory Control

CPU accesses memory through Memory Controller which handles the memory requests for both instruction and data access. The Memory Controller manages and arbitrates access to the entire memory map of the MIPS-X processor, including on-chip SRAM, on-chip Flash, and external SPI memory.

3.1 Memory Map

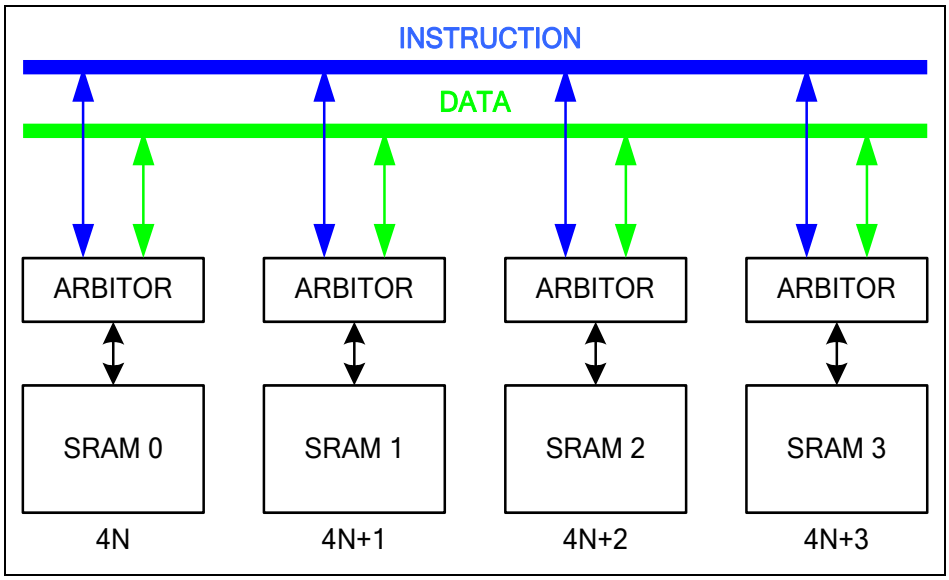
The addressing is in 24-Bit and the total addressing space is 16MB. The first 2MB space is reserved for on-chip SRAM memory that includes SRAM and cache, as well as SFR address space. The on-chip E-Flash starts at 20_0000 and extends upward. The external SPI-Flash starts after E-Flash and in CS6257, it starts at 22_0000. The SPI-Flash address is offset by 22_0000 when physical accessing the SPI-Flash. The last 1MB space is reserved for EJTAG debug interface.



The RESET starting vector is at 20_1380. This vector points to the embedded flash but avoid the beginning four pages of the embedded flash. These four pages are reserved for code security signatures and for EEPROM emulation. The security signature is stored at 20_0000 to 20_0007. The E-Flash read as all “1” after erasure and can only be written to “0”.

3.2 SRAM

On-Chip SRAM is the most valuable memory resources to CPU because of its fastest access time. It is also the most expensive to implement. MIPS-X utilizes an unique SRAM organization to maximize the performance of its on-chip SRAM. The SRAM is partitioned in an interleaving fashion as shown in the following diagram that has 4-Way Interleave.



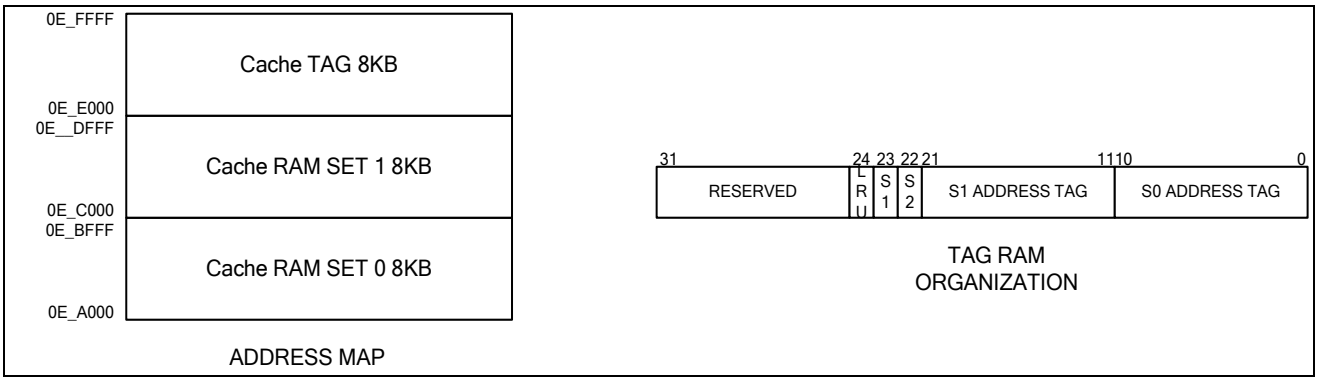
SRAM are accessed according to the LSB address. This allows simultaneous resolving both Instruction and data fetches. If a conflict occurs, the data access is stalled. As the interleaving arrangement, the conflict usually will be resolved after one-cycle because the sequential access nature of the Instruction request. In all, this SRAM arrangement greatly enhances the SRAM usable bandwidth to the CPU and overall system performance. The SRAM is used for both data storage and for critical program that needs to be executed at highest speed.

In CS6257, there is total 64KB SRAM. And it is partitioned into 4-Way interleave and each is 4K x 32.

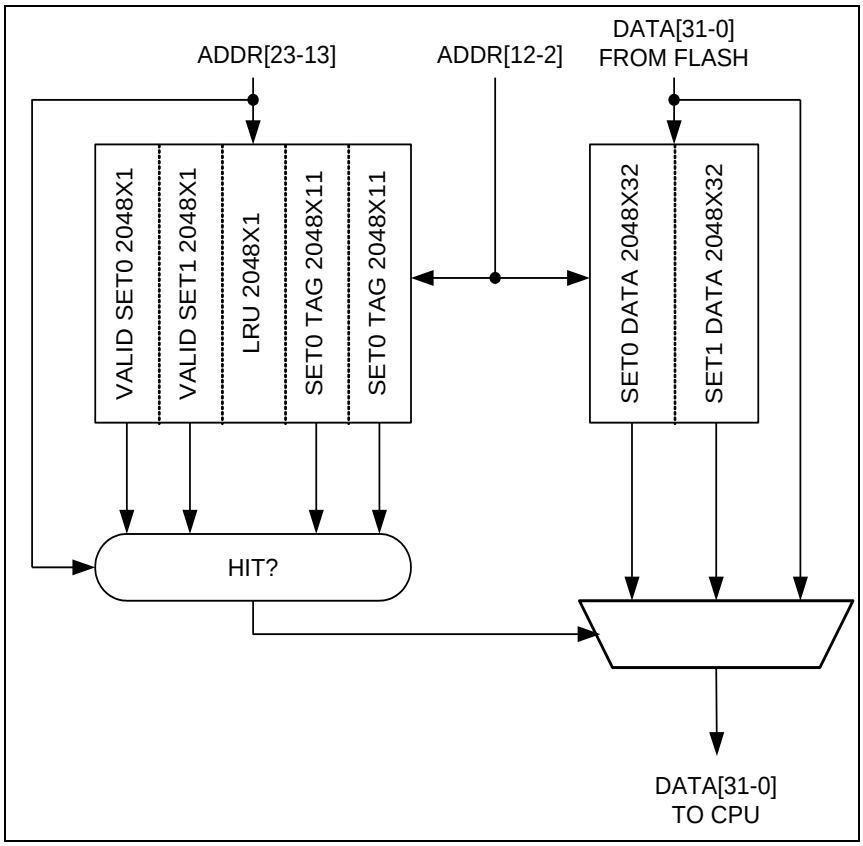
3.3 Cache Controller

The program can also be placed on the embedded Flash or on the external Flash through SPI flash interface. The access time for these program storages are slow and typically embedded flash access time is between 30nsec to 40nsec, while external flash will take even longer. To maintain the high clock rate of the CPU, the accesses to these addressing spaces are handled by a common Cache Controller. And the Cache Controller only handles READ accesses. The WRITE access to these addressing spaces is not allowed and can be done only through the SFR operations of the E-Flash Controller or SPI-FLASH Controller. In other word, there is no WRITE-THROUGH path through Cache.

The Cache Controller implemented 2-Way Set-Associative Cache and is organized as 2Kx 64 (16KB) Cache RAM with Tag RAM of 2048x32 (8KB) (only the LSB 25 bits are meaningful for TAG). The Cache Controller support byte, word and double word access. The filling of the Cache is always in double word entry a time. The Cache RAM and Tag RAM are also mapped to memory space too so program can have direct access to these for implementation of cache flush and testing purpose. If Cache operation is not necessary, the 16KB Cache RAM and 8KB Tag RAM can be configured as regular SRAM. This can increase the SRAM capacity by 24KB if SRAM requirement is more and E-Flash or SPI-Flash speed can be sacrificed. When they are used as regular SRAM, these SRAM can only be used as DATA memory by the CPU, and can be accessed in DW format only (issuing a byte or single word access may result unexpected overwriting effects). The address map and organization or the Cache and Tag RAM are shown in the following.



Note that the address indicated in the map is byte address. The access should be done only in double-word 32-bit format. Although the access to the TAG and Cache can be used for flush purpose, there is also hardware flush command available in the Cache Controller control register. It is recommended to use the hardware flush control. The operation of the Cache Controller is shown in the following diagram showing the access path and selections.



Although Cache can increase the access speed significantly especially for instruction access as its sequential nature, for some certain data structure the cache may actually impact the performance because it may cause MISS condition and interferes with other access. Therefore the E-Flash and SPI-Flash memory space is divided into 2M banks that allow individual control of cacheable or non-cacheable. The E-JTAG memory space is always non-cached. The cache setting can be changed at any time. However, the contents of the Cache RAM and TAG will remain unaffected. Further access will cause the Cache to be updated. For practical operation, it is recommended that the Cache is always flushed after the change of the Cache setting to avoid any inconsistency.

CACHECFG (Cache Configuration) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-24	-	-	-	Reserved
24	BCEN7	-	0	Bank 7 (E0_0000 – FF_FFFF) is always not cacheable
23	BCEN6	RW	0	Enable Bank 6 (C0_0000 – DF_FFFF) Cache.
22	BCEN5	RW	0	Enable Bank 5 (A0_0000 – BF_FFFF) Cache.
21	BCEN3	RW	0	Enable Bank 3 (80_0000 – 9F_FFFF) Cache.
20	BCEN2	RW	0	Enable Bank 2 (60_0000 – 7F_FFFF) Cache.
19	BCEN1	RW	0	Enable Bank 1 (40_0000 – 5F_FFFF) Cache.
18	BCEN0	RW	0	Enable Bank 0 (20_0000 – 3F_FFFF) Cache.
17	-	-	-	Reserved
16	CACHEEN	RW	-	Global Cache Enable. Set 1 to enable Cache Controller.
15-9	-	RW	0	Reserved
8	CACHEMEM	RW	0	Memory Map Enable. When this bit is set, the cache operation is disabled regardless of other setting. The 16KB Cache RAM and 2KB TAG RAM functions as regular SRAM space.
7-1	-	-	-	Reserved
0	FLUSH	WO	0	Hardware Cache Flush. Set to 1 to initiate hardware flush. It is cleared to 0 when the flush operation is completed. Only write 1 has meaning.

The Cache hit rate has a great impact on CPU execution efficiency. The Cache Controller has built-in profiling mechanism that can be used to analyze the Cache performance and find critical code bottleneck. The profiling mechanism gathers statistics for 4 sets of address ranges. These ranges can be exclusive, overlapping, or nested without constraint. Each set of profile consists of two address registers, Starting Address register, and Ending Address register, and two counters, Total Cache Hit counter, and Total Cache Miss and Write Through counter. These profile mechanisms are configured and accessed through indirect ways by manipulating CPFCMD and CPFDATA registers and are described in the following. The access sequence is by setting correct control in CPFCMD register first, then perform read or write operation on CPFDATA register for the desired results.

CPFCMD (Cache Profile Command Register) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-11	-	-	-	Reserved
10	WR	RW	0	Control the read or write access to the indirect access. 1 is for write and 0 is for read
9-8	SETADD	RW	0	Control the indirect access location. 00 – Access Profile Set 0 01 – Access Profile Set 1 10 – Access Profile Set 2 11 – Access Profile Set 3
7-3	-	-	-	Reserved
2-0	REGSEL	RW	0	Select which indirect registers of the specified profile set. 000 – Select the Starting Address register of the profile set. 010 – Select to control the profile counter. Under this selection, CPFDATA[0] is used to enable or disable the counter (1 = enable, 0 = disable). CPFDATA[1] is used to force clear the counter (1 = clear, 0 = continue count). Note under disable state, the counter value is maintained. 001 – Select the Ending Address register of the profile set.

BITS	NAME	RW	DEF	DESCRIPTION
				011 – Select the HIT counter fore operation.
				010 – Select the MISS+WRITETHROUGH counter for operations.
				Other settings are invalid.

CPFDATA (Cache Profile DATA Register) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-0	CPFDATA [31-0]	RW	0X000 00000	Profile Register Data

This register is used for multi-purpose. It contains the 32-bit content for Starting Address and Ending Address when performing a write command. It contains the cache MISS or HIT count value when performing a read command. When controlling the counter, it serves as disable/enable, and clear control of the two counters.

IPFCOUNT (Instruction Execution Counter) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-0	IPFCOUNT [31-0]	RW	0X000 00000	Instruction Execution Count

This register records the total number of executed instructions by CPU. It is zero after reset, and can be set to arbitrary number and start the count from that number. It can be used to dynamically profile the code complexity.

3.4 E-Flash Controller

The on-chip embedded flash memory is connected to MIPS-X through Cache Controller for Instruction and Data Access. This access is limited to reading out the flash content. To write or erase the flash memory, the CPU must operate on the E-Flash Controller.

3.4.1 E-Flash Memory

There are many variations in the size, configurations of the on-chip embedded flash memory. CS6257 has an on-chip embedded Flash of 128KB main memory (64Kx16) and a 256B (128x16) Information Block (IFB). The IFB is mainly used by manufacturer to store manufacturing information and calibration data and should not be altered by the user program.

The main memory block of the embedded flash is partitioned in uniform 1K Byte sectors. The sector can be erased or programmed separately. To write into the Flash or use as data storage, it must go through operations of the Flash Controller. The Flash is different from the EEPROM (byte erasable), the erase of the data in flash are segment based. This must be taken into consideration when use the Flash as data storage. After erasure, the content of the Flash is “1”. The content can only be written from “1” to “0”. After written to “0”, the flash can not be restored to “1” unless the whole segment is erased.

3.4.2 E-Flash Controller

Flash Controller is under program control through its SFR registers. The command issued to Flash Controller is in EFLHCMD register, while the address directed to the Flash memory is kept in EFLH_ADRR registers. The data operand of the command is kept in EFLHDATA register. Most of the accesses to the Flash Controller registers are protected by TB in order to prevent accidentally overwriting of the contents. There are also extensive protections that can be configured to maximize the reliability of the Flash contents. These include setting a range of protections for content protection, and also include code security range. These details are described by the registers of Flash Controller. Another critical aspect is the operation on the embedded Flash takes time especially commands like erase or write which takes approximately about 100usec and 200msec respectively. When the command execution is started, the Flash Controller will stall CPU until the command is completed if CPU initiate subsequent access request to Flash memory. Since these timing are critical for reliable Flash operations and these timing are

absolute, it does not scale with the CPU clock rate. The Flash Control clock needs to be scaled to around 4MHz. Also the embedded Flash is 16-bit wide, so all operations and command are double-byte based through the E-Flash Controller.

When Flash Controller is in execution of command, it will take full control of E-Flash, but it does not always stall the CPU executions if CPU access does not require E-Flash access. If CPU accesses the memory space of the E-Flash through the memory control path while Flash Controller is busy, it will stall the CPU access. Also, if E-Flash Controller is busy, any new command issued will be ignored

EFLHCMD (E-Flash Controller Command Register) TA

BITS	NAME	RW	DEF	DESCRIPTION
31	FCRESET	RW	0	Set this bit to 1 will reset the E-Flash controller. This bit is self-cleared.
30-27	WAIT[3-0]	RW	1111	Wait State Setting. This set the wait state of the embedded flash read access path. This applies for both CPU access and SFR access. The wait state setting should ensure the Flash read access time to be larger than 40nsec. The access time is equal to (WAIT[3-0+1]*1/SYSCLK.
26-24	-	-	-	Reserved
23-16	FCCKS[7-0]	RW	FF	Flash Controller Clock Scaler. This divides the SYSCLK to generate a reference clock for Flash Controller for program and erase timing. FCCKS[7-0] should be set to generate a approximately 4MHz clock.
15	EFCINTEN	RW	0	E-Flash Controller Interrupt Enable. When this bit is set to 1, it enables the interrupt of the E-Flash Controller. An interrupt is generated when either a flash command execution failed or execution time out.
14	FAILF	RW	0	Fail Flag This bit is set to 1 when a command execution failed. This bit must be cleared to 0 by software writing 0.
13	TOUTF	RW	0	Time Out Flag This bit is set to 1 when Time out happens. This bit must be cleared to 0 by software writing 0.
12	-	-	-	Reserved
11	TIMEOUT	RO	0	Time Out Status This bit is set by hardware. This is cleared when a new command is issued.
10	BUSY	RO	0	This bit indicates the status of the Flash Controller. It is set to 1 when the controller is operating on the flash. No new command should be issued if BUSY bit is set.
9	FAIL	RO	0	This bit indicate the result of the previous command
8	WORD	RW	1	If this bit is set to 1, it indicated a WORD command (16-bit). If it is 0, it is DWORD command (32-bit). This only affect READ and WRITE commands. For WORD command, the lower LSB bit of ADDR is ignored. For DWORD command, the two lower LSB bits of ADDR is ignored.
7	CMDEN	RW	0	If this bit is 0, then only BIT[5-0] are written. If this bit is 1, then all bits in this register are written.
6	TOEN	RW	0	Time Out Enable Set this bit to 1 to enable Time Out counter for Flash program and erase time out. The Time Out duration for program is 50*FCCKS[7-0]*1/SYSCLK (40usec). The Time Out duration for erase is 8180*FCCKS[7-0]*1/SYSCLK (20msec).
5	-	-	-	Reserved
4	MMSER	RW	0	Set this bit to initiate MM Sector Erase. This command is protected by

BITS	NAME	RW	DEF	DESCRIPTION
				the address range set by protection zone.
3	IFBWR	RW	0	Set this bit to initiate IFB Write. This command is only possible for address (80-FF in byte address).
2	MMWR	RW	0	Set this bit to initiate MM Write. This command is protected by the address range set by protection zone.
1	IFBRD	RW	0	Set this bit to initiate IFB Read
0	MMRD	RW	0	Set this bit to initiate MM Read

*** If multiple command bits (bit 4-0) are set, the command is not executed and returned with failed status.

For all commands, the address of the flash is composed from FLSH_ADDR, and the data is referred at FLSHDAT registers. For erase commands, the sector address is determined by upper address bits. Please note the sector organization of the main memory is not uniform. And the erase command will erase the whole addressed sector contents. For Erase and Write command, the Flash Controller will also check if the destination address falls within the protection zone defined by CNTPCTL and CNTPCTH registers. If it is protected, the Flash Controller will not execute the command and return with FAIL result bit. For IFB Byte write, the Flash Controller will not execute the command and return with Fail result bit if the byte address falls into manufacturer data range. The IFB can note

EFLHADDR (E-Flash Controller Address Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-17	-	-	-	Reserved
16-0	ADDR[16-0]	RW	0x00	Flash Address

This defines the address of the command. This is reference to the Flash macro and starts with 0x00000. Therefore only the lower 17 bits are meaningful for addressing the on-chip 128KB E-Flash. Because the Flash is organized as 64Kx16, the LSB is ignored. For DWORD operation, the lower 2 bits must be 0.

EFLHDATA (E-Flash Controller Data Buffer Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-0	DATA[31-0]	RW	0x00	Flash Data

This acts as the data buffer for the E-Flash Controller. All operations are based on 16-bit format to suit for the E-Flash organization. Only the lower 16 bits are used, DATA[31-16] are ignored.

A common problem of embedded flash memory used for both data and program storage is the content loss from improper software or accidental modification caused by program flow or noise induced random executions. The implementations of Flash Controller take into considerations of these events and provide protections to avoid accidental erasure or modifications of critical information or software code. When Flash Controller is issued with a command through FLSHCMD register, it checks whether the destination of the command falls in the content protection zones. If it falls within the protection zones, the flash control aborts its operations and returns with command failure status. The protection is zoned in 64KB zones. In each 64KB zone, two pointers are set. The upper pointer set the protection from 0xFFFF to UPPOINT, and lower pointer set the protection from 0x0000 to LWPOINT. In defaults, UPPOINT is 0xFFFF, and LWPOINT is 0x0000, therefore no protection is in effect. If UPPOINT and LWPOINT overlap, then the whole 64KB zone is protected. CS6257 contains a 128KB embedded Flash, therefore it has two zones of protection setting.

EFLHPCT1 (E-Flash Protection Zone for 1st 64KB) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-16	UPPOINT	RW	0xFF	Set to protect 0xFFFF to UPPOINT flash content
15-0	LWPOINT	RW	0x00	Set to protect 0x0000 to LWPOINT flash content

EFLHPCT2 (E-Flash Protection Zone for 2nd 64KB) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-16	UPPOINT	RW	0xFF	Set to protect 0xFFFF to UPPOINT flash content
15-0	LWPOINT	RW	0x00	Set to protect 0x0000 to LWPOINT flash content

3.5 SPI Flash Controller

The SPI Flash Controller allows the CPU to access external SPI flash memory for its data and instruction access. The CPU memory access for both instruction and data are through cache controller. These accesses are limited for read access of the SPI flash and are always in 4-byte burst mode.

The controller acts as a SPI master seen by the SPI flash memory. The master can be configured as either Mode 0 or Mode 3. The difference of these two modes is the clock polarity when the master is in stand-by state. The clock remains at 0 for Mode 0, and remains 1 for Mode 3 during stand-by state. In either case, SPI flash slave will use the rising edge of the clock to sample the data input, and use the falling edge to output the data. For high clock rate operation, the master can be configured to use different edges to sample the data from the slave. The instruction and data read access is through cache. The CPU can also operate on the registers of SPI Flash Controller to issue commands to the external SPI flash and accomplish read and write operations. CS6257 acts as a master device and SPI flash acts as a slave, and CS6257 only supports single external SPI flash. The external interface required include SFCK (Clock), SFDI, SFDO, and SFCS.

SFCCFG (SPI Flash Controller Configuration Register) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-16	-	-	-	Reserved
15	SFCINTEN	RW	0	SPI Flash Controller Interrupt Enable When this bit is set to 1, it enables the interrupt of the SPI-Flash Controller. An interrupt is generated when either a command fail execution has occurred or a CPU access to SPI-Flash space during stall timer is active.
14-11	-	-	-	Reserved
10-8	FSIZE	RW	111	External SPI Flash Size 000 – 1M Bits (128KB) 001 – 2M Bits (256KB) 010 – 4M Bits (512KB) 011 – 8M Bits (1MB) 100 – 16M Bits (2MB) 101 – 32M Bits (4MB) 110 – 64M Bits (8MB) 111 – 128M Bits (16MB)
7	SPI Mode	RW	0	SPI Flash Mode 0 – Mode 0 1 – Mode 3
5-4	REFEDGE	RW	00	MISO (Master Input Slave Output) Clock Edge Reference 00 – Data is referenced at current positive edge and sampled at falling edge 01 – Data is referenced at current negative edge and sampled at next rising edge 10 – Data is referenced at next positive edge and sampled at following negative edge 11 – Data is referenced at next negative edge and sampled at following positive edge
3-0	SPICKS	RW	1111	SPI Clock Setting

BITS	NAME	RW	DEF	DESCRIPTION
				SPI Clock = SYSCLK/(SPICKS+1)

SFCCMD (SPI Flash Command Register) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-16	-	-	-	Reserved
15	SHIFTDIR	RW	0	SDO and SDI (defined as Master) shift direction 0 – SDO active shift out during data byte transfer 1 – SDI active shift in during data byte transfer
14-11	DBYTEC	RW	0000	Number of data byte to be transferred in SFCARG1 and SRCARG2 For transmit command, the contents in SFCARG1 and SRCARG2 are used. DBYTE 0 is transmitted first. For receive command, the DBYTE0 location stored the first received byte. If DBYTEC is 0, the data byte transfer is skipped.
9-8	ABYTEC	RW	000	Number of bytes transmitted in SFCARG0 000 – Skip SFCARG0 001 – 100: Number of bytes to transmit in SFCARG0
7-0	CMD[7-0]	RW	0	Command Byte This contains the SPI Flash command value

The CPU needs to be stalled in two conditions if it is trying to access the memory space residing in SPI-Flash. First, the SPI-Flash controller is busy transferring the command. Second, the SPI-Flash itself is occupied in performing write or erase command. This timer enables a stall duration CPU access to SPI Flash. The timer is cleared when an SFC_CMD is issued. And the timer is expired when it reaches STIMER[30-0] value. During the timer active duration, all CPU data and instruction accesses to SPI Flash will be stalled. The CPU is stalled when CPU try to access SPI flash content during an SFR SPI Flash command is being transferred. Normally, if the command is a read data or read status SPI flash command, the command sequence is terminated once the command and its associated address and data are transferred. Then the CPU stall is released. However, for SPI flash write or erase command, the data access of SPI flash can not occur at the same time, and the content returned will be invalid. Therefore, the stall timer should be turned on when issuing these commands (ERASE, WRITE) and stalls the CPU access to the SPI-Flash space while SPI-Flash is busy.

SFCSTALLT (SPI Flash Controller CPU Stall Time Out Setting) TA

BITS	NAME	RW	DEF	DESCRIPTION
31	STIMEREN	RW	1	Set this bit to enable Stall Timer
30-0	STIMER[30-0]	RW	3FFF	This set the Time Out duration. Time Out duration = TO[30-0] * 1/SPI_CLK

SFCSTAT (SPI Flash STATUS Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-4	-	-	-	Reserved.
3	STALLF	RW	0	Stall Access Flag This bit is set when CPU tries to access SPI-Flash memory space during stall timer active duration. This bit must be cleared by software by writing 0.
2	FAILF	RW	0	Fail Flag This is set when a command execution failed. This must be cleared by software by writing 0.
1	FAIL	RO	0	Command Execution Result This bit is set to 1 if the previous command of SPI Flash controller failed, for example, if a new command is issued before the previous command is under transfer, then the new command will not be executed and this bit is set to 1. This bit is cleared by hardware when a command was executed successfully.
0	BUSY	RO	0	This bit is set to 1 when the previous command is still in progress communicating with the external SPI Flash. Note this bit does not reflect the state of the internal SPI Flash such as write or erase. This bit only indicates the operation state of the on-chip SPI Flash controller.

SFCARG0 (SPI Flash Command Argument 0)

BITS	NAME	RW	DEF	DESCRIPTION
31-24	ABYTE3	RW	0	Dummy Byte 0 or ADDR[23-16]
23-17	ABYTE2	RW	0	Dummy Byte 1 or ADDR[15-8]
16-8	ABYTE1	RW	0	Dummy Byte 2 or ADDR[7-0]
7-0	ABYTE0	RO	0	Dummy Byte 3

SFCARG1 (SPI Flash Command Argument 1)

BITS	NAME	RW	DEF	DESCRIPTION
31-24	DBYTE0	RW	0	DATA Byte 0
23-17	DBYTE1	RW	0	DATA Byte 1
16-8	DBYTE2	RW	0	DATA Byte 2
7-0	DBYTE3	RO	0	DATA Byte 3

SFCARG2 (SPI Flash Command Argument)

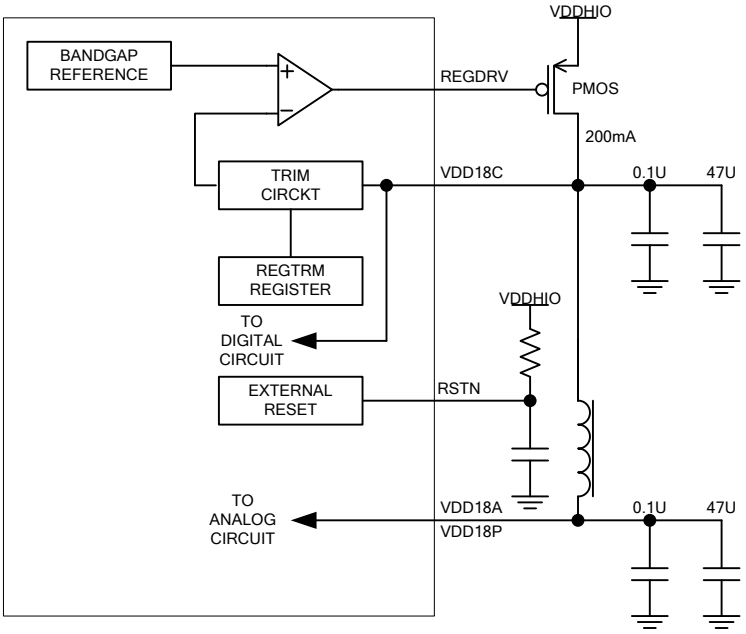
BITS	NAME	RW	DEF	DESCRIPTION
31-24	DBYTE4	RW	0	DATA BYTE 4
23-17	DBYTE5	RW	0	DATA BYTE 5
16-8	DBYTE6	RW	0	DATA BYTE 6
7-0	DBYTE7	RO	0	DATA BYTE 7

4. Essential Analog Peripheral

This chapter describes the functions of essential analog macros.

4.1 1.8V Regulator

The core logic and embedded Flash is supplied by the 1.8V output from the on-chip regulator that regulates VDD (3.0V to 5.5V). The regulator structure uses an external PNP or PMOS transistor for serial regulation to minimize the heat consumption on the chip in order to allow higher temperature tolerance. The connection of the on-chip regulator is shown in the following block diagram.



There is variation of this 1.8V due to chip to chip difference. Because this 1.8V is also used to generate the reference for other analog peripherals such as ADC, the relative accuracy of this supply voltage is important. The on-chip 1.8V regulator thus has trimming options to fine tune the output level. The trimming is done by register REGTRM. The power on default will set the regulator at its highest level. The trimming range is between 1.6V to 2.0V. The calibrated value of REGTRM for trimming to 1.8V is stored by manufacturer in IFB.

REGTRM (Regulator Trimming Register) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-8	-	-	-	Reserved
7-0	REGTRM [7-0]	RW	0xFF	Regulator Trimming Register. The default after reset will allow the maximum output level of the 1.8V regulator

4.2 System Clock Sources

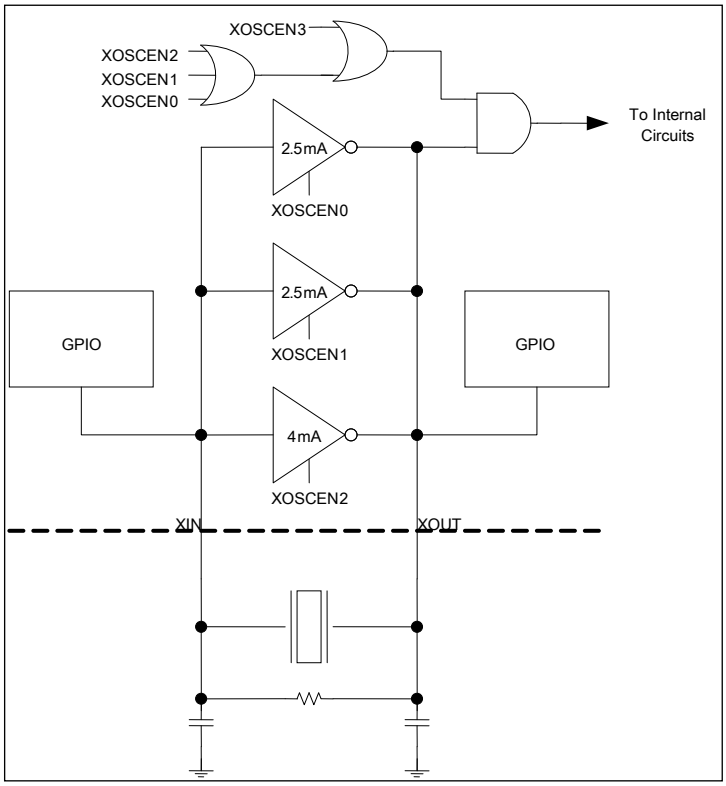
There are two possible clock sources – XOSC, and PLL. After reset, XOSC is always selected, and PLL is disabled and powered down. Typically, CS6257 requires a crystal oscillator ranging from 6MHz to 20MHz. And the crystal oscillator requires about 50msec to 100msec to becoming stable. So the reset time should be longer than this stable time. To switch into a new clock source, the software must first enable the target clock source and allow enough time for the clock source to stabilize before switch the selection

OSCCFG (IOSC Configuration Register) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-26	-	-	-	Reserved
25-24	CLKSEL[1-0]	RW	00	00 – XOSC 01 – XOSC 10 – XOSC 10 – PLL
23-20	-	-	-	Reserved
19	XOSCEN3	RO	0	Enable external clock source. (Not used)
18	XOSCEN2	RO	0	Enable 2.5mA XOSC driver. Hardwired to 0. (Not used)
17	XOSCEN1	RO	1	Enable 2.5mA XOSC driver. Hardwired to 1.
16	XOSCEN0	RO	1	Enable 2.5mA XOSC driver. Hardwired to 1.
15-10	-	-	-	Reserved
9-8	ITRIM[1-0]	RW	0x00	IOSC coarse trim setting (Not Used)
7-0	VTRIM[7-0]	RW	0x00	IOSC fine trim setting (Note Used)

4.2.1 Crystal Oscillator

The on-chip crystal oscillator is a configurable CMOS inverter. The block diagram is shown in the following.



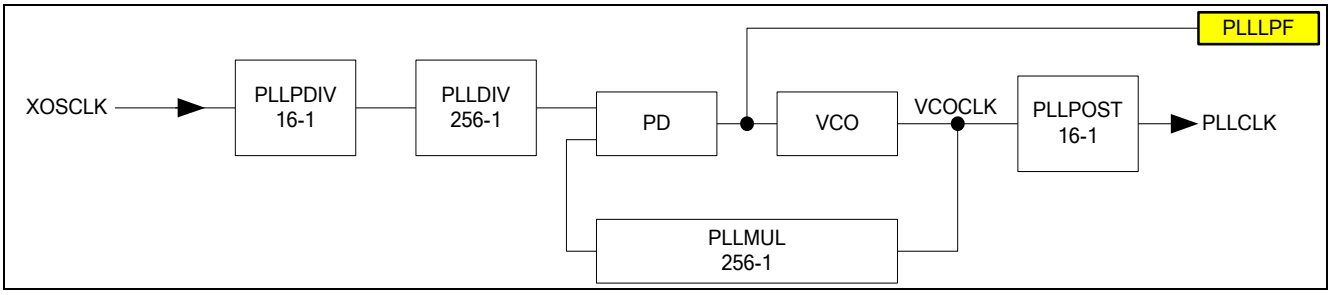
The configuration allows the adjustment of the driving strength of the inverter to suit different crystals. Typical setting is shown in the following. In CS6257, XOSCEN0 and XOSCEN1 are hardwired to 1, and XOSCEN3 and XOSCEN2 are hardwired 0.

XOSCEN3	XOSCEN2	XOSCEN1	XOSCEN0	OSC Operations
0	0	0	0	Powered down.
X	0	0	1	Low power for 3V up to 8MHz, 5V up to 12MHz.
X	0	1	1	Medium power for 3V up to 16MHz, 5V up to 24MHz.
X	1	1	1	High power for 3V up to 25MHz, 5V up to 30MHz.
1	0	0	0	External source applied at XOUT

The XOSC stabilization time strongly depends on the oscillation frequency and the quality of the crystal used. When using external clock source, it should be applied through XIN pin, and also the duty cycle should be between 40% and 60%.

4.2.2 Phase Lock Loop

An on-chip Phase-Lock Loop can also be used to provide clock source for the CPU and peripherals. The PLL uses VDD18P as the power supply and requires an external capacitor for loop filter. The reference clock source is from XOSC. The PLL consumes about 5mA from VDD18P and requires about 100msec to becoming stable after enable. The VCO has finite range between 100MHz to 200MHz. Therefore the software must ensure the setting so VCOCLK falls into this valid range. The resultant frequency of PLL clock is XOSCLK*PLLMUL/PLLPDIV/PLLDIV/PLLPOST.

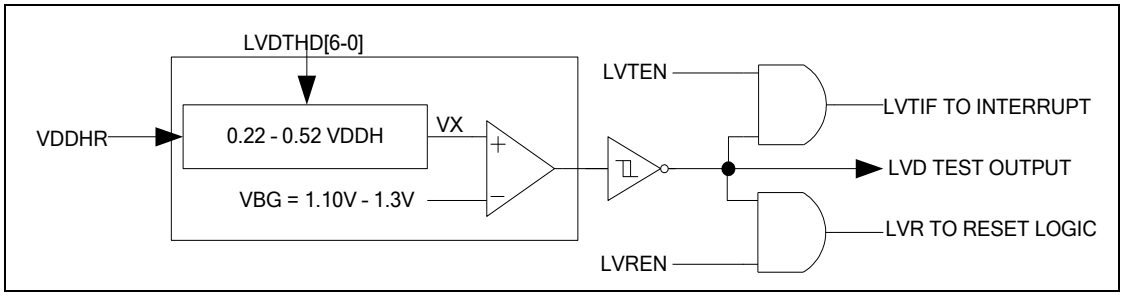


PLLCFG (PLL Configuration Register) TA

BITS	NAME	RW	DEF	DESCRIPTION
31	PLLEN	RW	1	Set 1 to enable PLL
30-25	-	-	-	Reserved
24	PLLSEL	RO	1	PLL Reference Select. 0 selects IOSC, 1 selects XOSC. Hardwired to 1.
23-20	PLLPDIV	RW	0x00	PLL pre divider for reference clock
19-16	PLLPOST	RW	0x00	PLL post divider
15-8	PLLMUL	RW	0x00	PLL Multiplicator
7-0	PLLDIV	RW	0x00	PLL Divider

4.3 Low Voltage Detect

The low voltage detect circuit detects the condition of VDDH supply. The supply rating of VDDH is 3.0V to 5.5V. When enabled, it detect VDDH < VTH condition, and can be configured to generate an interrupt or a system reset. Because the existence of on-chip regulator the system and user program should have ample time to responds to the interrupt. The larger the decoupling capacitance on VDD18, the longer this time can be extended. To ensure a reliable MCU operation and prevent loss of data, user program should terminate all critical process and wait for power supply to get back to normal or as power supply continue to deteriorate and finally reset the system. The block diagram of Low Voltage Detection Circuit is shown in the following figure.



The circuits detect a percentage of the VDDH and compare it against the internal band-gap reference voltage. The default state of the LVD circuit is disabled. The user program needs to enable the preferred configuration and set the appropriate detection threshold level. When enabled, the LVD circuit needs about 10usec to get initialized. The following register is used for this purpose. The LVD circuits consumes about 250uA (under VDDH=3.3V) up to 500uA (under VDD=5.0V) when enabled.

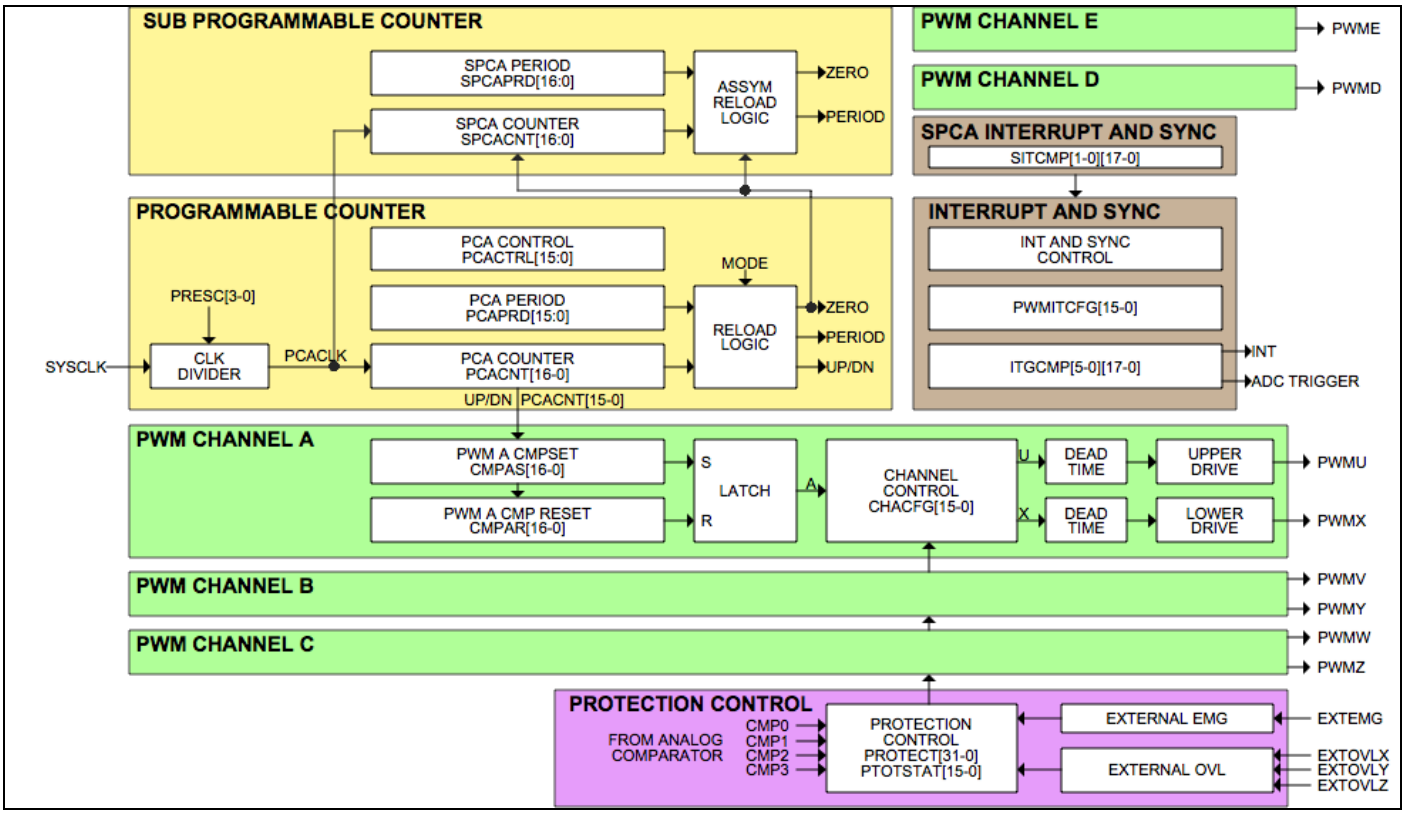
LVDCFG (Low Voltage Detect Configuration Register) TA

BITS	NAME	RW	DEF	DESCRIPTION
31-18	-	-	-	Reserved
17	LVTEN	RW	0	Set to enable low voltage interrupt. This will cause a interrupt when low voltage condition occurs.
16	LVREN	RW	0	Set to enable low voltage reset. This will cause hardware reset when low voltage condition occurs.
15	LVDEN	RW	0	Set to turn on supply voltage detection circuits.
14-8	LVDTHD[6-0]	RW	0x00	Set the LV detection threshold
7-1	-	-	-	Reserved
0	LVTIF	RW	0x00	Low voltage detection interrupt flag. Set when LVD detection occurs and must be cleared by software.

LVDTHD = 7F will set the detection threshold at its maximum (approximately 5.0V), and LVDTHD = 00 will set the detection threshold at its minimum (approximately 2.5V). LVDTHD[6-0] set the compare threshold from 0.22VDDH to 0.52VDDH against the internal reference voltage of 1.25V in uniform steps. Therefore the detection range is from 2.5V to 5.0V assuming the reference voltage is 1.25V.

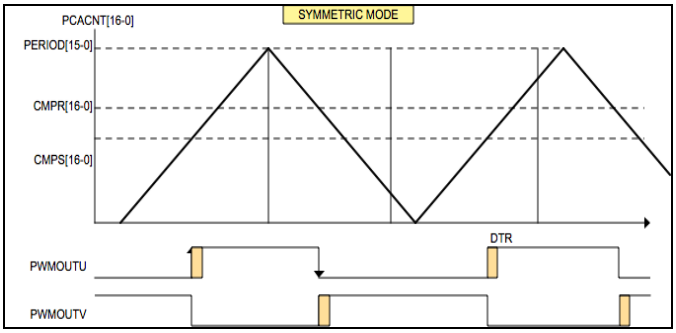
5. Motor Controller

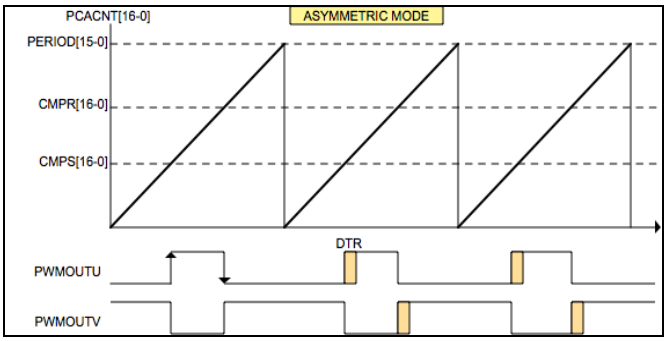
The motor controller is a specialized PWM waveform generation circuits with features dedicated for AC motor control. The central timing is generated by a Programmable Counter Array (PCA) and there are three PWM channels. PCA also supplies timing control for synchronization with ADC and interrupt logic to communicate with the CPU. There is a protection logic that is tightly coupled with each of the PWM channels to handle emergency and abnormal condition for motor applications. The block diagram of the Motor Controller is shown in the following diagram.



5.1 MPCA

The MPCA are used to generate a central PWM timing reference for motor control. It consists of a 16-Bit Counter and a period register for generating a periodic waveform. There are two modes of operation for the MPCA – symmetric or asymmetric. In symmetric mode, the MPCA counter increment from 0 until reach the period setting then starts decrementing to 0, and the resulting counting waveform is a triangular shape. In asymmetric mode, the counter starts with 0 and increments until reaching the period setting, and then restarts counting from 0, and the resulting counting waveform is a saw tooth shape.





The MPCA clock is derived from SYSCLK, and can be scaled down by a clock pre-scaler. The PCA can be enabled or disabled. Many of the registers in PCA/PWM module are in double-buffered configurations. This is to prevent PWM output glitches when updating these registers.

PCACFG (PCA Configuration Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-24	-	-	-	Reserved
23	ENCTRL	W	0	PCA Enable Write Control. This bit is used to allow easier control of PCA, and is write-only. When writing to PCA_CFG, if this bit is also 1, then the whole register is updated. If this bit is 0, then only PCAEN, bit 16 is affected. This bit is not a registered bit.
22-17	-	-	-	Reserved
16	PCAEN	RW	0	PCA Enable. Set to 1 for enable PCA/PWM module.
15	SRINIT	RW	0	Set the initial value of the S/R latch in the PWM channel. If SRINIT=0, then the channel S/R latch has 0 as its initial value when PWM is enabled. It is initialized as 1 if SRINIT=1.
14-12	EMGOVLSC[2-0]	RW	00	EMG and OVL pulse filter clock setting. This is used to scale down the pulse filter clock for the EMG and OVL logic. The pulse filter clock EMGOVLCLK is SYSCLK/(EMGOVLSC[2-0] +1). And unit time is 1/EMGOVLCLK.
11-8	DTPSC[3-0]	RW	0000	Dead Time Clock Prescaler. This is used to scale down the dead time logic clock. The Dead Time Clock (DTCLK) is SYSCLK/(DTPSC[3-0]+1). The unit dead time DTPRD is 1/DTCLK.
7	-	-	-	Reserved
6-5	DBUPD	RW	00	Define the Double Buffer Registers update timing. 00 – Immediate. 01 – Update occurs when PCACNT = 0 10 – Update occurs when PCACNT = PCAPRD 11 – Update occurs when PCACNT = 0 or PCAPRD whichever is earlier.
4	SMODE	RW	1	Symmetric Mode. Set to enable Symmetric Mode. Default is Asymmetric Mode.
3-0	PRESC[3-0]	RW	0000	PCA Clock Prescaler. PCACLK is SYSCLK/(PRESC[3-0]+1).

Note when PCA is disabled, the PCACNT is cleared to 0. At enabling, the PCACNT starts the count from 0.

PCACNT (PCA Counter Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-24	CNTCLR	WO	0	Write these bits with 0x55 will force the Counter to be cleared to 0x0000 with DIR = 0. The clear action is always immediate.
23-17	-	-	-	Reserved
16	DIR	RO	0	Count Direction. This bit is 0 when counting upward (incrementing) and 1 when counting downward (decrementing).
15-0	COUNT	RO	0x0000	PCA Counting Value. When read, the value of current count is read out.

PCAPRD (PCA Period Register) DB

BITS	NAME	RW	DEF	DESCRIPTION
31-16	-	-	-	Reserved
15-0	PERIOD [15-0]	RW	0x0000	PCA Count Period. This defines the PCA period. The counter is restart from 0 in asymmetric mode, or changes direction when the counter value is equal to the period value.

This register is double buffered. The update instant is defined by DBUPD[1-0] in PCA_CFG register. The number of cycles in symmetric mode is 2*(PERIOD[15-0]+1).

5.2 PWM Channels

There are three PWM channels named A, B and C and the status of the channel is from a S/R Latch. Each channel has two compare registers, one for setting the Latch output to 1, and one for resetting the Latch output to 0. These registers are all double buffered and the update instant is defined by DBUPD in PCACFG register.

CMPAS (PWM Channel A Compare Set Register) DB

BITS	NAME	RW	DEF	DESCRIPTION
31-17	-	-	-	Reserved
16	DIR	RW	0	Direction Bit. This is used to compare with the direction bit of the PCA counter. It is ignored under Asymmetric mode.
15-0	COMPSET	RW	0x0000	Compare Value for R/S Latch Set. When PCA count equals to this value, the output of channel S/R Latch is set to 1.

CMPAR (PWM Channel A Compare Reset Register) DB

BITS	NAME	RW	DEF	DESCRIPTION
31-17	-	-	-	Reserved
16	DIR	RW	0	Direction Bit. This is used to compare with the direction bit of the PCA counter. It is ignored under Asymmetric mode.
15-0	COMPSET	RW	0x0000	Compare Value for R/S Latch Reset. When PCA count equals to this value, the output of channel S/R Latch is reset to 0.

CMPBS (PWM Channel A Compare Set Register) DB

BITS	NAME	RW	DEF	DESCRIPTION
31-17	-	-	-	Reserved
16	DIR	RW	0	Direction Bit. This is used to compare with the direction bit of the PCA counter. It is ignored under Asymmetric mode.
15-0	COMPSET	RW	0x0000	Compare Value for R/S Latch Set. When PCA count equals to this value, the output of channel S/R Latch is set to 1.

CMPBR (PWM Channel A Compare Reset Register) DB

BITS	NAME	RW	DEF	DESCRIPTION
31-17	-	-	-	Reserved
16	DIR	RW	0	Direction Bit. This is used to compare with the direction bit of the PCA counter. It is ignored under Asymmetric mode.
15-0	COMPSET	RW	0x0000	Compare Value for R/S Latch Reset. When PCA count equals to this value, the output of channel S/R Latch is reset to 0.

CMPCS (PWM Channel A Compare Set Register) DB

BITS	NAME	RW	DEF	DESCRIPTION
31-17	-	-	-	Reserved
16	DIR	RW	0	Direction Bit. This is used to compare with the direction bit of the PCA counter. It is ignored under Asymmetric mode.
15-0	COMPSET	RW	0x0000	Compare Value for R/S Latch Set. When PCA count equals to this value, the output of channel S/R Latch is set to 1.

CMPCR (PWM Channel A Compare Reset Register) DB

BITS	NAME	RW	DEF	DESCRIPTION
31-17	-	-	-	Reserved
16	DIR	RW	0	Direction Bit. This is used to compare with the direction bit of the PCA counter. It is ignored under Asymmetric mode.
15-0	COMPSET	RW	0x0000	Compare Value for R/S Latch Reset. When PCA count equals to this value, the output of channel S/R Latch is reset to 0.

There is no limitation on the order of SET and RESET instant. In typical case, SET instant occurs first and then RESET instant occurs after in one period. Since PWM channel outputs are derived from a S/R latches, the initial value of the S/R latch is defaulted to 0. If RESET precedes SET, then the RESET in the first period after enabling does not have any effect under default configuration. The initial value of S/R latch can be configured to 1 if desired.

The output of channel A, B, and C will each drive two complementary PWM outputs for driving the external driver's upper and lower legs. Channel A has X and U outputs, Channel B has Y and V output, Channel C has Z and W outputs. In defaults, U, V, and W correspond to the positive output of Channel A, B and C, while X, Y, and Z correspond to the complementary output of Channel A, B, and C.

CHACFG (PWM Channel A Configuration Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-24	WE	-	-	To protect accidental write to this register, WE must be equal to "5A" when writing to allow modification of the register content.
23-19	-	-	-	Reserved
18	EMGMODE	RW	0	Defines EMG mode 0 – Use EMGL as EMG condition 1 – Use EMG as EMG condition
17-16	OVLMODE	RW	00	Defines the OVL mode 00 – Use OVLL as OVL condition 01 – Use OVL as OVL condition 10 – Use OVLAL as OVL condition 11 – Use OVLA as OVL condition
15	-	-	-	Reserved.
14	UPOL	RW	0	This bit controls the polarity relationship of U output. In default, U is the

BITS	NAME	RW	DEF	DESCRIPTION
				same as the output of PWM output A. When set to 1, the polarity of U is inverted, thus become the complement of output A.
13	XPOL	RW	0	This bit controls the polarity relationship of X output. In default, X is complement to the output of PWM output A. When set to 1, the polarity of X is inverted, thus become same as output A.
12	UFDTEN	RW	0	This bit controls the falling edge dead time of U output. When set to 1, the rising edge of U output will be delayed specified by falling edge dead time of DEADTIME register. If set to 0, no dead time is inserted in the falling edge.
11	URDTEN	RW	0	This bit controls the rising edge dead time of U output. When set to 1, the rising edge of U output will be delayed specified by rising edge dead time of DEADTIME register. . If set to 0, no dead time is inserted in the rising edge.
10	XFDTEN	RW	0	This bit controls the falling edge dead time of X output. When set to 1, the rising edge of X output will be delayed specified by falling edge dead time of DEADTIME register. If set to 0, no dead time is inserted in the falling edge.
9	XRDTEN	RW	0	This bit controls the rising edge dead time of X output. When set to 1, the rising edge of X output will be delayed specified by rising edge dead time of DEADTIME register. . If set to 0, no dead time is inserted in the rising edge.
8	OVLSEL	RW	0	This bit select overload input. OVLSEL = 0 will use a global OVL signal. OVLSEL = 1 will use external OVL input pin, in this case, OVLA. Pin.
7-6	UEMG[1-0]	RW	00	This defines what state of U output when Emergency condition occurs. 00 = Force U to Hi-Z 01 = Force U low 10 = Force U high 11 = No Action
5-4	XEMG[1-0]	RW	00	This defines what state of X output when Emergency condition occurs. 00 = Force X to Hi-Z 01 = Force X low 10 = Force X high 11 = No Action
3-2	UOVL[1-0]	RW	00	This defines what state of U output when Overload condition occurs. 00 = Force U to Hi-Z 01 = Force U low 10 = Force U high 11 = No Action
1-0	XOVL[1-0]	RW	00	This defines what state of X output when Overload condition occurs. 00 = Force X to Hi-Z 01 = Force X low 10 = Force X high 11 = No Action

This register set the configuration of Channel A. Channel A has two output U and X, and one input for overload detection OVLA. The action of Overload and Emergency is immediate.

CHBCFG (PWM Channel B Configuration Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-24	WE	-	-	To protect accidental write to this register, WE must be equal to “5A” when writing to allow modification of the register content.
23-19	-	-	-	Reserved
18	EMGMODE	RW	0	Defines EMG mode 0 – Use EMGL as EMG condition 1 – Use EMG as EMG condition
17-16	OVLMODE	RW	00	Defines the OVL mode 00 – Use OVLL as OVL condition 01 – Use OVL as OVL condition 10 – Use OVLBL as OVL condition 11 – Use OVLB as OVL condition
15	-	-	-	Reserved.
14	VPOL	RW	0	This bit controls the polarity relationship of V output. In default, V is the same as the output of PWM output B. When set to 1, the polarity of V is inverted, thus become the complement of output B.
13	YPOL	RW	0	This bit controls the polarity relationship of Y output. In default, Y is complement to the output of PWM output B. When set to 1, the polarity of Y is inverted, thus become same as output B.
12	VFDTEN	RW	0	This bit controls the falling edge dead time of V output. When set to 1, the rising edge of V output will be delayed specified by falling edge dead time of DEADTIME register. If set to 0, no dead time is inserted in the falling edge.
11	VRDTEN	RW	0	This bit controls the rising edge dead time of V output. When set to 1, the rising edge of V output will be delayed specified by rising edge dead time of DEADTIME register. . If set to 0, no dead time is inserted in the rising edge.
10	YFDTEN	RW	0	This bit controls the falling edge dead time of Y output. When set to 1, the rising edge of Y output will be delayed specified by falling edge dead time of DEADTIME register. If set to 0, no dead time is inserted in the falling edge.
9	YRDTEN	RW	0	This bit controls the rising edge dead time of Y output. When set to 1, the rising edge of Y output will be delayed specified by rising edge dead time of DEADTIME register. . If set to 0, no dead time is inserted in the rising edge.
8	OVLSEL	RW	0	This bit select overload input. OVLSEL = 0 will use a global OVL signal. OVLSEL = 1 will use external OVL input pin, in this case, OVLB. Pin.
7-6	VEMG[1-0]	RW	00	This defines what state of V output when Emergency condition occurs. 00 = Force V to Hi-Z 01 = Force V low 10 = Force V high 11 = No Action
5-4	YEMG[1-0]	RW	00	This defines what state of Y output when Emergency condition occurs. 00 = Force Y to Hi-Z 01 = Force Y low 10 = Force Y high 11 = No Action
3-2	VOVL[1-0]	RW	00	This defines what state of V output when Overload condition occurs. 00 = Force V to Hi-Z

BITS	NAME	RW	DEF	DESCRIPTION
				01 = Force V low 10 = Force V high 11 = No Action
1-0	YOVL[1-0]	RW	00	This defines what state of Y output when Overload condition occurs. 00 = Force Y to Hi-Z 01 = Force Y low 10 = Force Y high 11 = No Action

This register set the configuration of Channel B. Channel B has two output V and Y, and one input for overload detection OVLB. The action of Overload and Emergency is immediate.

CHCCFG (PWM Channel C Configuration Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-24	WE	-	-	To protect accidental write to this register, WE must be equal to “5A” when writing to allow modification of the register content.
23-19	-	-	-	Reserved
18	EMGMODE	RW	0	Defines EMG mode 0 – Use EMGL as EMG condition 1 – Use EMG as EMG condition
17-16	OVLMODE	RW	00	Defines the OVL mode 00 – Use OVLL as OVL condition 01 – Use OVL as OVL condition 10 – Use OVLCL as OVL condition 11 – Use OVLC as OVL condition
15	-	-	-	Reserved.
14	WPOL	RW	0	This bit controls the polarity relationship of V output. In default, V is the same as the output of PWM output B. When set to 1, the polarity of V is inverted, thus become the complement of output B.
13	ZPOL	RW	0	This bit controls the polarity relationship of Y output. In default, Y is complement to the output of PWM output B. When set to 1, the polarity of Y is inverted, thus become same as output B.
12	WFDTEN	RW	0	This bit controls the falling edge dead time of V output. When set to 1, the rising edge of V output will be delayed specified by falling edge dead time of DEADTIME register. If set to 0, no dead time is inserted in the falling edge.
11	WRDTEN	RW	0	This bit controls the rising edge dead time of V output. When set to 1, the rising edge of V output will be delayed specified by rising edge dead time of DEADTIME register. . If set to 0, no dead time is inserted in the rising edge.
10	ZFDTEN	RW	0	This bit controls the falling edge dead time of Z output. When set to 1, the rising edge of Z output will be delayed specified by falling edge dead time of DEADTIME register. If set to 0, no dead time is inserted in the falling edge.
9	ZRDTEN	RW	0	This bit controls the rising edge dead time of Z output. When set to 1, the rising edge of Z output will be delayed specified by rising edge dead time of DEADTIME register. . If set to 0, no dead time is inserted in the rising edge.
8	OVLPOL	RW	0	This bit controls the external OVLX pin assertion polarity. 0 - high active

BITS	NAME	RW	DEF	DESCRIPTION
				1 – low active
7-6	WEMG[1-0]	RW	00	This defines what state of W output when Emergency condition occurs. 00 = Force W to Hi-Z 01 = Force W low 10 = Force W high 11 = No Action
5-4	ZEMG[1-0]	RW	00	This defines what state of Z output when Emergency condition occurs. 00 = Force Z to Hi-Z 01 = Force Z low 10 = Force Z high 11 = No Action
3-2	WOVL[1-0]	RW	00	This defines what state of W output when Overload condition occurs. 00 = Force W to Hi-Z 01 = Force W low 10 = Force W high 11 = No Action
1-0	ZOVL[1-0]	RW	00	This defines what state of Z output when Overload condition occurs. 00 = Force Z to Hi-Z 01 = Force Z low 10 = Force Z high 11 = No Action

This register set the configuration of Channel C. Channel C has two outputs W and Z, and one input for overload detection OVLC. The action of Overload and Emergency is immediate.

CHFORCE (PWM Channel Force Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-24	WE	-	-	To protect accidental write to this register, WE must be equal to “5A” when writing to allow modification of the register content.
23-22	-	-	-	Reserved
21	UFORCE	RW	1	0 – No force action. 1 – Allow force action of output V.
20	XFORCE	RW	1	0 – No force action. 1 – Allow force action of output Y.
19	UVALUE	RW	0	0 – Force U output to low. 1 – Force U output to high.
18	XVALUE	RW	0	0 – Force X output to low. 1 – Force X output to high.
17	UHZ	RW	1	0 – No action 1 – Force U output to HI-Z. Has higher priority than force 0 or 1.
16	XHZ	RW	1	0 – No action 1 – Force X output to HI-Z. Has higher priority than force 0 or 1.
15-14	-	-	-	Reserved
13	VFORCE	RW	1	0 – No force action. 1 – Allow force action of output V.
12	YFORCE	RW	1	0 – No force action. 1 – Allow force action of output Y.
11	VVALUE	RW	0	0 – Force V output to low. 1 – Force V output to high.

BITS	NAME	RW	DEF	DESCRIPTION
10	YVALUE	RW	0	0 – Force Y output to low. 1 – Force Y output to high.
9	VHZ	RW	1	0 – No action 1 – Force V output to HI-Z. Has higher priority than force 0 or 1.
8	YHZ	RW	1	0 – No action 1 – Force Y output to HI-Z. Has higher priority than force 0 or 1.
7-6	-	-	-	Reserved
5	WFORCE	RW	1	0 – No force action. 1 – Allow force action of output W.
4	ZFORCE	RW	1	0 – No force action. 1 – Allow force action of output Z.
3	WVALUE	RW	0	0 – Force W output to low. 1 – Force W output to high.
2	ZVALUE	RW	0	0 – Force Z output to low. 1 – Force Z output to high.
1	WHZ	RW	1	0 – No action 1 – Force W output to HI-Z. Has higher priority than force 0 or 1.
0	ZHZ	RW	1	0 – No action 1 – Force Z output to HI-Z. Has higher priority than force 0 or 1.

This register when written by software will overwrite the PWM output with specified value. This allows the software for ultimate control over PWM outputs. When writing into this register Bit[31-24] must be “5A’ to allow actual modification. If Bit[31-24] is not “5A”, the write action is ignored. The force actions are immediate meaning the effect is immediate reflected on the outputs without delays. Note all outputs of PWM, U/V/W and X/Y/Z are in Hi-Z states after any reset as the default force setting.

CHSTATUS (PWM Channel STATUS Register) RO

BITS	NAME	RW	DEF	DESCRIPTION
31-6	-	-	-	Reserved
5	UVALUE	RO	0	This returns the current state of the U output pin. This is read from input buffer.
4	VVALUE	RO	0	This returns the current state of the V output pin. This is read from input buffer.
3	WVALUE	RO	0	This returns the current state of the W output pin. This is read from input buffer.
2	XVALUE	RO	0	This returns the current state of the X output pin. This is read from input buffer.
1	YVALUE	RO	0	This returns the current state of the Y output pin. This is read from input buffer.
0	ZVALUE	RO	0	This returns the current state of the Z output pin. This is read from input buffer.

This register is read only and when read returns the status of the PWM output channels.

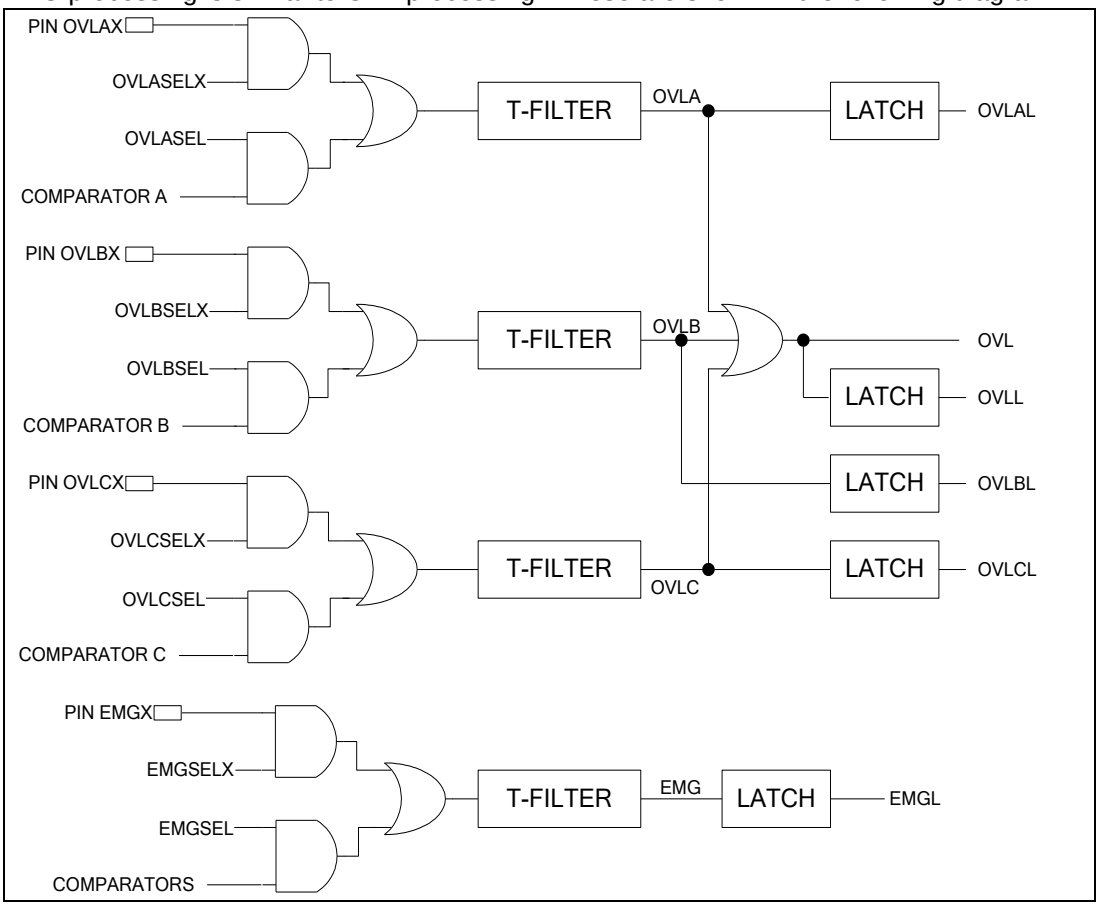
DEADTIME (DEAD TIME Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-16	-	-	-	Reserved
15-8	FALLDT[7-0]	RW	0x00	This specifies the falling edge dead time. The dead time is FALLDT * DTPRD.
7-0	RISEDT[7-0]	RW	0x00	This specifies the rising edge dead time. The dead time is RISEDT * DTPRD.

This register defines the dead time of the rising and falling edges of the channel outputs. All outputs have the same dead time. The time unit of the dead time is specified in PCA_CFG register as DTPRD. The dead time is applied at the last stage of the output after polarity control. Rising edge and falling edges are referring to actual output signals on U/V/W and X/Y/Z pins.

5.3 Protection Logic

The protection logic detects various abnormal conditions including external inputs and internal comparator outputs then acts upon these abnormal conditions to specified action either stopping the PWM or disable the PWM output. The abnormal conditions are classified into two categories, EMG (Emergence) and OVL (Overload). There are three analog comparators associated with these conditions which will be described in the later sections. The conditions for EMG and OVL can be specified as external input pins or the outputs from these analog comparators. When enabled, EMG and OVL status can be read and used to trigger actions on the PWM outputs, in addition, it can be used to generate interrupt for notifying software. For OVL condition, each channel has one external input pin, OVLA, OVLB, and OVLC. And the OVL condition can be specified as the assertion of the corresponding external pin, and/or one of the three comparator outputs. The global OVL is asserted by OR of the three channel's OVL conditions. EMG processing is similar to OVL processing. These are shown in the following diagram.



When protection condition is trigger, a protection interrupt is generated. This is separated from motor PCA allowing the software to handle the protection separately. The interrupt flag is shared in PCTSTAT register.

PRCTCFG (Protection Configuration Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-24	PROTCTWR	WO	0x00	To prevent accidental writing to this register, Bit[31-24] needs to be "5A" for write operation to be effective.
23-16	EMGFILTER [7-0]	RW	0x00	This set the pulse filter of the EMG condition. The minimum pulse width is set by EMGFILER[7-0] * EMGOVLPD.
15-8	OVLFILTER [7-0]	RW	0x00	This set the pulse filter of the OVL condition. The minimum pulse width is set by OVLFILER[7-0]*EMGOVLPD.
7	EMGSEL	RW	0	0 – Ignore analog comparator 1 – Use comparator results
6	EMGSELX	RW	0	This bit controls the definition of EMG 0 – Ignore the EMG external pin 1 – Enable EMG external pin
5	OVLASEL	RW	0	0 – Ignore comparator A 1 – Use comparator A
4	OVLBSEL	RW	0	0 – Ignore comparator B 1 – Use comparator B
3	OVLCSEL	RW	0	0 – Ignore comparator C 1 – Use comparator C
2	OVLASELX	RW	0	This bit controls the definition of OVLA. 0 – Ignore the OVLA external pin. 1 – Enable OVLA external pin.
1	OVLBSELX	RW	0	This bit controls the definition of OVLB. 0 – Ignore the OVLB external pin. 1 – Enable OVLB external pin.
0	OVLCSELX	RW	0	This bit controls the definition of OVLC. 0 – Ignore the OVLC external pin. 1 – Enable OVLC external pin.

When EMGSEL=1, the EMG condition includes the status of the analog window comparators. Combination of comparator results can be included which is specified in the comparator channel configuration registers. Expressing in equation, the EMG condition is
PRCTCFG(EMGSELX) && EMGX + PRCTCFG(EMGSEL) && [
CMPCHA(MEMGEN)&&CMPAOUT + CMPCHB(MEMGEN)&&CMPBOUT + CMPCHC(MEMGEN)&&CMPCOUT + CMPCHD(MEMGEN)&&CMPDOUT + CMPCHE(MEMGEN)&&CMPEOUT].

PRCTSTAT (Protection Status Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-24	WE	WO	0x00	To prevent accidental writing to this register, Bit[31-24] needs to be "5A" for write operation to be effective.
23-10	-	-	-	Reserved
9	EMGL	RW	0	This bit is read as 1 after EMG condition has occurred and latched. This bit must be cleared by software.
8	EMG	RO	0	This bit is read as 1 when EMG condition is asserted.
7	OVLL	RW	0	This bit is read as 1 after OVL condition on channel A, or B, or C has occurred and latched. This bit must be cleared by software.
6	OVLAL	RW	0	This bit is read as 1 after OVL condition on channel A has occurred and latched. This bit must be cleared by software.
5	OVLBL	RW	0	This bit is read as 1 after OVL condition on channel B has occurred and latched. This bit must be cleared by software.
4	OVLCL	RW	0	This bit is read as 1 after OVL condition on channel C has occurred and latched. This bit must be cleared by software.
3	OVL	RO		This bit is read as 1 when OVL condition on channel A, or B, or C.
2	OVLA	RO	0	This bit is read as 1 when OVL condition on channel A.
1	OVLB	RO	0	This bit is read as 1 when OVL condition on channel B.
0	OVLC	RO	0	This bit is read as 1 when OVL condition on channel C.

This register when read returns the current status of Protection logic. The latched status bits must be cleared by software. These status output are also send to Channel circuits to active the protections. The configurations of the protection are implemented in the Channel Configuration registers. The priority of protection is EMG > OVL > Force.

5.4 Synchronization and Interrupt

The synchronization of MPCA provides triggering of the ADC conversion as well as generates interrupt to CPU. There are total six triggering setting by ITCMP0 to ITCMP6 associated with MPCA timing. Each of this can be used for ADC conversion triggering and/or for generating interrupt. For ADC conversion triggering, any one of the five ADC channels can be selected. The trigger can also specify whether an EOC interrupt by ADC should be enabled or not. All Compare Registers are double buffered and updated at MPCA period or zero count. The relationship of each trigger condition and timing of ADC is further explained in the ADC sections.

ITCMP0 (Interrupt and Synchronization Compare Register 0) DB

BITS	NAME	RW	DEF	DESCRIPTION
31	INTEN	RW	0	Set this bit to 1 to enable PCA interrupt when ITCMP0=PCACNT.
30-29	-	-	-	Reserved.
28-26	ADCCHSEL	RW	000	ADC Channel Select. This selects which channel to S/H and convert when triggering ADC. 000-ADCINA, 001-ADCINB, 010-ADCINC, 011-ADCIND, 100-ADCINE. Other settings are ADCINE.
25	ADCEOCINT	RW	0	Set this bit to 1 to enable ADC end of conversion interrupt of ADC triggering.
24	ADCTRG	RW	0	Set this bit to 1 to trigger ADC conversion when ITCMP is equal to PCA count.
23	BPDB	RW	0	Set this bit to bypass double buffer. Default is 0 and the update occurs as DBUPD defined.
22-17	-	-	-	Reserved
16	DIR	RW	0	Compare to the DIR bit of PCA counter. To operate in Asymmetric mode, this bit should always set to 0.
15-0	ITCMP[15-0]	RW	0	Compare value used to compare with PCA counter

ITCMP1 (Interrupt and Synchronization Compare Register 1) DB

BITS	NAME	RW	DEF	DESCRIPTION
31	INTEN	RW	0	Set this bit to 1 to enable PCA interrupt when ITCMP1=PCACNT.
30-29	-	-	-	Reserved.
28-26	ADCCHSEL	RW	000	ADC Channel Select. This selects which channel to S/H and convert when triggering ADC. 000-ADCINA, 001-ADCINB, 010-ADCINC, 011-ADCIND, 100-ADCINE. Other settings are ADCINE.
25	ADCEOCINT	RW	0	Set this bit to 1 to enable ADC end of conversion interrupt of ADC triggering.
24	ADCTRG	RW	0	Set this bit to1 to trigger ADC conversion when ITCMP is equal to PCA count.
23	BPDB	RW	0	Set this bit to bypass double buffer. Default is 0 and the update occurs as DBUPD defined.
22-17	-	-	-	Reserved
16	DIR	RW	0	Compare to the DIR bit of PCA counter. To operate in Asymmetric mode, this bit should always set to 0.
15-0	ITCMP[15-0]	RW	0	Compare value used to compare with PCA counter

ITCMP2 (Interrupt and Synchronization Compare Register 2) DB

BITS	NAME	RW	DEF	DESCRIPTION
31	INTEN	RW	0	Set this bit to 1 to enable PCA interrupt when ITCMP2=PCACNT.
30-29	-	-	-	Reserved.
28-26	ADCCHSEL	RW	000	ADC Channel Select. This selects which channel to S/H and convert when triggering ADC. 000-ADCINA, 001-ADCINB, 010-ADCINC, 011-ADCIND, 100-ADCINE. Other settings are ADCINE.
25	ADCEOCINT	RW	0	Set this bit to 1 to enable ADC end of conversion interrupt of ADC triggering.
24	ADCTRG	RW	0	Set this bit to1 to trigger ADC conversion when ITCMP is equal to PCA count.
23	BPDB	RW	0	Set this bit to bypass double buffer. Default is 0 and the update occurs as DBUPD defined.
22-17	-	-	-	Reserved
16	DIR	RW	0	Compare to the DIR bit of PCA counter. To operate in Asymmetric mode, this bit should always set to 0.
15-0	ITCMP[15-0]	RW	0	Compare value used to compare with PCA counter

ITCMP3 (Interrupt and Synchronization Compare Register 3) DB

BITS	NAME	RW	DEF	DESCRIPTION
31	INTEN	RW	0	Set this bit to 1 to enable PCA interrupt when ITCMP3=PCACNT.
30-29	-	-	-	Reserved.
28-26	ADCCHSEL	RW	000	ADC Channel Select. This selects which channel to S/H and convert when triggering ADC. 000-ADCINA, 001-ADCINB, 010-ADCINC, 011-ADCIND, 100-ADCINE. Other settings are ADCINE.
25	ADCEOCINT	RW	0	Set this bit to 1 to enable ADC end of conversion interrupt of ADC triggering.
24	ADCTRG	RW	0	Set this bit to1 to trigger ADC conversion when ITCMP is equal to PCA count.
23	BPDB	RW	0	Set this bit to bypass double buffer. Default is 0 and the update occurs

BITS	NAME	RW	DEF	DESCRIPTION
				as DBUPD defined.
22-17	-	-	-	Reserved
16	DIR	RW	0	Compare to the DIR bit of PCA counter. To operate in Asymmetric mode, this bit should always set to 0.
15-0	ITCMP[15-0]	RW	0	Compare value used to compare with PCA counter

ITCMP4 (Interrupt and Synchronization Compare Register 4) DB

BITS	NAME	RW	DEF	DESCRIPTION
31	INTEN	RW	0	Set this bit to 1 to enable PCA interrupt when ITCMP4=PCACNT.
30-29	-	-	-	Reserved.
28-26	ADCCHSEL	RW	000	ADC Channel Select. This selects which channel to S/H and convert when triggering ADC. 000-ADCINA, 001-ADCINB, 010-ADCINC, 011-ADCIND, 100-ADCINE. Other settings are ADCINE.
25	ADCEOCINT	RW	0	Set this bit to 1 to enable ADC end of conversion interrupt of ADC triggering.
24	ADCTRG	RW	0	Set this bit to1 to trigger ADC conversion when ITCMP is equal to PCA count.
23	BPDB	RW	0	Set this bit to bypass double buffer. Default is 0 and the update occurs as DBUPD defined.
22-17	-	-	-	Reserved
16	DIR	RW	0	Compare to the DIR bit of PCA counter. To operate in Asymmetric mode, this bit should always set to 0.
15-0	ITCMP[15-0]	RW	0	Compare value used to compare with PCA counter

ITCMP5 (Interrupt and Synchronization Compare Register 5) DB

BITS	NAME	RW	DEF	DESCRIPTION
31	INTEN	RW	0	Set this bit to 1 to enable PCA interrupt when ITCMP1=PCACNT.
30-29	-	-	-	Reserved.
28-26	ADCCHSEL	RW	000	ADC Channel Select. This selects which channel to S/H and convert when triggering ADC. 000-ADCINA, 001-ADCINB, 010-ADCINC, 011-ADCIND, 100-ADCINE. Other settings are ADCINE.
25	ADCEOCINT	RW	0	Set this bit to 1 to enable ADC end of conversion interrupt of ADC triggering.
24	ADCTRG	RW	0	Set this bit to1 to trigger ADC conversion when ITCMP is equal to PCA count.
23	BPDB	RW	0	Set this bit to bypass double buffer. Default is 0 and the update occurs as DBUPD defined.
22-17	-	-	-	Reserved
16	DIR	RW	0	Compare to the DIR bit of PCA counter. To operate in Asymmetric mode, this bit should always set to 0.
15-0	ITCMP[15-0]	RW	0	Compare value used to compare with PCA counter

PSYNCCFG (PWM Interrupt and Synchronization Configuration Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-21	-	-	-	Reserved.
20	EMGINTEN	RW	0	Set this bit to 1 to enable EMG interrupt. This condition is on EMG assertion.
19	OVLINTEN	RW	0	Set this bit to 1 to enable OVL (Overload) interrupt. This condition is on OVL assertion.
18	OVLAINTEN	RW	0	Set this bit to 1 to enable Channel A OVL interrupt. This condition is on OVLA assertion.
17	OVLBINTEN	RW	0	Set this bit to 1 to enable Channel B OVL interrupt. This condition is on OVLB assertion.
16	OVLCINTEN	RW	0	Set this bit to 1 to enable Channel C OVL interrupt. This condition is on OVLC assertion.
15	PRDINTEN	RW	0	Set this bit to 1 to enable PWM period interrupt. This condition is asserted when PCACNT = PCAPRD.
14	ZRINTEN	RW	0	Set this bit to 1 to enable PWM zero interrupt. This condition is asserted when PCACNT = 0.
13-0	-	-	-	Reserved

PINTSTAT (PWM Interrupt Status Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-16	-	-	-	Reserved.
15	SCOUNT	RW	0	SPCA Count=0 Interrupt Flag. This must be cleared by software
14	SITCMP1F	RW	0	SPCA SITCMP1 Interrupt Flag. This must be cleared by software.
13	SITCMP0F	RW	0	SPCA SITCMP0 Interrupt Flag. This must be cleared by software.
12	EMGINTF	RW	0	EMG Interrupt Flag. This must be cleared by software.
11	OVLINTF	RW	0	OVL Interrupt Flag. This must be cleared by software.
10	OVLAINTF	RW	0	OVLA Interrupt Flag. This must be cleared by software.
9	OVLBINTF	RW	0	OVLB Interrupt Flag. This must be cleared by software.
8	OVLCINTF	RW	0	OVLC Interrupt Flag. This must be cleared by software.
7	PRDINTF	RW	0	PRD Interrupt Flag. This must be cleared by software.
6	ZRINTF	RW	0	ZERO Interrupt Flag. This must be cleared by software.
5	CMP5INTF	RW	0	ITCMP5 Interrupt Flag. This must be cleared by software.
4	CMP4INTF	RW	0	ITCMP4 Interrupt Flag. This must be cleared by software.
3	CMP3INTF	RW	0	ITCMP3 Interrupt Flag. This must be cleared by software.
2	CMP2INTF	RW	0	ITCMP2 Interrupt Flag. This must be cleared by software.
1	CMP1INTF	RW	0	ITCMP1 Interrupt Flag. This must be cleared by software.
0	CMP0INTF	RW	0	ITCMP0 Interrupt Flag. This must be cleared by software.

This register is the interrupt status of PWM module. The set bit of this register must be cleared by software. It is also necessary to clear the flags in the corresponding interrupt source such OVLL and EMGL.

5.5 Sub-PCA and PWM Channels

The sub-PCA provides a synchronous timing base that can subdivide the main PCA period. Sub-PCA can be used to generate PWM output with frequency in integer multiples of main PWM. SPCA can be configured to be always cleared to 0 and restart when main PCA counter is 0 and restarted. It is necessary for software to ensure that main PCA period is in integer multiples of SPCA periods. SPCA can also be configured to be decoupled with MPCA operations. The SPCA always functions as asymmetric mode and it is in 17-bit. If configured properly, SPCA can be identical to main PCA. The double buffer operation always occurs at SPCACNT=0 instant. The interrupts from SPCA use an independent interrupt in interrupt vector and priority for easy software processing. The PWM outputs are also controlled by the window comparators to allow overload condition to overwrite PWM output into tri-state. This is configurable in the comparator section of Channel D and E comparators.

SPCACNT (SPCA Counter Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-24	CNTCLR	WO	0	Write these bits with 0x55 will force the Counter to be cleared to 0x0000 with DIR = 0. The clear action is always immediate.
23-18	-	-	-	Reserved
17	COUNT0IE	RW	0	COUNT0IE=1 will enable the interrupt when SCOUNT=0.
16-0	SCOUNT [16-0]	RO	0x0000	PCA Counting Value. When read, the value of current count is read out.

SPCAPRD (SPCA Period Register) DB

BITS	NAME	RW	DEF	DESCRIPTION
31-24	WRIMD	WO	0000	If bit[31-24]=11111111, then the write operation will bypass the double buffer operation and immediate update.
23	SYNC	RW	0	SYNC=0 will decouple the SPCA with MPCA, in another word, SPCA operates independent with MPCA. SYNC=1 will synchronize SPCA count with MPCA by forcing SPCA to be 0 and restart when MPCA count is 0.
22-17	-	-	-	Reserved
16-0	SPERIOD [16-0]	RW	0x0000	Sub PCA Count Period. This defines the Sub PCA period. The counter is restart from 0 when reach to Period. For proper synchronization with main PCA, this should be set to a value which can be fully divided by the main PCA period.

SCMPDS (SPCA PWM Channel SD Compare Register) DB

BITS	NAME	RW	DEF	DESCRIPTION
31-24	WRIMD	WO	0000	If bit[31-24]=11111111, then the write operation will bypass the double buffer operation and immediate update.
23-17	-	-	-	Reserved
16-0	SCMPDS [16-0]	RW	0x0000	Compare Value for PWM SD Output. When SPCA count is less than this value, the output of channel is 0. When SPCA count is equal or greater than this value, the output of the channel is 1.

SCMPDE (SPCA PWM Channel SE Compare Register) DB

BITS	NAME	RW	DEF	DESCRIPTION
31-24	WRIMD	WO	0000	If bit[31-24]=11111111, then the write operation will bypass the double buffer operation and immediate update.
23-17	-	-	-	Reserved
16-0	SCMPDE [16-0]	RW	0x0000	Compare Value for PWM SD Output. When SPCA count is less than this value, the output of channel is 0. When SPCA count is equal or greater than this value, the output of the channel is 1.

There are two triggering setting for SPCA, SITCMP0 and SITCMP1. Each can be used for interrupt to CPU and/or for ADC conversion triggering.

SITCMP0 (SPCA Interrupt and Synchronization Compare Register 0) DB

BITS	NAME	RW	DEF	DESCRIPTION
31	INTEN	RW	0	Set this bit to 1 to enable PCA interrupt when ITCMP1=PCACNT.
30-29	-	-	-	Reserved.
28-26	ADCCHSEL	RW	000	ADC Channel Select. This selects which channel to S/H and convert when triggering ADC. 000-ADCINA, 001-ADCINB, 010-ADCINC, 011-ADCIND, 100-ADCINE. Other settings are ADCINE.
25	ADCEOCINT	RW	0	Set this bit to 1 to enable ADC end of conversion interrupt of ADC triggering.
24	ADCTRG	RW	0	Set this bit to1 to trigger ADC conversion when SITCMP is equal to SPCA count.
23	BPDB	RW	0	Set this bit to bypass double buffer. Default is 0 and the update occurs as DBUPD defined.
22-17	-	-	-	Reserved
16-0	SITCMP0 [16-0]	RW	0	Compare value used to compare with SPCA counter.

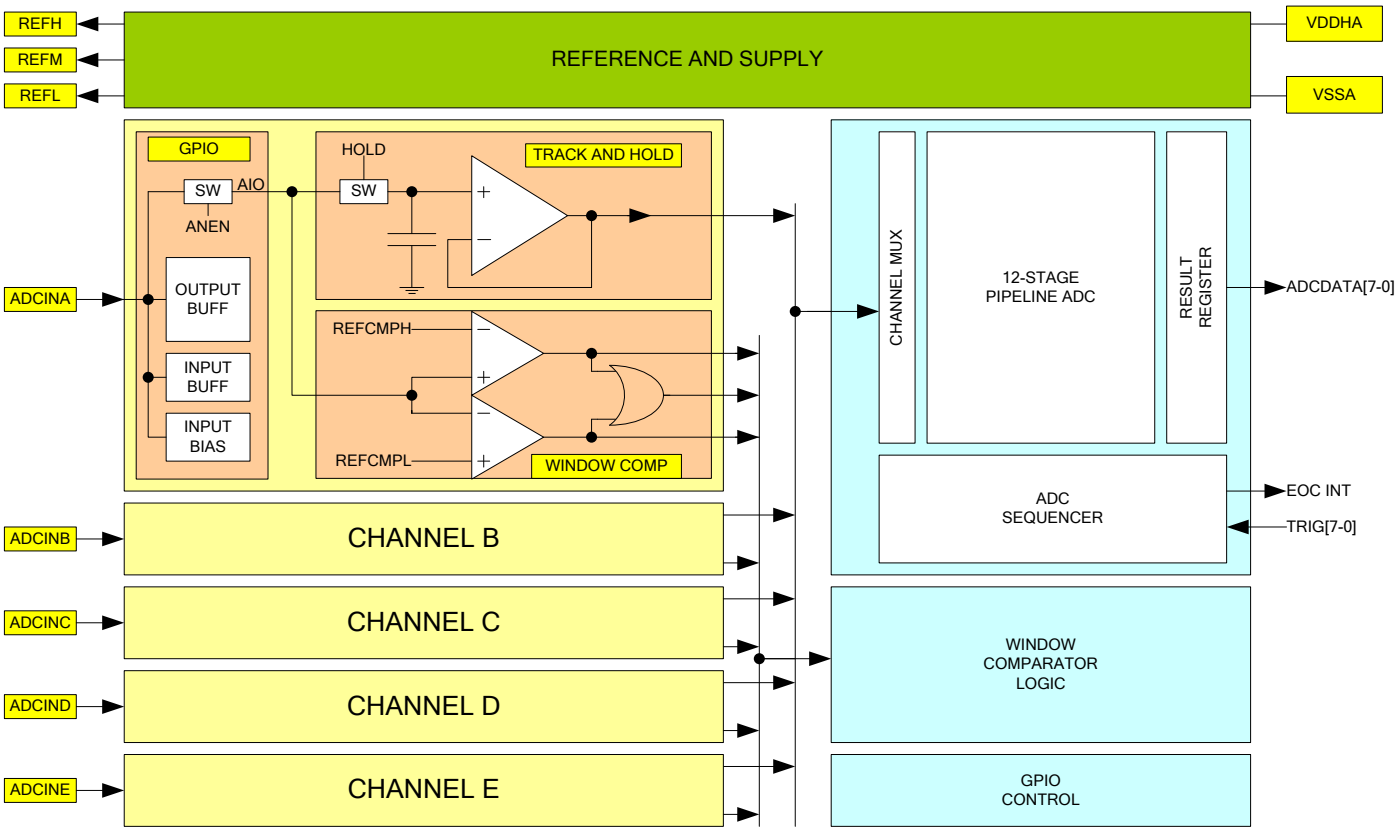
SITCMP1 (SPCA Interrupt and Synchronization Compare Register 1) DB

BITS	NAME	RW	DEF	DESCRIPTION
31	INTEN	RW	0	Set this bit to 1 to enable PCA interrupt when ITCMP1=PCACNT.
30-29	-	-	-	Reserved.
28-26	ADCCHSEL	RW	000	ADC Channel Select. This selects which channel to S/H and convert when triggering ADC. 000-ADCINA, 001-ADCINB, 010-ADCINC, 011-ADCIND, 100-ADCINE. Other settings are ADCINE.
25	ADCEOCINT	RW	0	Set this bit to 1 to enable ADC end of conversion interrupt of ADC triggering.
24	ADCTRG	RW	0	Set this bit to1 to trigger ADC conversion when SITCMP is equal to SPCA count.
23	BPDB	RW	0	Set this bit to bypass double buffer. Default is 0 and the update occurs as DBUPD defined.
22-17	-	-	-	Reserved
16-0	SITCMP1 [16-0]	RW	0	Compare value used to compare with SPCA counter.

6. Pipeline ADC and Overload Comparator

The pipeline ADC has five input channels and each is shared with a GPIO port. Each ADC input is also connected to a pair of analog window comparator. The analog input of the GPIO must be enabled to allow the input to be connected to the ADC input channel and the window comparator and all the driving functions of the GPIO should be disabled for proper operation of the analog signal processing. The connection block diagram of GPIO input, Pipeline ADC and the analog window comparators are shown in the following.

The Track and Hold (T/H) front-end. The pipeline ADC when enabled consumes about 15mA while the analog comparators consumes about 3mA. The following figure shows the overall block diagram.



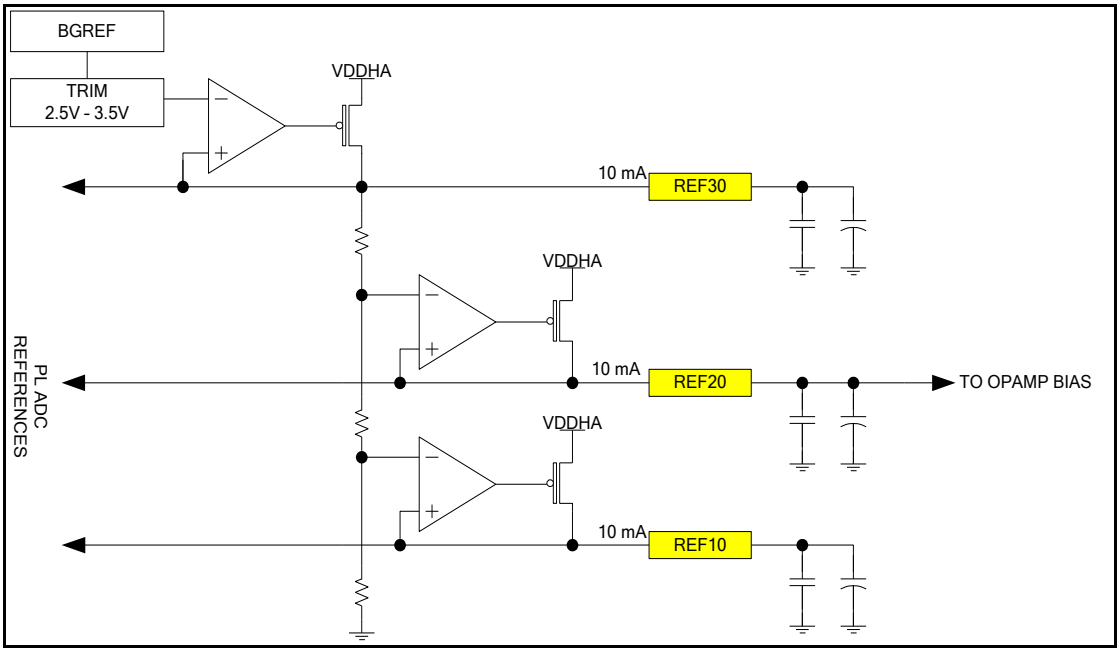
6.1 GPIO and S/H

Each ADC channel input is also shared with GPIO functions. The ADC input is connected to the GPIO's ANIO terminals through an analog switch to the pin. To allow actual connection, the corresponding GPIO's configuration must be set correctly to enable the analog switch. The GPIO uses VDDHA and VSSA for digital I/O driving and buffering. To minimize interference, the I/O drive of the GPIO should also be disabled.

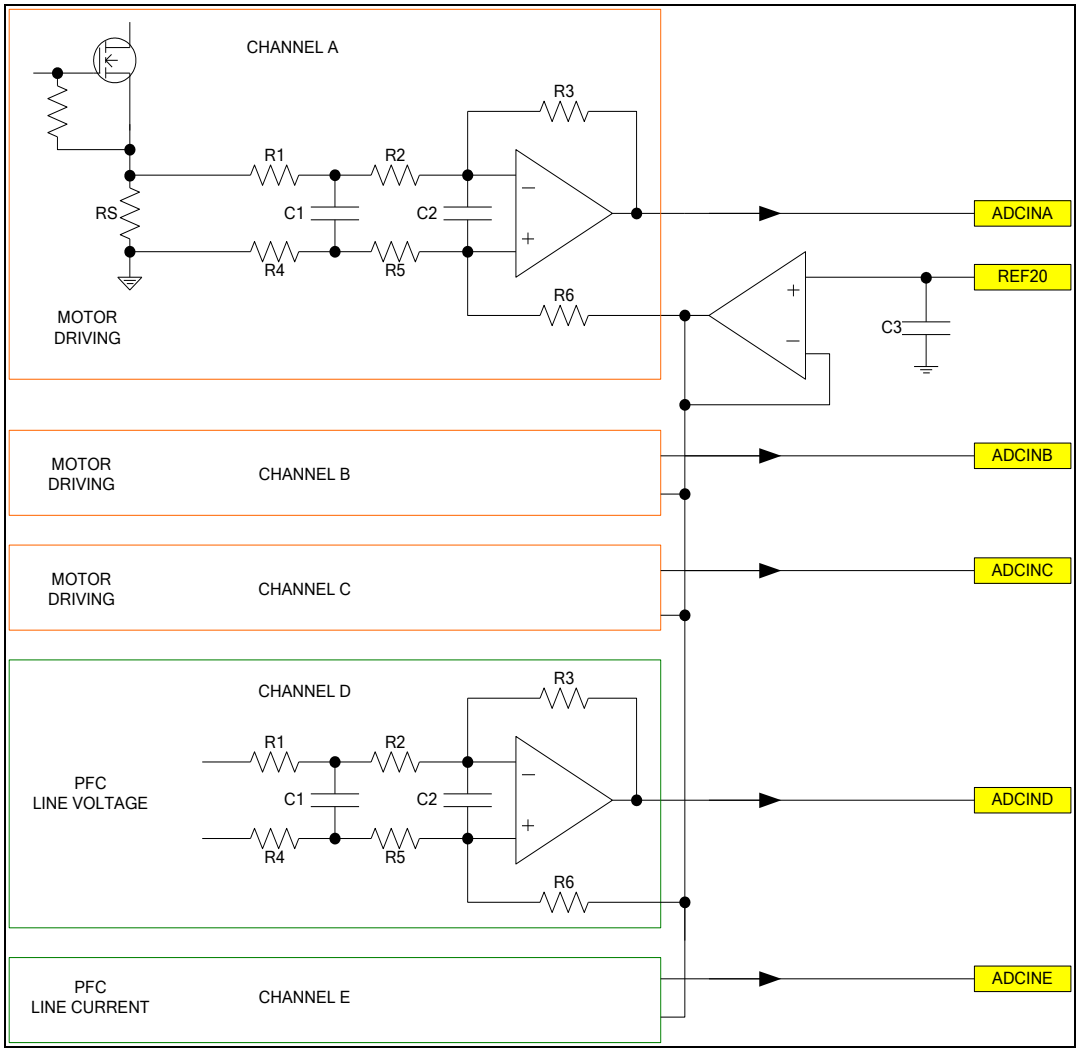
Each channel input is first connected to a sample and hold circuits. When triggered, the sample and hold circuit will hold the voltage at the triggering instant.

6.2 Input Signal Condition and Range

The pipe-line ADC has a full-range of 2.0V and its DC range is 1.0V to 3V. Three reference levels are required for ADC, REF30 (3.0V), REF20 (2.0V), and REF10 (1.0V). REF30 voltage is a trim-able level which can be fine adjusted to cancel chip to chip variation. REF30 is also used to generate REF20 and REF10 levels using resistor dividing networks. All these three levels are brought out to external pins for external applications as well as decoupling. Good decoupling between these levels to VSSA is necessary to ensure good accuracy of ADC. The connection diagram of the ADC reference circuit is shown in the following diagram. Also note these references are driven by internal buffers which only provide sourcing capabilities, thus only pull-down loads should connected to these references. REF20 is important because it is used to bias the external signal conditioning circuit and provides correct DC bias to the input signal to fit the ADC input range.



Since the input range of ADC is from 1V to 3V, it is required to do level shifting on the input signal to fit the full-scale of the ADC. This is typically done through external OPAMP which provides low-pass filtering for anti-aliasing as well as signal amplification. A typical application circuits is shown in the following circuit.



In the above circuit, R1/R2/R4/R5 and C1/C2 provide low-pass filtering. If R3=R6, then the DC center is shift to REF20. The signal amplification factor is R3/(R1+R2) = R6/(R4+R5).

6.3 ADC Triggering and Sequencer Operations

All ADC conversions are triggered by MPCA or SPCA trigger setting. There are total 8 trigger settings, 6 of them are associated with MPCA (ITCMP0/1/2/3/4/5) and 2 of them are associated with SPCA (SITCMP0/1). Each triggering can specify one of the five channels and the condition of the trigger. Therefore a channel can be triggered for conversion by multiple triggers, and it is also possible that several triggers occur at the same time. Please see the detail description in the MPCA and SPCA sections.

When the channel is triggered for conversion, it is first sample and held, the sequencer will arrange the held signal to be put into the pipeline for conversion. If there is no pending conversion, it is put into the pipeline immediately. If there is a higher priority channel waiting to be converted, the sequencer will first complete the higher priority channel then put in the lower priority channel.

When more than one channel is triggered by different trigger at the same time, there is a natural priority in the conversion of the channels. Channel A has higher priority than B, then C, D, and E. However this should not affect the accuracy of the conversion because the input signals are sampled and held at the same instant as the triggering occurs. The priority of the channels will put the higher priority channel into the pipeline first and thus the conversion result will be ready earlier.

A channel can also be triggered successively with interval longer than 4 ADC clock periods (1usec when ADC clock is 4MHz). This is the minimum time the sequencer needs to process the sample and hold circuit and direct the held signal into the pipeline. However, an extreme situation can happen that the second trigger occurs while the first triggered signal is still waiting for the sequencer due to there are higher pending channels. This will cause the overrun of the S/H and thus ruin the previous held signal. When this condition happens, S/H overrun error flag of the triggered channel will be set at the ADC flag register. Also the first trigger is aborted by the sequencer and due to the overrun the converted results of the second trigger will not be correct.

The conversion results of ADC are stored according to its trigger sources. Since there are 8 trigger sources, there are also 8 conversion result registers. As described in MPCA and SPCA section, each trigger source can specify whether EOC interrupt is enabled for the trigger. Usually for several sequential triggers, only the last trigger will turn on its EOC interrupt. This allow the software to respond to only one EOC request and collect all the conversion results in one place. For each conversion result register, there is a “NEW” bit which is set by the hardware indicating a new result is ready, and there is also an “DAOVR” bit indicating that an old result was written over by new result before the old result was read out by the CPU.

The pipeline ADC when enabled consumes about 20mA including the sample and hold circuits, the reference generator and the pipeline stages.

6.4 ADC Registers

PADCCONF (Pipeline ADC Configuration Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31	ADCEN	RW	0	ADC Enable 0 – Disable. This disables all the references and ADC circuits. 1 – Enable. There is 5msec initialization time after enable.
30-24	-	-	-	Reserved
23-16	REF30TM[7-0]	RW	00	REF30 Regulator Trim The trimming range is between 2.5V to 3.5V.
15-8	ADCCKS[7-0]	RW	0x00	ADC Clock Divider. The ADC clock is SYSCLK/2/ADCCKS[7-0]
7-0	-	-	-	Reserved

PADCINTF (ADC Interrupt Flag)

BITS	NAME	RW	DEF	DESCRIPTION
31-13	-	-	-	Reserved
12	SHOVRCHE	RW	0	This bit is set to 1 by hardware indicating that there was overrun at the S/H stage of the S/H on channel E. This is caused by two successive triggering of the same channel within too short interval. The previous sampled voltage triggered by another triggering condition was overrun. And the hardware will thus cancel the previous trigger and proceed with new triggering. When this condition occurs, the current conversion result may not be correct. This must be cleared by software.
11	SHOVRCHD	RW	0	This bit is set to 1 by hardware indicating that there was overrun at the S/H stage of the S/H on channel D. This is caused by two successive triggering of the same channel within too short interval. The previous sampled voltage triggered by another triggering condition was overrun. And the hardware will thus cancel the previous trigger and proceed with new triggering. When this condition occurs, the current conversion result may not be correct. This must be cleared by software.
10	SHOVRCHC	RW	0	This bit is set to 1 by hardware indicating that there was overrun at the S/H stage of the S/H on channel C. This is caused by two successive triggering of the same channel within too short interval. The previous sampled voltage triggered by another triggering condition was overrun. And the hardware will thus cancel the previous trigger and proceed with new triggering. When this condition occurs, the current conversion result may not be correct. This must be cleared by software.
9	SHOVRCHB	RW	0	This bit is set to 1 by hardware indicating that there was overrun at the S/H stage of the S/H on channel B. This is caused by two successive triggering of the same channel within too short interval. The previous sampled voltage triggered by another triggering condition was overrun. And the hardware will thus cancel the previous trigger and proceed with new triggering. When this condition occurs, the current conversion result may not be correct. This must be cleared by software.
8	SHOVRCHA	RW	0	This bit is set to 1 by hardware indicating that there was overrun at the S/H stage of the S/H on channel A. This is caused by two successive triggering of the same channel within too short interval. The previous sampled voltage triggered by another triggering condition was overrun. And the hardware will thus cancel the previous trigger and proceed with new triggering. When this condition occurs, the current conversion result may not be correct. This must be cleared by software.

BITS	NAME	RW	DEF	DESCRIPTION
7	ADCIF7	RW	0	This bit is set to 1 to indicate the EOC condition of trigger 7. This must be cleared by software.
6	ADCIF6	RW	0	This bit is set to 1 to indicate the EOC condition of trigger 6. This must be cleared by software.
5	ADCIF5	RW	0	This bit is set to 1 to indicate the EOC condition of trigger 5. This must be cleared by software.
4	ADCIF4	RW	0	This bit is set to 1 to indicate the EOC condition of trigger 4. This must be cleared by software.
3	ADCIF3	RW	0	This bit is set to 1 to indicate the EOC condition of trigger 3. This must be cleared by software.
2	ADCIF2	RW	0	This bit is set to 1 to indicate the EOC condition of trigger 2. This must be cleared by software.
1	ADCIF1	RW	0	This bit is set to 1 to indicate the EOC condition of trigger 1. This must be cleared by software.
0	ADCIF0	RW	0	This bit is set to 1 to indicate the EOC condition of trigger 0. This must be cleared by software.

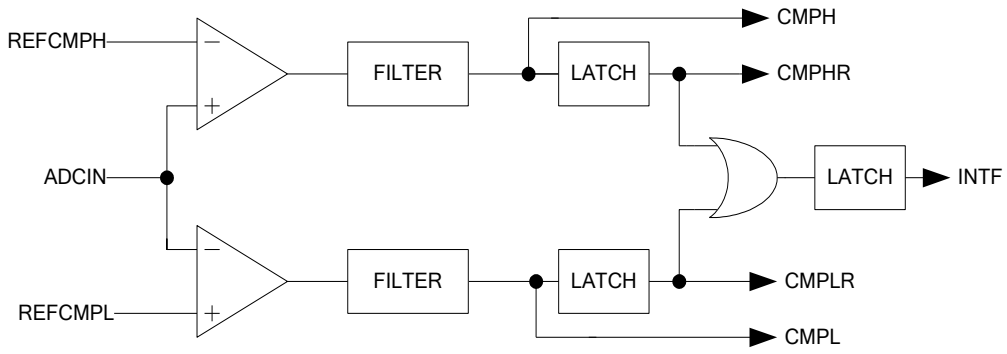
PADCDATA0 (ADC Conversion Result of Trigger 0 by ITCMP0)

BITS	NAME	RW	DEF	DESCRIPTION
31-1	-	-	-	Reserved
15	NEW	RO	0	This bit is set to 1 by hardware indicating ADC0[11-0] contains new conversion results. This bit is self cleared after this register is read.
14	DAOVR	RO	0	This bit is set to 1 by hardware indicating that there was overrun of the conversion result, meaning old conversion data is overwritten by new conversion data before the old data was read out by CPU. This bit is self cleared after this register is read.
12-11	-	-	-	Reserved.
11-0	ADCZ[11-0]	RO	0	Contains the ADC conversion result of Trigger 0.

PADCDATA1 (ADC Conversion Result of Trigger 1 by ITCMP1)
PADCDATA2 (ADC Conversion Result of Trigger 2 by ITCMP2)
PADCDATA3 (ADC Conversion Result of Trigger 3 by ITCMP3)
PADCDATA4 (ADC Conversion Result of Trigger 4 by ITCMP4)
PADCDATA5 (ADC Conversion Result of Trigger 5 by ITCMP5)
PADCDATA6 (ADC Conversion Result of Trigger 6 by SITCMP0)
PADCDATA7 (ADC Conversion Result of Trigger 7 by SITCMP1)

6.5 Overload Window Comparators

Each ADC channel is also connected to a pair of analog comparators for detection of overload condition. The comparator pair detects two thresholds, REFCMPH and REFCMPL. There are two sets of REFCMPH and REFCMPL that can be used for each pair of window comparators. Because the ADC input voltage is centered at 1V to 3V, the compare level of REFCMPH and REFCMPL are programmable from 0V to 3V. If the input voltage exceeds the range defined by REFCMPH and REFCMPL, the output of the comparator is asserted. The output of the comparator can be further processed by time filtering, polarity, and used for overload condition in the protection logic of the Motor Controller, and can also be used to generate interrupt. The functional circuit of the window comparator is shown as following.



The immediate comparator outputs are available at CMPH and CMPL. The latched comparator outputs are also available as CMPHR and CMPLR, and together they are used to generate the latched interrupt flag.

The output of the comparator can be used for generating interrupt. It can also be used to trigger overload and emergency conditions of the motor PWM. Channel A, B, and C are dedicated for overload conditions for PWM channel A, B and C. For Motor emergency condition, the configuration is set by Motor Protection logic along with the comparator channel setting. Any or more than one comparator channel can be used for emergency conditions. It is also possible to use any or more than one comparator channel for generating PFC emergency. When PFC emergency occurs, the hardware will force the PWM channel D to be Hi-Z state.

CREFCFG (Window Analog Reference Configuration Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31-14	REFCMPH1 [7-0]	RW	FF	Reference Set 1 REFCMPH1 level setting FF is 3.0V and 00 is 0V
23-16	REFCMPL1 [7-0]	RW	00	Reference Set 1 REFCMPL1 level setting FF is 3.0V and 00 is 0V
15-8	REFCMPH0 [7-0]	RW	FF	Reference Set 0 REFCMPH0 level setting FF is 3.0V and 00 is 0V
7-0	REFCMPL0 [7-0]	RW	00	Reference Set 0 REFCMPL0 level setting FF is 3.0V and 00 is 0V

CMPCHA (Window Analog Comparator Channel A Configuration and STATUS Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-21	-	-	-	Reserved
20-16	OTF[3-0]	RW	0000	Output time filter setting. OTF[3-0] determines the minimum pulse width of the comparator output for qualifying valid condition. OTF[3-0] is based on ADC clock period. When OTF[3-0]=0, no minimum pulse width is set. When OTF[3-0] >=0, the minimum pulse width is determined by OTF[3-0]*ADCCLK.
15	CMPEN	RW	0	CMPEN=1 will enable the Channel A comparator. CMPEN=0 disables the comparator and force its output to be 0.

BITS	NAME	RW	DEF	DESCRIPTION
14-12	-	-	-	Reserved.
11	PEMGEN	RW	0	PEMGEN=1 will use channel A result to reflect the PFC EMG condition. Thus if Channel A output is 1, it will force PFC PWM D output to be Hi-Z.
10	MEMGEN	RW	0	MEMGEN=1 will use channel A result to reflect the Motor EMG condition. It is gated by EMGSEL control in PRCTCFG register.
9	REFSEL	RW	0	REFSEL=0 will select the Reference Set 0 and REFSEL=1 selects the Reference Set 1.
8	INTEN	RW	0	INTEN=1 enables the channel A result to generate an interrupt.
7	WEN	WO	0	If this bit is 1 when writing, only bit[6-0] are written.
6	-	-	-	Reserved.
5	INTF	RW	0	Latched A Channel Comparator Interrupt Flag. Must be cleared by software by writing 0.
3	CMPHR	RW	0	Latched-1 A Channel REFCMPH Comparator Output. Must be cleared by software by writing 0.
2	CMPLR	RW	0	Latched-1 A Channel REFCMPL Comparator Output. Must be cleared by software by writing 0.
1	CMPH	RO	0	A Channel REFCMPH Comparator Outputs. This reflects the immediate comparator results.
0	CMPL	RO	0	A Channel REFCMPL Comparator Outputs. This reflects the immediate comparator results.

CMPCHB (Window Analog Comparator Channel B Configuration and STATUS Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-21	-	-	-	Reserved
20-16	OTF[3-0]	RW	0000	Output time filter setting. OTF[3-0] determines the minimum pulse width of the comparator output for qualifying valid condition. OTF[3-0] is based on ADC clock period. When OTF[3-0]=0, no minimum pulse width is set. When OTF[3-0] >=0, the minimum pulse width is determined by OTF[3-0]*ADCCLK.
15	CMPEN	RW	0	CMPEN=1 will enable the Channel B comparator. CMPEN=0 disables the comparator and force its output to be 0.
14-12	-	-	-	Reserved.
11	PEMGEN	RW	0	PEMGEN=1 will use channel B result to reflect the PFC EMG condition. Thus if Channel B output is 1, it will force PFC PWM D output to be Hi-Z.
10	MEMGEN	RW	0	MEMGEN=1 will use channel B result to reflect the Motor EMG condition. It is gated by EMGSEL control in PRCTCFG register.
9	REFSEL	RW	0	REFSEL=0 will select the Reference Set 0 and REFSEL=1 select the Reference Set 1.
8	INTEN	RW	0	INTEN=1 enables the channel B result to generate an interrupt.
7	WEN	WO	0	If this bit is 1 when writing, only bit[6-0] are written.
6	-	-	-	Reserved.
5	INTF	RW	0	Latched B Channel Comparator Interrupt Flag. Must be cleared by software by writing 0.
3	CMPHR	RW	0	Latched-1 B Channel REFCMPH Comparator Output. Must be cleared by software by writing 0.
2	CMPLR	RW	0	Latched-1 B Channel REFCMPL Comparator Output. Must be cleared

BITS	NAME	RW	DEF	DESCRIPTION
				by software by writing 0.
1	CMPH	RO	0	B Channel REFCMPH Comparator Outputs. This reflects the immediate comparator results.
0	CMPL	RO	0	B Channel REFCMPL Comparator Outputs. This reflects the immediate comparator results.

CMPCHC (Window Analog Comparator Channel C Configuration and STATUS Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-21	-	-	-	Reserved
20-16	OTF[3-0]	RW	0000	Output time filter setting. OTF[3-0] determines the minimum pulse width of the comparator output for qualifying valid condition. OTF[3-0] is based on ADC clock period. When OTF[3-0]=0, no minimum pulse width is set. When OTF[3-0] >=0, the minimum pulse width is determined by OTF[3-0]*ADCCLK.
15	CMPEN	RW	0	CMPEN=1 will enable the Channel C comparator. CMPEN=0 disables the comparator and force its output to be 0.
14-12	-	-	-	Reserved.
11	PEMGEN	RW	0	PEMGEN=1 will use channel C result to reflect the PFC EMG condition. Thus if Channel C output is 1, it will force PFC PWM output to be Hi-Z.
10	MEMGEN	RW	0	MEMGEN=1 will use channel C result to reflect the Motor EMG condition. It is gated by EMGSEL control in PRCTCFG register.
9	REFSEL	RW	0	REFSEL=0 will select the Reference Set 0 and REFSEL=1 select the Reference Set 1.
8	INTEN	RW	0	INTEN=1 enables the channel C result to generate an interrupt.
7	WEN	WO	0	If this bit is 1 when writing, only bit[6-0] are written.
6	-	-	-	Reserved.
5	INTF	RW	0	Latched C Channel Comparator Interrupt Flag. Must be cleared by software by writing 0.
3	CMPHR	RW	0	Latched-1 C Channel REFCMPH Comparator Output. Must be cleared by software by writing 0.
2	CMPLR	RW	0	Latched-1 C Channel REFCMPL Comparator Output. Must be cleared by software by writing 0.
1	CMPH	RO	0	C Channel REFCMPH Comparator Outputs. This reflects the immediate comparator results.
0	CMPL	RO	0	C Channel REFCMPL Comparator Outputs. This reflects the immediate comparator results.

CMPCHD (Window Analog Comparator Channel D Configuration and STATUS Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-21	-	-	-	Reserved
20-16	OTF[3-0]	RW	0000	Output time filter setting. OTF[3-0] determines the minimum pulse width of the comparator output for qualifying valid condition. OTF[3-0] is based on ADC clock period. When OTF[3-0]=0, no minimum pulse width is set. When OTF[3-0] >=0, the minimum pulse width is determined by OTF[3-0]*ADCCLK.
15	CMPEN	RW	0	CMPEN=1 will enable the Channel D comparator. CMPEN=0 disables the comparator and force its output to be 0.
14-12	-	-	-	Reserved.

11	PEMGEN	RW	0	PEMGEN=1 will use channel D result to reflect the PFC EMG condition. Thus if Channel D output is 1, it will force PFC PWM D output to be Hi-Z.
10	MEMGEN	RW	0	MEMGEN=1 will use channel D result to reflect the Motor EMG condition. It is gated by EMGSEL control in PRCTCFG register.
9	REFSEL	RW	0	REFSEL=0 will select the Reference Set 0 and REFSEL=1 select the Reference Set 1.
8	INTEN	RW	0	INTEN=1 enables the channel D result to generate an interrupt.
7	WEN	WO	0	If this bit is 1 when writing, only bit[6-0] are written.
6	-	-	-	Reserved.
5	INTF	RW	0	Latched D Channel Comparator Interrupt Flag. Must be cleared by software by writing 0.
3	CMPHR	RW	0	Latched-1 D Channel REFCMPH Comparator Output. Must be cleared by software by writing 0.
2	CMPLR	RW	0	Latched-1 D Channel REFCMPL Comparator Output. Must be cleared by software by writing 0.
1	CMPH	RO	0	D Channel REFCMPH Comparator Outputs. This reflects the immediate comparator results.
0	CMPL	RO	0	D Channel REFCMPL Comparator Outputs. This reflects the immediate comparator results.

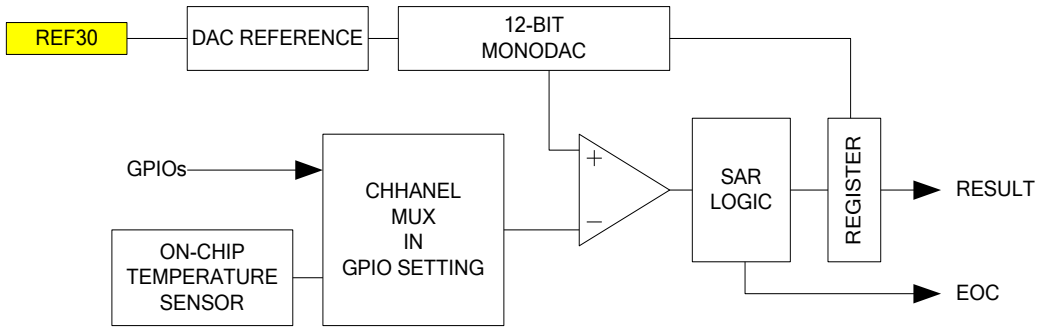
CMPCHE (Window Analog Comparator Channel E Configuration and STATUS Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-21	-	-	-	Reserved
20-16	OTF[3-0]	RW	0000	Output time filter setting. OTF[3-0] determines the minimum pulse width of the comparator output for qualifying valid condition. OTF[3-0] is based on ADC clock period. When OTF[3-0]=0, no minimum pulse width is set. When OTF[3-0] >=0, the minimum pulse width is determined by OTF[3-0]*ADCCLK.
15	CMPEN	RW	0	CMPEN=1 will enable the Channel E comparator. CMPEN=0 disables the comparator and force its output to be 0.
14-12	-	-	-	Reserved.
11	PEMGEN	RW	0	PEMGEN=1 will use channel E result to reflect the PFC EMG condition. Thus if Channel F output is 1, it will force PFC PWM output to be Hi-Z.
10	MEMGEN	RW	0	MEMGEN=1 will use channel E result to reflect the Motor EMG condition. It is gated by EMGSEL control in PRCTCFG register.
9	REFSEL	RW	0	REFSEL=0 will select the Reference Set 0 and REFSEL=1 select the Reference Set 1.
8	INTEN	RW	0	INTEN=1 enables the channel E result to generate an interrupt.
7	WEN	WO	0	If this bit is 1 when writing, only bit[6-0] are written.
6	-	-	-	Reserved.
5	INTF	RW	0	Latched E Channel Comparator Interrupt Flag. Must be cleared by software by writing 0.
3	CMPHR	RW	0	Latched-1 E Channel REFCMPH Comparator Output. Must be cleared by software by writing 0.
2	CMPLR	RW	0	Latched-1 E Channel REFCMPL Comparator Output. Must be cleared by software by writing 0.
1	CMPH	RO	0	E Channel REFCMPH Comparator Outputs. This reflects the immediate comparator results.

BITS	NAME	RW	DEF	DESCRIPTION
0	CMPL	RO	0	E Channel REFCMPL Comparator Outputs. This reflects the immediate comparator results.

7. SAR ADC

There is also a 12-Bit SAR ADC that can be used for other general purpose and its inputs are multiplexed with GPIO pins. The ADC has inherent monotonic characteristics. The ADC clock is programmable and set by the ADC clock scalar. The maximum ADC clock is 4MHz and each conversion takes 16 cycles thus the minimum conversion time is 4 usec. The reference of SAR ADC is REF30 and 0V. Thus the full-scale input range is thus 3.0V. When enabled, the ADC consumes about 3mA of current. The functional block diagram of SAR ADC is shown in the following figure.



The SAR ADC only supports software trigger and when the conversion is ready, EOC is set to 1 by hardware. The ADC result can be read by CPU either using polling method or interrupt method. If ADC interrupt is enabled. The ADC macro is a single channel ADC with its input connect to a single wire bus connected to all GPIO ANIN terminals. Therefore, the channel multiplexing is done by enable the ANEN control in the GPIO configuration registers, and only one of them should be enabled. The channel selection is done at the pin multiplexing. Only the one selected pin with appropriate ANEN should be on. The SARADC can also be connected to internal temperature sensors to provide thermal protection. There are two types of internal temperature sensors. One is a diode connected PNP which has negative temperature coefficient with its forward voltage. One is a band-gap reference which has positive temperature coefficient and a fixed slope. Either temperature sensor can provide +/-3 degree C accuracy after calibration.

The SARADC has self calibration capability. Three steps of calibrations should be performed in sequence of A-B-C and it is recommended that calibration to be done after power up and ADC enabling.

SADCCFG (SAR ADC Configuration and Status Register) TD

BITS	NAME	RW	DEF	DESCRIPTION
31	ADCEN	RW	0	ADC Enable 0 – Disable 1 – Enable. There is 5msec initialization time after enable.
30-29	-	-	-	Reserved
28	CALC	RW	0	Calibration C Set this bit to 1 will initiate a calibration of ADC stage C. Read to indicate if calibration step has been completed or not. 1 indicates completion. 0 means not completed.
27	CALB	RW	0	Calibration B Set this bit to 1 will initiate a calibration of ADC stage B. Read to indicate if calibration step has been completed or not. 1 indicates completion. 0 means not completed.
26	CALA	RW	0	Calibration A Set this bit to 1 will initiate a calibration of ADC stage A. Read to indicate if calibration step has been completed or not. 1 indicates completion. 0 means not completed.
25	REFPSEL	RW	0	REFPS Select Set this bit to 1 will disable the internal REFPS generator and use

BITS	NAME	RW	DEF	DESCRIPTION
				external REFPS input for SAR ADC. (Not Used)
24-16	REFPS[7-0]	RW	0x00	REFPS Setting This set the positive full scale of the SAR ADC. (Not Used)
15-8	ADCCKS[7-0]	RW	0x00	ADC Clock Divider. The ADC clock is SYSCLK/2/ADCCKS[7-0]
7	TEMPS1EN	RW	0	Set this bit to 1 will enable the type-A internal temperature sensor. This is a diode-connected vertical PNP. Thus it exhibits a negative temperature coefficient.
6	TEMPS2EN	RW	0	Set this bit to 1 will enable the type-B internal temperature sensor. This is a voltage generated by a band-gap reference. Thus it exhibits a positive temperature coefficient.
5	TEMPS	RW	0	Set this bit to1 connect the internal temperature sensor. Set this bit to 0 to connect the ADC input to GPIO pins.
4	INTEN	RW	0	ADC Interrupt Enable. When enabled, EOC will cause an interrupt 0 – Disable Interrupt 1 – Enable Interrupt
3	-	-	-	Reserved
2	WE21	WO	0	Controls the modification of bit 1 and 0. When this bit is 1 when writing only bit 1 and bit 0 are affected and is not TD protected.
1	EOC	RW	0	Indicate the end of conversion and is set by the ADC hardware. It must be cleared by software. If EOC is not cleared, the next conversion will not be started. After interrupt, EOC also server as interrupt status and must be cleared.
0	STARTC BUSY	RW	0	Write 1 to this register will initiate a software trigger of ADC. When read, this bit indicates whether ADC is in busy in the process of conversion. 1 is busy and 0 is non busy.

SADCDATA (SAR ADC Conversion Result)

BITS	NAME	RW	DEF	DESCRIPTION
31-12	-	-	-	Reserved
11-0	ADC0[11-0]	RO	0	Contains the conversion result of ADC.

8. EUART0/EUART1/EUART2

CS6257 include three enhanced UART controllers. Each EUART controller has independent baud rate generator, and two 7-Bytes FIFO for receive and transmit paths. The additions of FIFO significantly reduce the CPU loading. The depth of FIFO can be programmed for generating interrupt for optimal CPU performance. The EUART also has LIN capability extension. The extension includes the auto baud rate synchronization which allows up to 10% variation of clock frequency. The LIN extension also includes hardware for constructing LIN frame structure with minimum software resources.

SCONFG (EUART Configuration Register) TB

BITS	NAME	RW	DEF	DESCRIPTION
31	EUARTEN	RW	0	EUART Enable Control Set EUARTEN=1 to enable EUART operation If EUARTEN=0, the EUART operation is suspended. All flags and the pointers of TFIFO and RFIFO are cleared. The state machine will be put in idle mode.
30	SB	RW	0	Stop Bit SB = 0 configures one stop bit. SB=1 configures two stop bits.
29-28	WLS[1-0]	RW	10	The number of bits of a data byte. This does not include the parity bit when parity is enabled. 00 5 bits 01 6 bits 10 7 bits 11 8 bits
27	OP	RW	0	Odd/Even Parity OP=0 uses even parity OP=1 uses odd parity
26	PE	RW	0	Parity Enable PE=0 disable parity generation and checking PE=1 enable parity generation and checking
25	PS	RW	0	Parity Force PS=1 will force the parity bit as 1 regardless of parity generation.
24	FBREAK	RW	0	Force Break Condition Setting this bit to 1 will force break condition on the UART interface by holding UART output at low until this bit is cleared. For normal operation, this bit should be cleared.
23	LINEN	RW	0	LIN Extension Enable Set to 1 to enable Lin extension for break/sync detection. EUARTEN must be 1 for this bit to be meaningful.
22	LINMODE	RW	0	LIN Operation Mode LINMODE=1 will configure the LIN extension as Master LINMODE=1 will configure the LIN extension as Slave This bit can be modified only when LINEN=0.
21	AUTOSYNC	RW	0	Auto Baud Rate Sync Set AUTOSYNC=1 will enable the LIN controller hardware to update the baud rate register from synchronization result after SYNC field. Set AUTOSYNC=0 to disable this feature and BR[15-0] will keep the baud rate constant. AUTOSYNC should be set to 1 only in LIN slave mode.
20-16	LBDL[4-0]			LIN Break Length

BITS	NAME	RW	DEF	DESCRIPTION
				This is used to program the length of dominant bits for BREAK. The break time is (LBDL[4-0] + 1)*BT.
15	FCLEAR	WO		Set this bit to 1 will reset the pointers for both receive and transmit FIFO.
14	CMDEN	WO		Enable LINSBK command bit. This bit is write-only. When this bit is 1, only bit[13] is affected, and not protected by TC.
13	LINSBK	WO		Send LIN BREAK This bit is meaningful only if LINEN=1 and LINMODE=1 as LIN master. When this bit is set to 1, the LIN Master will initiate a LIN BREAK on the bus which is composed of a bit sequence of 13+LBDL[2-0] consecutive dominant bits and 1 recessive bit on the bus. This bit is self cleared when the sequence is completed. Upon completion, a SBKI interrupt is generated if enabled. This command should be set only in LIN master mode. If there is pending data in TFIFO, the data will be transmitted after the BREAK condition is completed. This bit is write-only and is gated by CMDEN and writing 0 into this bit is ignored.
12	SINTEN	RW	0	This is the global interrupt enable for EUART. This bit must be set to 1 to enable individual interrupt.
11	IESTIMER	RW	0	Enable SFITIMER Expiration Interrupt
10	IESBK	RW	0	Enable Send Break Completion Interrupt
9	IERSC	RW	0	Enable Receive Synchronization Completion Interrupt
8	IETFOV	RW	0	Enable Transmit FIFO Overflow Interrupt
7	IETFFULL	RW	0	Enable Transmit FIFO Full Interrupt
6	IETFEMPTY	RW	0	Enable Transmit FIFO Empty Interrupt
5	IETFRDY	RW	0	Enable Transmit FIFO Ready Interrupt
4	IERFOF	RW	0	Enable Receive FIFO Overflow Interrupt
3	IERFUR	RW	0	Enable Receive FIFO Under-run Interrupt
2	IERFFULL	RW	0	Enable Receive Full Interrupt
1	IERFEMPTY	RW	0	Enable Receive FIFO Empty Interrupt
0	IERFRDY	RW	0	Enable Receive FIFO Ready Interrupt

SBAUD (EUART Baud Rate Register) TB

BITS	NAME	RW	DEF	DESCRIPTION
32-16	SBR[15-0]	RO	0	Synchronized Baud Rate This is read only and contains the result of synchronization baud rate when LIN extension is enabled. In general, reading SBR[15-0] and the value should be written back to BR[15-0]. The update can be configured automatically if AUTOSYNC=1, and the update will occur for every LIN frame.
15-0	BR[15-0]	RW	0xFFFF	Baud Rate Scaling Factor BAUDRATE = SYSCLK/16/(BR[15-0]). This is the actual EUART baud rate. And if AUTOSYNC=1, this is updated every LIN frame through synchronization result.

SBUF (EUART Data Register)

BITS	NAME	RW	DEF	DESCRIPTION
31-9	-	-	-	Reserved.
8	PERR	RO	0	Parity Error This reflects the parity error of the current available received byte. PERR=1 means parity error. This bit is read only.
7-0	SBUF[7-0]	RW	0x00	FIFO Data Buffer When written, the data will be written into the transmit FIFO. When read, read out the receive FIFO.

SSTAT (EUART Status Register)

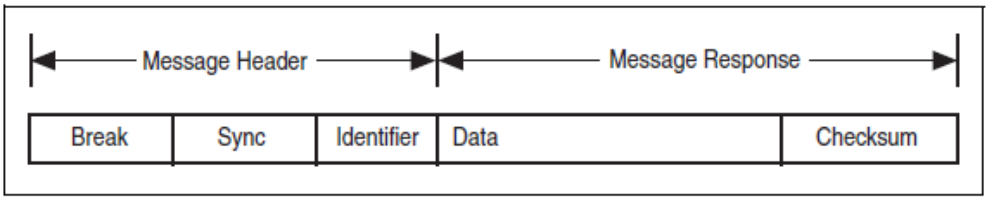
BITS	NAME	RW	DEF	DESCRIPTION
31	LINSTAT	RO	0	LIN Bus State LINSTAT=0 indicates DOMINANT state LINSTAT=1 indicates RECESSIVE state
30	FERR	RO	0	Framing Error This bit is set to 1 by hardware to indicate framing error has occurred during the received byte. Framing error is defined as missing STOP bit of the reception of one or more bytes (i.e. a mark of 1 was not detected when a STOP bit should have occurred). If a framing error occurs, the data byte that causing error will be dropped. Since the STOP bit (MARK) is not detected, the start bit of the next byte can not be recognized. The next reception will resume only after a mark to space transition which indicates the START bit. When Frame Error occurs, it usually means the baud rate is not correct or accurate.
29-23	-	-	-	Reserved
22-20	TFLVL[2-0]	RO	0	Transmit FIFO Current Level This reflect current receive FIFO byte count
19	-	-	-	Reserved
18-16	RFLVL[2-0]	RO	0	Receive FIFO Current Level This reflect current receive FIFO byte count
15-12	-	-	-	Reserved
11	STIMERF	RW0	0	SFITMER Expiration Flag
10	SBKF	RW0	0	Send Break Complete
9	RSI	RW0	0	Receive Synchronization Complete Flag This bit is set to 1 by hardware after a valid SYNC byte has been received following a LIN break.
8	TFOF	RW0	0	Transmit FIFO Overflow Flag
7	TFFULL	RW0	0	Transmit FIFO Full Flag
6	TFEMPTY	RW0	0	Transmit FIFO Empty Flag
5	TFRDY	RW0	0	Transmit FIFO Ready Flag
4	RFOF	RW0	0	Receive FIFO Overflow Flag
3	RFUR	RW0	0	Receive FIFO Under-run Flag
2	RFFULL	RW0	0	Receive FIFO Full Flag
1	RFEMPTY	RW0	0	Receive FIFO Empty Flag
0	RFRDY	RW0	0	Receive FIFO Ready Flag

SFITIMER (EUART Frame Time and Idle Time Timer) TB

BITS	NAME	RW	DEF	DESCRIPTION
31-28	TFTH[3-0]	RW	0000	Transmit FIFO Threshold Setting This set the threshold for generating TFIFO ready interrupt. When TFTH[3-0]=0000, the transmit FIFO is disabled.
27-24	RFTH[3-0]	RW	0000	Receive FIFO Threshold Setting This set the threshold for generating RFIFO ready interrupt. When RFTH[3-0]=0000, the receive FIFO is disabled.
23-21	-	-	-	Reserved.
20-18	RSPDLY[1-0]	RW	00	Response Space. This set the Response Space after the Identifier is sent. This delay is only applicable for LIN Master mode. This insert a delay window after ID field is transmitted. So if the Master has a pending transmission, it will wait until this window has elapsed. In other word, it does not necessary mean the 3rd byte transmission of the master. 00 – 0 01 – 8BT 10 – 12BT 11 – 16BT
17-16	IBDLY[1-0]	RW	00	Transmit Inter-Byte Delay. This set the delay between each byte transmission and applicable to all EUART transmission. This delay is inserted between each data byte transmission. 00 – 0 01 – 1BT 10 – 2BT 11 – 3BT
15-0	SFITIMER[15-0]	RW	0	The Frame Time Timer and Idle Time Timer The value is used to compare with an internal counter to generate an interrupt.

This timer has dual purposes. When LIN is enabled and configured as LIN Master, this timer can be used for indexing Frame Time. As Frame Time Timer, an internal counter is cleared after a “Send Break Command” is initiated. The counter increments every BT (1/BAUDRATE) and generates an interrupt when it reaches SFITIMER[15-0]. When not in LIN Master mode, the counter is cleared whenever there is a RX signal transition, and increments every 8*BT. And when the counter reaches SFITIMER[15-0], it generates an interrupt. Therefore, when not in LIN Master mode, this timer can be used to detect bus idle time.

LIN bus protocol is based on frame. Each frame is partitioned into several parts as shown in the following.



For master to initiate a frame, the software needs to follow the following procedure.

1. Initiate a SBK command. (SW need to check if the bus is in idle state, and there is no pending transmit datat).
2. Write “55” into TFIFO.
3. Write “PID” into TFIFO.
4. Wait for SBK complete interrupt and then write following transmit data. (This is optional).

9. I²C Master Controller (I2CM0)

The I2C master controller provides the interface to I²C slave devices. It can be programmed to operate with arbitration and clock synchronization to allow it to operate in multi-master configurations. The master uses SCL and SDA pins. The controller contains a built-in 12-bit timer to allow various I²C bus speed.

I2CMCFG (I²C Master Configuration) TB

BITS	NAME	RW	DEF	DESCRIPTION
31	I2CMEN	RW	0	I²C Master Enable. I2CMEN=0 will disable the I²C master.
30	I2CMINTEN	RW	0	I²C Master Interrupt Enable This bit should be set to 1 to allow normal operations of I2CM master. An interrupt is generated when command bits in this register are set, and the command sequence is completed.
29	-	-	-	Reserved
28	INFILEN	RW	0	INFILEN is input pulse filtering control. When IFILEN is set, pulses shorter than SYSCLK/(I2CMCS[3-0]+1) on inputs of SDA and SCL are filtered out.
27-24	I2CMCS[3-0]	RW	0000	I²C Master Controller Clock This is used to scale down the operating clock of the I²C Master Controller to save power consumption when system clock is high. The I²C master operates under SYSCLK/(I2CMCS[3-0]+1)
23-16	I2CMTP[7-0]	RW	0x000	I2C Master Clock Setting This sets the period time of I²C bus clock – SCL. The SCL frequency is SYSCLK/(I2CMCS[3-0]+1)/(1+ I2CMTP[7-0])
15	-	-	-	Reserved.
14	BUSBUSY	RO		This bit indicates that the external I²C bus is busy and access to the bus is not possible. This bit is set/reset by START and STOP conditions.
13	IDLE	RO	0	This bit indicates that I²C master is in the IDLE mode.
12	ARBLOST	RO	0	This bit indicates that the last operation I²C master controller lost the bus arbitration
11	DATAERR	RO	0	This bit indicates that the last operation transmitted data was not acknowledged.
10	ADDRERR	RO	0	This bit indicates that the last operation slave address transmitted was not acknowledged
9	ERROR	RO	0	This bit indicates that error occurred in the last operations. The errors include slave address was not acknowledged, or transmitted data was not acknowledged, or the master controller lost arbitration.
8	BUSY	RO	0	This bit indicates that I²C master is receiving or transmitting data, and other status bits are not valid.
7	CMDEN	WO	0	This is command enable control. If bit[7] is set to 1 during writing, then only bit[3-0] in this register are affected. When this bit is 1, the operation is not protected by TC.
6-5	-	-	-	Reserved
4	HS	RW	0	Switching to high speed mode
3	ACK	RW	0	Automatically send ACK bit after each byte transfer
2	STOP	RW	0	Control the STOP condition
1	START	RW	0	Control the START condition
0	RUN	RW	0	Initiate the transfer sequence

The Command bits are described in details. The START bit is used to generate START, or REPEAT START protocol. The STOP bit determines if the cycle will stop at the end of the data cycle or continue on to a burst. To generate a single read cycle, SA is written with the desired address, RS is set to 1, and I2CMCR is written with ACK=0, STOP=1, START=1, RUN=1 to perform the operation and then STOP. When the operation is completed (or aborted due to errors), I^2C master generates an interrupt. The ACK bit must be set normally 1. This causes the controller to send an ACK automatically after each byte transaction. The ACK bit must be reset to 0 when the master is operating in receive mode and do not intend to receive further data from the slave device.

HS	RS	ACK	STOP	START	RUN	OPERATIONS
Master IDLE Mode						
0	0	-	0	1	1	START condition followed by SEND. Master remains in TRANSMITTER mode
0	0	-	1	1	1	START condition followed by SEND and STOP
0	1	0	0	1	1	START condition followed by RECEICE operation with negative ACK. Master remains in RECEICER mode
0	1	0	1	1	1	START condition followed by RECEIVE and STOP
0	1	1	0	1	1	START condition followed by RECEIVE. Master remains in RECEIVER mode
0	1	1	1	1	1	Illegal command
1	0	0	0	0	1	Master Code sending and switching to HS mode
Master TRASMITTER Mode						
0	-	-	0	0	1	SEND operation. Mater remains in TRANSMITTER mode
0	-	-	1	0	0	STOP condition
0	-	-	1	0	1	SEND followed by STOP condition
0	0	-	0	1	1	Repeated START condition followed by SEND. Master remains in TRANSMITTER mode
0	1	-	1	1	1	Repeated START condition followed by SEND and STOP condition
0	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with negative ACK. Master remains in TRANSMITTER mode
0	1	0	1	1	1	Repeated START condition followed by SEND and STOP condition.
0	1	1	0	1	1	Repeated START condition followed by RECEIVE. Master remains in RECEIVER mode.
0	1	1	1	1	1	Illegal command
Master RECEIVER Mode						
0	-	0	0	0	1	RECEIVE operation with negative ACK. Mater remains in RECEIVE mode
0	-	-	1	0	0	STOP condition
0	-	0	1	0	1	RECEIVE followed by STOP condition
0	-	1	0	0	1	RECEIVE operation. Mater remains in RECEIVER mode
0	-	1	1	0	1	Illegal command

HS	RS	ACK	STOP	START	RUN	OPERATIONS
0	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with negative ACK. Master remains in RECEIVER mode
0	1	0	1	1	1	Repeated START condition followed by RECEIVE and STOP conditions
0	1	0	1	1	1	Repeated START condition followed by RECEIVE. Master remains in RECEIVER mode
0	0	-	0	1	1	Repeated START condition followed by SEND. Master remains in TRANSMITTER mode.
0	0	-	1	1	1	Repeated START condition followed by SEND and STOP conditions.

All other control bits combinations not mentioned in the above tables are NOP. In Master RECEIVER mode, STOP condition should be generated only after data negative ACK executed by Master or address negative ACK executed by slave. Negative ACK here means SDA is pulled low during the acknowledge clock pulse.

I2CMSA0 (I^2C Master Slave Address)

BITS	NAME	RW	DEF	DESCRIPTION
31-8	-	-	-	Reserved.
7-1	SA[6-0]	RW	000000	SA[6-0] defines the slave address to be used.
0	RS	RW	0	RS bit determines if the next operation will be a RECEIVE (1) or SEND (0).

I2CMBUF0 I^2C Master Data Buffer Register

BITS	NAME	RW	DEF	DESCRIPTION
31-8	-	-	-	Reserved.
7-0	I2CMBUF[7-0]	RW	0	I2CMBUF functions as a transmit data register when written and as a receive data register when read

When written, I2CMBUF[7-0] will be sent on the bus by the next SEND or BURST SEND operations. I2CMBUF[7] is sent first. When read, I2CMBUF[7-0] contains the 8-bit data that has been received the bus due to the last RECEIVE or BURST RECEIVE operations.

10. I²C Slave Controller (I2CS0)

The address of the slave is set by I2CSADRx register. The MSB in I2CSADDR is the enable bit control for the I²C slave controller. I2CSADR[6-0] specifies the actual slave address.

In receive mode, the controller detects a valid matching address and issues an ADDRMI interrupt. At the same time, the data bit on SDA line is shifted into receive buffer. The RCBI interrupt is generated whenever a complete byte is received and is ready to be read from I2CSDAT. If for any reason, the software does not respond to RCBI interrupt in time (i.e. RCBI is not cleared), and a new byte is received, the controller will either force an NACK response on I²C (if CLKSTREN bit is not set) or by pulling and holding SDA low (if CLKSTREN bit is set) to stretch the SCL low duration to force the master into a wait state. In clock stretching mode, SCL is released when the software responds to RCBI interrupt and cleared RCBI flag.

In transmit mode, the controller detects a valid matching address and issue an ADDRMI interrupt. At the same time, the data preloaded in the transmit data register through I2CSDAT is transferred to the transmit shift register and is serially shifted out onto SDA line. When this is occurring, the controller generates a TXBI interrupt to inform the software that a new byte can be written into I2CSDAT. When the shift register is empty and ready for the next transmit, the slave controller checks if new byte is been written to the I2CSDAT. If TXBI is still not cleared indicating no new data is available, the slave controller will hold SCL line low to stretch the current clock cycle if CLKSTREN is set. If clock stretching is not enabled, the slave controller will take the old byte into the shift register and reply with NACK, and thus will cause data corruption. On the other hand, if the master returns the NACK after the byte transfer, this indicates the end of data to the I²C slave. In this case, the I²C slave will release the data line to allow the master to generate a STOP or repeated START condition.

The I²C slave controller also implements the input noise filter. This is enabled by the INFILEN bit in the I2CSCON register. The filter is implemented using digital circuit. When INFILEN is set, the spike under 1/2 SYSCLK period on the input of SDA and SCL lines will be filtered out. If INFILEN is low, no input filtering is done.

I2CSCON0 (I²C Slave Controller Configuration) TB

BITS	NAME	RW	DEF	DESCRIPTION
31	I2CSEN	RW	0	I²C Slave Enable. I2CMEN=0 will disable the I²C master.
30	I2CSRST	RW	0	I²C Slave Reset Bit. Set this bit will cause the Slave Controller to reset all internal state machine. Clear this bit for normal operations. Set this bit will also clear the I2CSADRx (I²C slave address x).
29-28	I2CSCS[2-0]	RW	00	I2CS Clock Scaling The I²C Slave is clocked by SYSCLK/(I2CSCS[2-0]+1). This is for the purpose to reduce the power consumption of the I²C slave. The I²C slave clock rate must be maintained at least 8X of the I²C bit rate.
27-24	HOLDT[2-0]	RW	0000	This four bits define the number of I²C slave clock cycles that SDA to SCL hold time. The I²C specification requires for minimum of 300nsec hold time, so the "$T_{I2CSLAVECLK}$*(HOLDT[2:0]+3) ≧300nsec hold time" equation condition must be met. For example, if I2CS slave clock is 20MHz, then HOLD[2-0] should be set to ≧3.
23	INFILEN	RW	0	INFILEN is input pulse filtering control. When IFILEN is set, pulses shorter than SYSCLK/(I2CSCS[2-0]+1) S on inputs of SDA and SCL are filtered out.
22-16	I2CSA[6-0]	RW	00	I2CS Slave Address
15	EADDRMI	RW	0	ADDRMI interrupt Enable Bit. Set this bit will allow ADDRMI interrupt as the I²C slave interrupt. This interrupt is generated when I²C slave received a matching address.
14	ESTOPI	RW	0	STOPI Interrupt Enable Bit. Set this bit will allow STOPI interrupt as the I²C slave interrupt.

BITS	NAME	RW	DEF	DESCRIPTION
13	ERPSTARTI	RW	0	RPTSTARTI Interrupt Enable Bit. Set this bit will allow RPTSTARTI interrupt as the I²C slave interrupt.
12	ETXBI	RW	0	TXBI Interrupt Enable Bit. Set this bit will allow TXBI interrupt as the I²C slave interrupt.
11	ERCBI	RW	0	RCBI Interrupt Enable Bit. Set this bit will allow RCBI interrupt as the I²C slave interrupt.
10	CLKSTREN	RW	0	Set to enable the clock stretching function of the slave controller. Clock stretching is an optional feature defined in I²C specification. If the clock stretching option is enabled (for slave I²C), the data write to transmit buffer will be shift out only after the occurrence of clock stretch, i.e. even the transmit buffer is written data during the I²C transfer, the data won't be loaded to transmit shift register, the programmer must write same data again to the transmit buffer.
9	XMT	RO	0	This bit is set by the controller when the I²C slave is in transmit operation, and is 0 when the I²C slave controller is in receive operation.
8	FIRSTBIT	RO	0	This bit is set to indicate the data in the data register is the first byte received after address match. This bit is cleared after the first byte of the transaction is read. This bit is generated by slave controller and is read-only.
7	FLAGCLN	WO	0	When this bit is written as 1, only bit[6-4] are affected. And the operation is not protected by TC.
6	ADDRMI	RW	0	Slave Address Match Interrupt Flag. This bit is set when the received address matches the address defined in I2CSADR1. If EADDMI is set, this will generate an interrupt. This bit must be cleared by software.
5	STOPI	RW	0	Stop Condition Interrupt Flag. This bit is set when the slave controller detects a STOP condition on the SCL and SDA lines. This bit must be cleared by software.
4	RPSTARTI	RW	0	Repeat Start Condition Interrupt Flag. This bit is set when the slave controller detects a repeat Start condition on the SCL and SDA lines. This bit must be cleared by software.
3	TXBI	RO	0	Transmit Buffer Interrupt Flag. This bit is set when the slave controller is ready to accept a new byte for transmit. This bit is cleared when new data is written into I2CSBUF register.
2	RCBI	RO	0	Receiver Buffer Interrupt Flag. This bit is set when the slave controller have put a new data in the I2CSDAT and ready for software to read. This bit is cleared after the software read out the I2CSBUF.
1	START	RO	0	Start Condition. This bit is set when the slave controller have detected a Start condition on the SCL and SDA lines. This bit is not very useful as the start of transaction can be indicated by address match interrupt. This bit read-only and is cleared when Stop condition is detected.
0	NACK	RO	0	NACK Condition. This bit is set when the host has responded with NACK in the byte transaction. This bit is only meaningful for slave-transmit operation. Please note if the master returns with NACK on the byte transaction, the slave will not upload new data into the shift register. And the slave will re-transmit the old data again in the next transfer, and this re-transmission will continue if NACK condition is repeated until the transmission is successful with ACK returned. This bit is cleared when a new ACK condition is detected or it can be cleared by software.

I2CSBUF0 (I²C Slave Data Buffer Register)

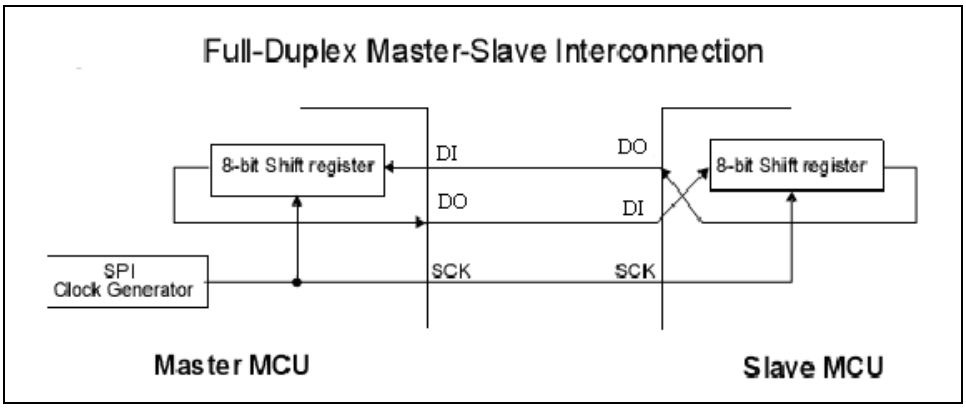
BITS	NAME	RW	DEF	DESCRIPTION
31-8	-	-	-	Reserved.
7-0	I2CSBUF[7-0]	RW	0	I2CSBUF functions as a transmit data register when written and as a receive data register when read

11. SPI Controller

The Serial Peripheral Interface (SPI) is an enhanced synchronous serial hardware which is compatible with Motorola's SPI specifications. There are 15-Byte FIFO for both transmit and receive paths thus can significantly reduce the CPU overhead for handling SPI transfer.

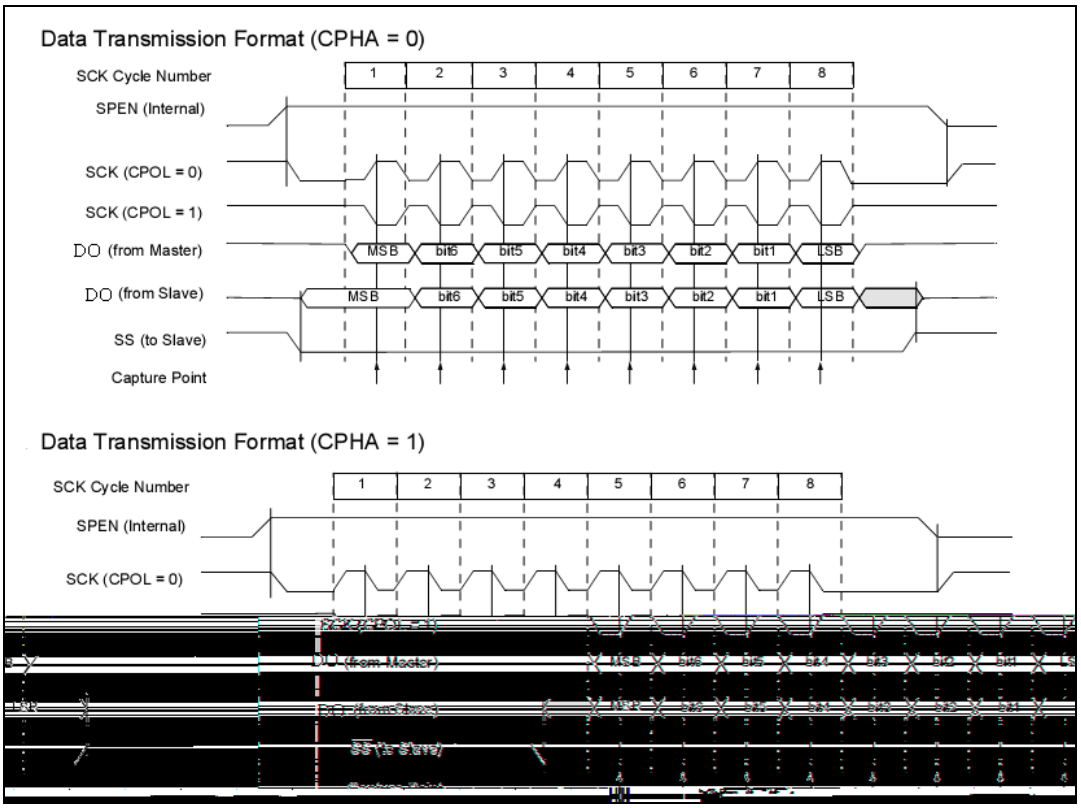
11.1 Operating Modes

Serial Peripheral Interface can be configured either Master or Slave mode. The configuration and initialization of the SPI Module is made through one register (SPCR). During an SPI transmission, data is simultaneously transmitted (shifted out serially) and received (shifted in serially) through SDI and SDO respectively. . A serial clock line (SCK) synchronizes shifting and sampling on the two serial data lines. When the Master device transmits data to the Slave device via one bus line, the Slave device responds by sending data to the Master device via the other line. This implies full-duplex transmission with both data out and data in synchronized with the same clock.



11.2 Transmission Formats

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPCR: the Clock Polarity (CPOL) and the Clock Phase (CPHA). CPOL defines the default SCK line level in idle state. It has no significant effect on the transmission format. CPHA defines the edges on which the input data are sampled and the edges on which the output data are shifted .The clock phase and polarity should be identical for the Master SPI device and the communicating Slave device. The SPI Module should be configured as a Master or Slave before it is enabled (SPEN set). Also, the Master SPI should be configured before the Slave SPI. The maximum frequency of the SCK for an SPI configured as a Slave is the bus clock speed. Before writing to the CPOL and CPHA bits, the SPI should be disabled (SPEN = 1'b0).



11.2.1 Master Mode Operations

Under the Master Mode, if CS is 0, transmit and receive as well as clock logic will be put on suspended state. To initiate a transaction, the software must first set CS to 1 through configuration register. The transmission of the SCK will not start until CS is set to 1. The SCK is tightly coupled with data transmit logic. Although the CS can be changed by software at any time, the output CS will always change only on byte boundaries. Any remaining pending transmit data will result SCK to be outputted. And if there is no pending transmit data, the SCK will not start. As SCK in progress, the receiving logic also receives data and put received data into RFIFO. Since SCK is tied with transmit data, therefore, the number of bytes transmitted and the number of bytes received are exactly equal. In other words, in order to receive data, the software must also transmit data.

In general, in each SPI transaction, the software usually follows the following procedures. Since in typical SPI applications, the transaction is less than 16-Byte length of the FIFO, this can be easily done.

i. Determine the number of total number of bytes in this transaction.
ii. Fill the TFIFO with the intended transmit data and dummy data for receive bytes.
iii. Set CS to 1.

Wait until TFIFO empty interrupt and then set CS to 0 and read out all received data.

11.2.2 Slave Mode Operations

Slave mode operation is relative passive. The configuration allows interrupt to respond to any CS level change. When CS change from 0 to 1 usually means a transaction is started by the master. In response to the CS interrupt, the slave usually can follow the following procedure to complete the transaction. Also note that in slave mode, CS will gate the SCK signal.

i. Set RFIFO threshold according to the number of the command bytes.
ii. In response to RFIFO ready interrupt and interpret the received command from master.
iii. If the master requires the slave to transmit data, then slaves write the data into TFIFO.
iv. If the master requires the slave to receive data, then set RFIFO threshold again. And enable CS interrupt.
v. Upon CS interrupt which means the transaction by master is completed, the slave can read out the data or finish the transaction.

Note that in the above procedure if there is no valid data in the TFIFO, the SDO will be outputted with FF. Alternatively if the slave already knows the coming transaction requires it to send data to master, it can pre-fill the TFIFO with intended data. And the software can just depend the hardware to complete the transaction.

11.3 SPI Registers

SPICFG0 (SPI Controller Configuration) TB

BITS	NAME	RW	DEF	DESCRIPTION
31	SPIEN	RW	0	SPI Controller Enable. SPIEN=0 will disable the SPI Controller for power saving. SPIEN=1 puts the SPI Controller in normal operation.
30	SPIRST	RW	0	SPI Controller Reset Set this bit to 1 will reset the controller's state machine and FIFO pointers to put the controller into initialized state.
29	MODE	RW	0	Master or Slave Mode Select Mode=1 puts the SPI Controller in Master mode Mode=0 puts the SPI Controller in Slave mode
28-26	SPICS[2-0]	RW	00	SPI Controller Clock Scaling The SPI Controller is clocked by SYSCLK/2/(SPICS[2-0]+1). This is for the purpose to reduce the power consumption of the controller. The SPI controller clock rate must be maintained at least 2X of the SPI clock.
25-23	SPIBCR[2-0]	RW	000000	SPI Bus Clock Rate (Master Mode only) 000 – SYSCLK/2/(SPICS[2-0]+1)/1 000 – SYSCLK/2/(SPICS[2-0]+1)/2 000 – SYSCLK/2/(SPICS[2-0]+1)/4 000 – SYSCLK/2/(SPICS[2-0]+1)/8 000 – SYSCLK/2/(SPICS[2-0]+1)/16 000 – SYSCLK/2/(SPICS[2-0]+1)/32 000 – SYSCLK/2/(SPICS[2-0]+1)/64 000 – SYSCLK/2/(SPICS[2-0]+1)/128
22	SCKPOL	RW	0	Idle Clock State (Master Mode only) This bit set the SCK state at idle state. SCKPOL=0 will put SCK HIGH at idle state. SCKPOL=1 will put SCK LOW at idle state.
21	CPHA	RW	0	SCK Clock Phase Select This bit is used to select the SDA sampling phase of SCK.

BITS	NAME	RW	DEF	DESCRIPTION
				CPHA=0 set the SDI input sampling with rising edge of SCK and SDO output sampling at falling edge of SCK. CPHA=1 set the SDI input sampling with falling edge of SCK and SDO output sampling at rising e
20	DIR	RW	0	Transfer Direction Control This bit controls the first bit transfer order. When DIR=0, the data is transferred as LSB first. When DIR=1, the data is transferred as MSB first.
19	-	-	-	Reserved.
18	CLRTFIFO	WO	0	Set this bit to 1 will cause TFIFO pointer be cleared and transmit state machine restarted into idle.
17	CLRRFIFO	WO	0	Set this bit to 1 will cause RFIFO pointer be cleared and receive state machine restarted into idle.
16	WREN	WO	0	If this bit is set to 1, then only BIT[15-0] is affected in writing.
15	CSFEDGEIE	RW	0	CS Falling Edge Transition Interrupt Enable Set this bit to 1 to enable CS falling edge transition interrupt.
14	CSREDGEIE	RW	0	CS Rising Edge Transition Interrupt Enable Set this bit to 1 to enable CS rising edge transition interrupt.
13	TFUDRIE	RW	0	Transmit FIFO Under Run Interrupt Enable Set this bit to 1 to enable TFIFO under run interrupt.
12	TFEMPIE	RW	0	Transmit FIFO Empty Interrupt Enable Set this bit to 1 to enable the TFIFO empty interrupt.
11	TFRDYIE	RW	0	Transmit FIFO Ready Interrupt Enable Set this bit to 1 to enable the TFIFO ready interrupt.
10	RFOVRIE	RW	0	Receive FIFO Overrun Error Interrupt Enable Set this bit to 1 to enable the RFIFO overrun error interrupt.
9	RFFULLIE	RW	0	Receive FIFO Full Interrupt Enable Set this bit to 1 to enable the RFIFO full interrupt.
8	RFRDYIE	RW	0	Receive FIFO Ready Interrupt Enable Set this bit to 1 to enable the RFIFO ready interrupt.
7-4	TFIFOTH [3-0]	RW	0	Transmit FIFO Ready Interrupt Threshold 0000 disable the FIFO.
3-0	RFIFOTH [3-0]	RW	0	Receive FIFO Ready Interrupt Threshold 0000 disables the FIFO.

SPISTAT0 (SPI Controller Configuration)

BITS	NAME	RW	DEF	DESCRIPTION
31-17	-	-	-	Reserved.
16	CS	RW	0	This bit is read-only and only valid in slave mode, and write-only in master mode. In slave mode, it reflects the current CS state. In master mode, it controls the CS output.
15	CSFEDGEF	RW	0	This is the CS falling edge transition Flag. This is set by hardware when either CS changes from 1 to 0. This must be cleared by software.
14	CSREDGEF	RW	0	This is the CS riding edge transition Flag. This is set by hardware when either CS changes from 0 to 1. This must be cleared by software.
13	TFUDRF	RW	0	Transmit FIFO Underrun Error Flag

BITS	NAME	RW	DEF	DESCRIPTION
				This is set by hardware when transmit FIFO has underrun error. This usually occurs in slave mode when transmit FIFO is empty but SCK is received. This must be cleared by software.
12	TFEMPTYF	RW	0	Transmit FIFO Empty Flag This is set by hardware when transmit FIFO pointer is equal to 0000 meaning the transmit FIFO is empty. This must be cleared by software.
11	TFRDYF	RW	0	Transmit FIFO Ready Flag. This is set by hardware when transmit FIFO pointer is equal to the threshold. This must be cleared by software.
10	RFOVRF	RW	0	Receive FIFO Overflow Error Flag This is set by hardware when receive FIFO has overflow error. This must be cleared by software.
9	RFFULLF	RW	0	Receive FIFO Full Flag. This is set by hardware when receive FIFO pointer is 1111 meaning the FIFO is already full. This must be cleared by software.
8	RFRDYF	RW	0	Receive FIFO Ready Flag. This is set by hardware when receive FIFO pointer is equal to the threshold. This must be cleared by software.
7-4	TFIFOPT [3-0]	RO	0	0000 means the FIFO is empty.
3-0	RFIFOPT [3-0]	RO	0	0000 means the FIFO is empty.

SPIDAT0 (SPI Data Buffer Register)

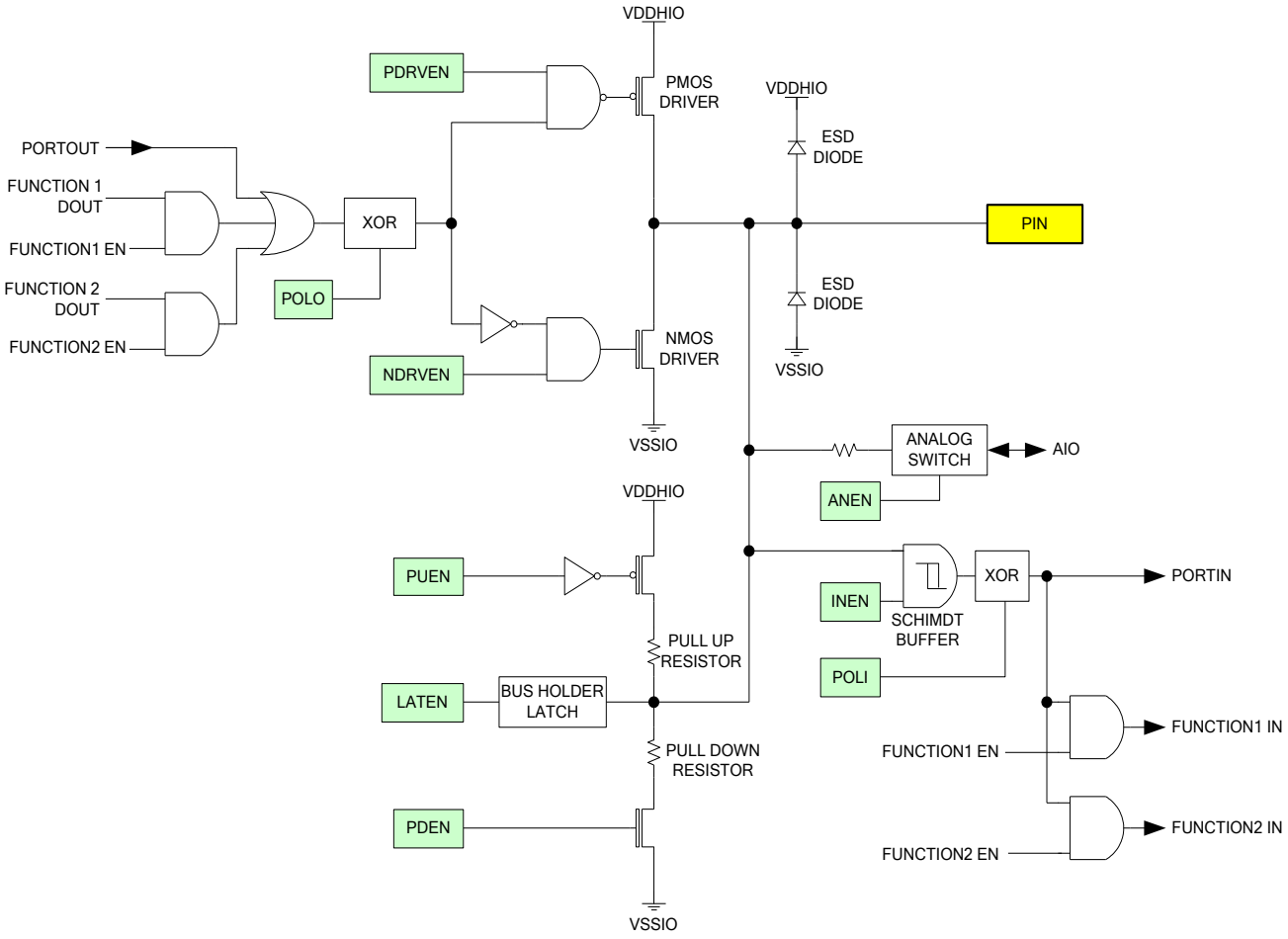
BITS	NAME	RW	DEF	DESCRIPTION
31-8	-	-	-	Reserved.
7-0	SPIDAT[7-0]	RW	0	This is the data register for both transmit and receive path. It acts as the buffer register for FIFO.

12. GPIO Port and Pin Configurations

The GPIO ports are typically used for bit-oriented operations. Therefore, each port is assigned with a register for control and configurations. All GPIO ports are shared with other peripheral functions and to allow proper operations, the register must be configured correctly. For those analog inputs, ADCIN0 – ADCIN7, if used for GPIO, only input should be allowed because it uses analog power supplies. For those pins with more than one functions, it also noted that these functions are not necessary mutually exclusive and it is up to the user's setting. For example, a GPIO pin also is RX of EUART, and can also be enabled as external interrupt if both functions are enabled. The data out and data in both have polarity controls, and this can be redundant or conflicting with the polarity setting within the functional units. The user program should be careful to have correct settings. The port output and input are always enabled. Therefore to enable other function outputs, PORTOUT must be set to low.

12.1 GPIO PORT

The IO port and pin circuits are shown in the following diagram. PORT register gives a detail description of the GPIO port configuration. All port registers have the same definition of Bit[15-0]. The only differences are their multifunction usages. Thus for specific port register, only FEN bits are described. The default setting of the register is all function disabled and all drivers disabled, and no pull-up and pull-down. Also please note for a multi-function GPIO pin, the GPIO port function is always enabled. As shown in the following block diagram, the PORTIN and PORTOUT for GPIO are always connected. So the pin status can always be read by software through GPIO register if INEN is set. It is also true that through GPIO register, PORTOUT can always affect the output of the pin. Therefore, for proper output of a multi-function, the PORTOUT must be set to 0.



PORT (I/O Pin Configuration)

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
20	FEN4	RW	0	Function 4 Enable
19	FEN3	RW	0	Function 3 Enable
18	FEN2	RW	0	Function 2 Enable
17	FEN1	RW	0	Function 1 Enable
16	INTGATE	RW	0	Gate the pin interrupt input. This is not the interrupt enable.
15-13	-	-	-	Reserved
12	ANEN	RW	0	Analog input switch enable
11	NDRVEN	RW	0	Low driver enable
10	PDRVEN	RW	0	High driver enable
9	LATEN	RW	0	Pin weak latch enable
8	PDEN	RW	0	Pull down resistor enable
7	PUEN	RW	0	Pull up resistor enable
6	IEN	RW	0	Input buffer enable
5	POLO	RW	0	Output Polarity
4	POLI	RW	0	Input Polarity
3	-	-	-	Reserved
2	PORTWE	WO	0	If this bit is 0, then only bit 0 is modified during write. When this bit is 0, register is not TC protected.
1	PORTIN	RO	0	Reading this bit reflects the actual state of the external pin.
0	PORTOUT	RW	0	Write to this bit to output the registered value to the pin. This bit when read reflects the registered value of PORTOUT. This may not be the same as PORTIN

12.2 Multifunction GPIO PORT Pin

All I/O pin have a GPIOXX register to define its circuit configurations. This ensures uniform ESD characteristics. Most of the pin can be used for more than one function and are routed to the specific functional macros. For pins with analog features, usually only one analog function is assigned to one pin. When configured as analog pin, the ANEN bit of the register must be set to 1 too, and all the drive to this pin must be turned-off, and input buffer should also be turned-off to avoid any noise.

PORT00 (P0/EMG/SCK) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	SCKEN	RW	0	Set 1 to enable SCK function of SPI Interface. This will connect the input to SCKIN of the SPI controller in slave mode, and connect the output to the SCKOUT as master mode.
17	EMGEN	RW	0	Set 1 to enable EMG function
16	INTGATE	RW	0	Set 1 to allow this pin to function as external interrupt
15-0	-	-	-	Same as PORT definition

PORT01 (P1/OVLA/SDO) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	SDO	RW	0	Set 1 to enable SDO function of SPI Interface. This will connect the output to the SDO of the SPI Controller
17	OVLA	RW	0	Set 1 to enable OVLA function
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition

PORT02 (P2/OVLB/SDI/PWME) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	PWME	RW	0	Set 1 to enable the function of PWM Channel E output.
18	SDI	RW	0	Set 1 to enable SDI function of SPI Interface. This will connect the input to the SDI of the SPI Controller
17	OVLA	RW	0	Set 1 to enable OVLB function
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition

PORT03 (P3/SCS/OVLC/PWMD) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	PWMD	RW	0	Set 1 to enable the function of PWM Channel D output.
18	SCS	RW	0	Set 1 to enable SCS function of SPI Interface. SCS is an input if SPI is in slave mode, and an output if in master mode.
17	OVLA	RW	0	Set 1 to enable OVLC function
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT04 (P4/MSCL0) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	MSCL0	RW	0	Set 1 to enable I^2C Master SCL function. This should be configured as an open-drain input/output.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT05 (P5/MSDA0) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	MSDA0	RW	0	Set 1 to enable I^2C Master SDA function This should be configured as an open-drain input/output.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition

PORT06 (P6/RX0/T3EX) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	T3EX	RW	0	Set this to 1 to use this pin as Timer 3 external input.
17	RX0	RW	0	Set 1 to enable RX function of EUART 0.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT07 (P7/TX0/T4EX) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	T4EX	RW	0	Set this to 1 to use this pin as Timer 4 external input.
17	TX0	RW	0	Set 1 to enable TX function of EUART 0.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT08 (P8/SSCL0/RX1) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	RX1	RW	0	Set 1 to enable RX function of EUART 1.
17	SSCL0	RW	0	Set 1 to enable SCL function of I^2C Slave. SCL is the serial clock for I^2C slave. In order for this to function correctly, the pin drive should be configured as open-drain I/O.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT09 (P11/SSDA1/TX1) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	TX1	RW	0	Set 1 to enable TX function of EUART 1.
17	SSDA0	RW	0	Set 1 to enable SDA function of I^2C Slave. SDA is the serial data for I^2C slave. In order for this to function correctly, the pin drive should be configured as open-drain I/O.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT10 (P10/AIN0) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	AIN0	RW	0	Set 1 to enable analog input channel 0 of the SAR ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT11 (P11/AIN1) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	AIN1	RW	0	Set 1 to enable analog input channel 1 of the SAR ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT12 (P12/AIN2) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	AIN2	RW	0	Set 1 to enable analog input channel 2 of the SAR ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT13 (P13/AIN3) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	AIN3	RW	0	Set 1 to enable analog input channel 3 of the SAR ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT14 (P14/AIN4) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	AIN4	RW	0	Set 1 to enable analog input channel 4 of the SAR ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT15 (P15/AIN5) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	AIN5	RW	0	Set 1 to enable analog input channel 5 of the SAR ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT16 (P16/ADCINE) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	ADCINE	RW	0	Set 1 to enable analog input channel E of the pipeline ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT17 (P17/ADCIND) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	ADCIND	RW	0	Set 1 to enable analog input channel D of the pipeline ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT18 (P18/SFCS) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	SFCS	RW	0	Set this to 1 to enable SCS function of external SPI Flash interface
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT19 (P19/SFDO) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	SFDO	RW	0	Set this to 1 to enable SDO function of external SPI Flash interface
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT20 (P20/SFCK) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	SFCK	RW	0	Set this to 1 to enable SCK function of external SPI Flash interface
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT21 (P21/SFDI) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	SFDI	RW	0	Set this to 1 to enable SDI function of external SPI Flash interface
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition

PORT22 (P22/TX2/PWMD) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	PWME	RW	0	Set this to 1 to enable function of PWM channel E output
17	TX2	RW	0	Set this to 1 to enable TX function of EUART 2.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT23 (P23/RX2/PWME) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	PWMD	RW	0	Set this to 1 to enable function of PWM channel D output
17	RX2	RW	0	Set this to 1 to enable RX function of EUART 2.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT24 (P24/AIN6) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	AIN6	RW	0	Set 1 to enable analog input channel 6 of the SAR ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition

PORT25 (P25/CANR) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	AIN7	RW	0	Set 1 to enable analog input channel 7 of the SAR ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition

PORT26 (P26/ADCINC) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	ADCINC	RW	0	Set 1 to enable analog input channel C of the pipeline ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT27 (P27/ADCINB) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	ADCINE	RW	0	Set 1 to enable analog input channel B of the pipeline ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

PORT28 (P28/ADCINA) TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-20	-	-	-	Reserved
19	-	-	-	Reserved
18	-	-	-	Reserved
17	ADCINE	RW	0	Set 1 to enable analog input channel A of the pipeline ADC. The corresponding port setting must be configured correctly for analog input to function correctly.
16	INTGATE	RW	0	Set 1 to allow this pin to function as an external interrupt
15-0	-	-	-	Same as PORT definition.

12.3 GPIO Interrupt

All GPIO ports can be configured to function as external interrupt by setting the INTGATE in the port configuration register. The interrupt condition can be set to level-sensitive, or edge-sensitive. It is possible to define multiple interrupt condition such as high level sensitive and high-to-low edge sensitive. The interrupts of all ports are wired-OR and then sent to the interrupt controller.

GPINTCFG1 TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-0	LEVELLO	RW	00	Set the corresponding bit of the GPIO port will allow the low level on the pins to generate an interrupt

GPINTCFG2 TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-0	LEVELHI	RW	00	Set the corresponding bit of the GPIO port will allow the high level on the pins to generate an interrupt

GPINTCFG3 TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-0	EDGELH	RW	00	Set the corresponding bit of the GPIO port will allow the low to high edge on the pins to generate an interrupt

GPINTCFG4 TC

BITS	NAME	TYPE	DEF	DESCRIPTION
31-0	EDGEHL	RW	00	Set the corresponding bit of the GPIO port will allow the high level on the pins to generate an interrupt

GPINTSTAT

BITS	NAME	TYPE	DEF	DESCRIPTION
31-0	GPINTF	RW	0	The corresponding set-bit positions reflect which GPIO cause the interrupt. This is a latched interrupt flag and must be cleared by software.

12.4 Dedicated Function Pin

For dedicated functional pins, they do not need to configure the function enable setting. However, the I/O structures are the same, the driving configuration and input configuration can be set for varieties of purpose. The motor PWM output pins are controlled by both the PIN configuration register and the Motor Controller. The drive configuration depends on both setting and condition. For example, if the pin configuration is set as a push-pull CMOS drive, then motor controller when under EMG condition can cause it to be Hi-Z. And if the pin configuration is OD, then the output is OD but can still be set to Hi-Z under EMG condition. Under the OD configuration, the force high function can thus just turn off the low drive, and does not cause active force. The pull-up and pull-down options, and LATEN are controlled by the pin configuration register setting. The IEN and ANEN should always be set to low. The polarity control for both input and output are not used. The PORTIN and PORTOUT bits are not used.

PINMOTORU TD

BITS	NAME	TYPE	DEF	DESCRIPTION
31-26	-	-	-	Reserved
15-0	-	-	-	Same as PORT definition.

PINMOTORV TD

BITS	NAME	TYPE	DEF	DESCRIPTION
31-26	-	-	-	Reserved
15-0	-	-	-	Same as PORT definition

PINMOTORW TD

BITS	NAME	TYPE	DEF	DESCRIPTION
31-26	-	-	-	Reserved
15-0	-	-	-	Same as PORT definition

PINMOTORX TD

BITS	NAME	TYPE	DEF	DESCRIPTION
31-26	-	-	-	Reserved
15-0	-	-	-	Same as PORT definition

PINMOTORY TD

BITS	NAME	TYPE	DEF	DESCRIPTION
31-26	-	-	-	Reserved
15-0	-	-	-	Same as PORT definition

PINMOTORZ TD

BITS	NAME	TYPE	DEF	DESCRIPTION
31-26	-	-	-	Reserved
15-0	-	-	-	Same as PORT definition

13. Electrical Characteristics

13.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT	NOTE
VDDHIO	Supply Voltage for IO and 1.8V regulator	5.5	V	
VDDHA	Supply Voltage for analog circuit	5.5	V	
TA	Ambient Operating Temperature	-40 – 85	℃	
TSTG	Storage Temperature	-65 – 150	℃	

13.2 Recommended Operating Condition

SYMBOL	PARAMETER	RATING	UNIT	NOTE
VDDHIO	Supply Voltage for IO and 1.8V regulator	3.0 - 5.5	V	
VDDHA	Supply Voltage for analog circuit	4.5 – 5.5	V	
TA	Ambient Operating Temperature	-40 – 85	℃	

13.3 DC Electrical Characteristics (VDDHIO=VDDHA=4.5V to 5.5V TA=-40C to 85℃)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Power Supply Current						
IDDC	Total IDD Core Current		120		mA	@125MHz
IDDH	Total IDD HIO Current		10		mA	All IO Hi-Z
IDDHA	Total IDD H analog Current		50		mA	
Core Power Supply Regulator and Power On Reset						
VDDCUT	Regulated VDDC Supply	1.6	1.8	2.0	V	Untrimmed
VDDCTM	Regulated VDDC Supply	1.72	1.8	1.88	V	Trimmed
IREGDRV	Sink Current for REGDRV	-	-	1.0	mA	Driving PNP Transistor
VPORUP	Power Up Reset Level Ramp Up	83	88	93	%	% of VDDC
VPORDN	Power Down Reset Level Ramp Down	65	70	75	%	% of VDDC
RSTN Reset						
VIHRS	Input High Voltage	+1.2	-	-	V	Reference to 0.5VDDH
VILRS	Input Low Voltage	-	-	-1.2	V	Reference to 0.5VDDH
VRSHYS	RSTN Hysteresis	-	1.2	-	V	VDDH=5V
GPIO						
VOH	Output High Voltage 1 mA	-	-0.4	-0.5	V	Reference to VDDHIO
VOH	Output High Voltage 4 mA	-	-0.6	-0.8	V	Reference to VDDHIO
VOL	Output Low Voltage 4 mA	-	0.4	0.5	V	Reference to VSSIO
VOL	Output Low Voltage 12 mA	-	0.6	0.8	V	
VIH	Input High Voltage	0.7	-	-	V	Reference to 0.5VDDH
VIL	Input Low Voltage	-0.7	-	-	V	Reference to 0.5VDDH
VIHYS	Input Hysteresis	120	250	600	mV	
RPU	Equivalent Pull-Up resistance		160K		Ohm	
RPD	Equivalent Pull-Down Resistance		80K		Ohm	
RPULAT	Equivalent Pull-Up Resistance for Latch		10K		Ohm	Measured at VDDHIO
RPDLAT	Equivalent Pull-Down Resistance for Latch		5K		Ohm	Measured at 0V

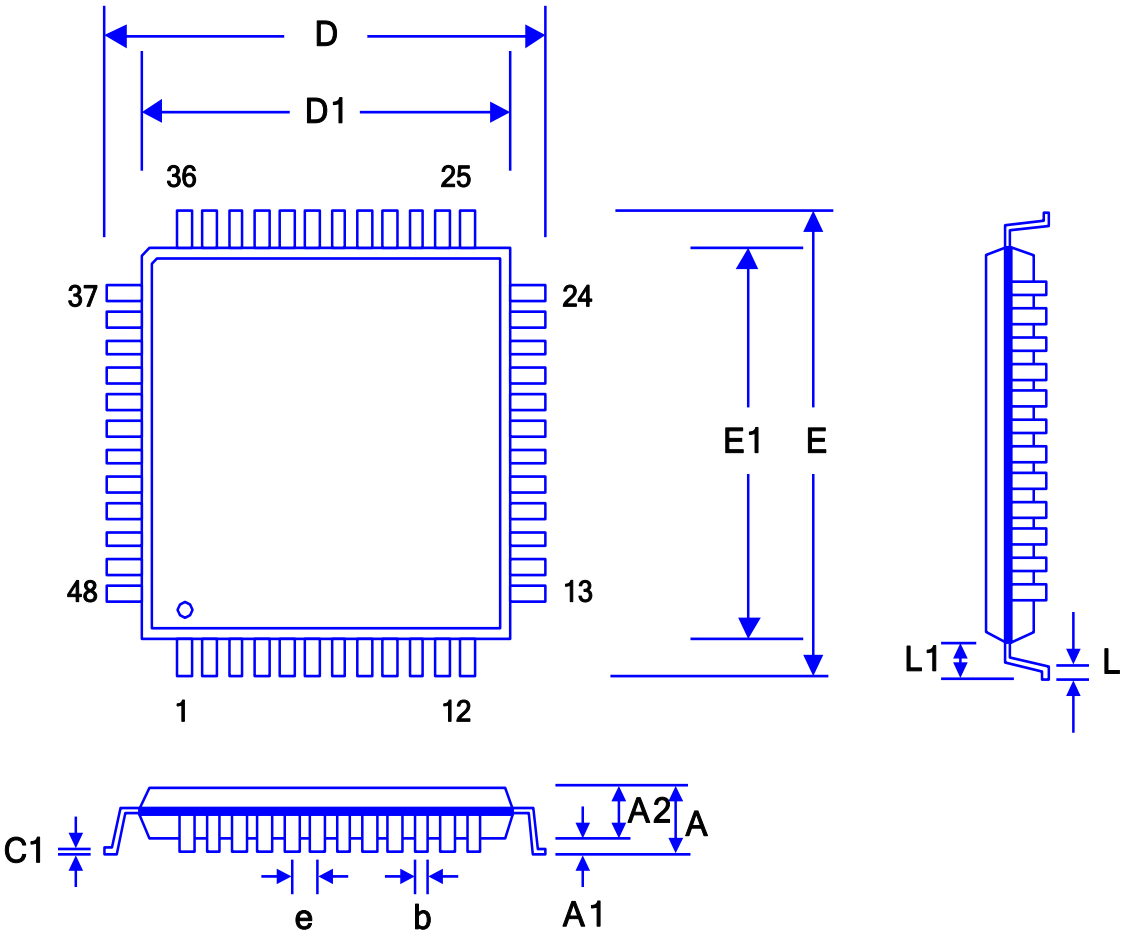
RAN	Equivalent Resistance for Analog Switch		600		Ohm	
Analog Reference						
VR30UT	REF30 Untrimmed	2.5	3.0	3.5	V	
VR30TM	REF30 Trimmed	2.92	3.0	3.08	V	
IVRSRC	Maximum REF source current	-	-	10	mA	50mV deviation
IVRSNK	Maximum REF sink current	-	-	100	uA	
VR21AC	REF20 and REF10 accuracy		+/-5		%	After REF30 Trimmed
Pipeline ADC						
VINPL	Input DC range	1.0	-	3.0	V	
RINPL	Input Equivalent Resistance		20K		Ohm	Sample at 1MHz
RINPLOFF	Input Equivalent Resistance Off State		500K		Ohm	
CINPL	Input Equivalent Capacitance		10		pF	
LINPL	Pipeline ADC Accuracy		+/- 2		LSB	
Analog Comparator						
VINCMP	Input Range	1.0	-	3.0	V	
INSEN	Input Sensitivity		5		mV	
INHYS	Input Hysteresis		20		mV	
THACC	Compare threshold accuracy		+/- 25		mV	After REF30 Trimmed
SAR ADC						
VINSAR	Input DC Range	0	-	3.0	V	
LINSARM	SAR ADC Accuracy (0.5V – 2.5V)		+/- 2		LSB	
LINSARE	SAR ADC Accuracy (0-0.5V, 2.5V-3.0V)		+/-5		LSB	
PLL						
IDDPLL	PLL Supply Current		20		mA	PLLVDD=1.8V,125MHz
VPLLLPF	PLL LPF voltage level	0	0.9	1.8	V	
Low Supply (VDDHR) Voltage Detection						
VDET	Detection Range	2.8	-	5.0	V	
VDETHYS	Detection Hysteresis		100		mV	

13.4 AC Electrical Characteristics (VDDHIO=VDDHA=4.5V to 5.5V TA=-40℃ to 85℃)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
System Clock and Reset						
FSYS	System Clock Frequency	8	100	125	MHz	
FXOSC	Crystal Oscillator Frequency	8	16	20	MHz	
FPLL	PLL Frequency Range	40	100	150	MHz	
TSXOSC	Stable Time for XOSC after power up	50	-	-	msec	VDDHIO>4.5V
TSPLL	Stable Time for PLL after enable	100	-	-	msec	
Supply Timing						
TSUPRU	Maximum VDDH Ramp Up time	-	-	50	msec	
TSUPRD	Maximum VDDH Ramp Down Time	-	-	50	msec	
TPOR	Power On Reset Delay	-	10	-	msec	XOSC=16MHz
TSPLL	Stable Time for PLL after enable	100	-	-	msec	
Flash Memory Timing						
TEMAC	Embedded Flash Access Time	-	35	45	nsec	TWAIT must > TEMAC
TEMWR	Embedded Flash Write Time	-	20	25	usec	
TEMSER	Embedded Flash Sector Erase Time	-	2	2.5	msec	
TEMMER	Embedded Flash Mass Erase Time	-	10	12	msec	
FSPFM	SPI Flash Clock Frequency	1	64	80	MHz	
Pipeline ADC						
FPLADC	Maximum Pipeline ADC Frequency	-	-	4	MHz	
TPLADC	Latency of Pipeline ADC	-	14	-	Cycle	ADC clock cycles
TSHD	Track and Hold Delay	-	100	-	nsec	
SAR ADC						
FSARADC	Maximum SAR ADC Frequency	-	-	4	MHz	
TSARADC	Conversion time of SAR ADC	-	16	-	Cycle	ADC clock cycles
TSADCSE	Set up time for SAR ADC channel select	250	-	-	nsec	
Analog Comparator						
TDACMP	Analog comparator delay	-	-	250	nsec	

PACKAGE OUTLINE

48-Pin LQFP



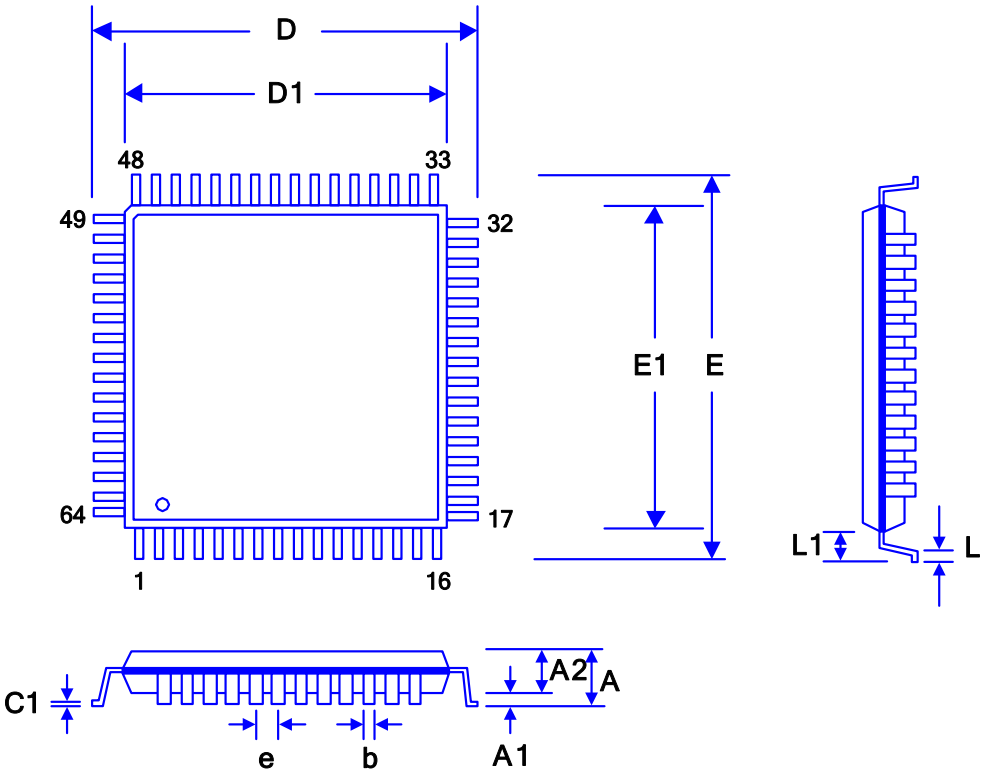
SYMBOL	DIMENSIONS IN MILLIMETERS	
	MIN.	MAX.
A	-	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

1. JEDEC outline: MS-026 BBC.

2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

3. Dimension b does not include damper protrusion. Allowable damper protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.

64-Pin LQFP



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	-	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	

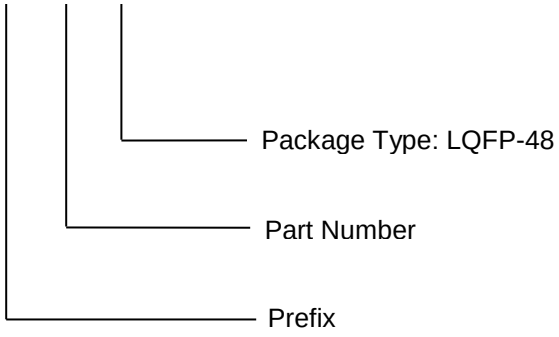
Notes:

1. *JEDEC outline: MS-026 BBD.*
2. *Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
3. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm.

ORDERING INFORMATION

Prefix	Part Number	Package Type	Suffix
CS	6257	AG : LQFP-64	
		BG : LQFP-48	

Example: CS 6257 BG



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14. Test Mode and Writer-Mode

This section contains the description of test modes and embedded Flash programming, should not be released to customer. The following table lists the various test modes.

PLLLFP	CPF	SMTEN	Operation Mode
0-1.8V	0	0	Normal Mode
HH > 4V	0	0	Flash Writer mode and Trimming mode
X	1	1	CP Flash Test
X	1	0	CP scan/BIST test

*** CPF and SMTEN are probe pad with pull-down. It is down bonded to substrate in package form. Preferably it is placed close to a VSS pad.

14.1 CP Flash Test Mode

This mode is enabled when CPF=1 and SMTEN=1. Under this mode, other part of logic is in reset mode and non-essential analog peripherals are disabled.

i. The tester needs to apply 1.8V to some VDD18C and 5V to some VDDH pads.
ii. Flash has a separate VDD18C pad (VDDC18CF) and are supplied separately. VDDC18CF needs to be placed next to a VDD18C pad and bonded to VDD18C finger in package form. VDDC18CF uses ESD to VDDHIO.
iii. There are two separate dedicated probe pads VPP and VNN. These two pads are not bonded.
iv. IO signals to and from tester are in VDDH – 0V range.
v. Additional IO pins must be enabled to allow the following signals to internal Flash macro.
   SMTEN (IN). (This pin at package should be bonded to VSS)
   SCE (IN) = P11
   SCLK (IN) = P12
   SIO (I/O) = P13.
vi. Note SMTEN pad should be bonded to VSS at package.
vii. Note the output drive enable control of IOCELL of P13 needs to be controlled by SIO_OEN of the Flash macro under this mode.

Mode	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13
CPF	X	X	X	X	X	X	X	X	X	X	X	SCE	SCLK	SIO

14.2 CP SCAN and BIST Test Mode

This mode is enabled when CPF=1 and SMTEN=0. Use ADCINA, ADCINB, ADCINC to further differentiate the scan and test mode.

ADCINA	ADCINB	ADCINC	Test Mode
0	0	0	SCAN1
0	0	1	SCAN2
1	0	0	BIST1
1	0	1	BIST2

Only SCAN1 mode is used. SCAN enable is TDI. TDI must be 1. There are total 17 SCAN chains. The corresponding scan chain input and output are listed as following.

CHAIN	SCANIN	SCANOUT
#1	P0	P1
#2	P2	P3
#3	P4	P5
#4	P6	P7
#5	P8	P9
#6	P10	P11
#7	P12	P13
#8	P14	P15
#9	P16	P17
#10	P18	P19
#11	P20	P21
#12	P22	P23
#13	P24	P25
#14	TMS	TDO
#15	MOTORU	MOTORV
#16	MOTORW	MOTORX
#17	MOTORY	MOTORZ

Only BIST1 mode is used. The BIST mode uses P0 to indicate the completion of the BIST test. P1 to P6 are used to indicate the BIST fail or success condition (High indicates failure). The tester should first wait for P0 to be high then read P1 to P6 to determine the SRAM BIST failure.

BISTOUT	Description
P0	BIST FINISH
P1	SRAM4KX32 – 1
P2	SRAM4KX32 – 2
P3	SRAM4KX32 – 3
P4	SRAM4KX32 – 4
P5	SRAM2KX64 (Cache)
P6	SRAM2KX32 (Tag)

i. The tester needs to supply 1.8V to all VDD18C and 5V to all VDDH pads.
ii. IO signals to and from tester are in VDDH – 0V range.
iii. SYSTEM clock is applied externally through XTIN.
iv. Need to determine how many scan chains and BIST outputs.

14.3 Writer Mode and Trimming Mode

This mode is enabled when PLLLPF is forced to > 4V. Under this mode, EJTAG pins are directed to P0 to P3 and use the same protocol to perform Flash programming. P0=TMS, P1=TCK, P2=TDI, P3=TDO, P4=TRSTN. The system clock is forced from XTIN. This mode also covers Trimming of the following internal values. P5=LVDOUT. P[13-6] are used as data input. MOTORU, MOTORV, MOTORW are used to select Trimming Mode.

MOTORU	MOTORV	MOTORW	TRIM Mode
0	X	X	None
1	0	0	Reserved
1	0	1	P[13-6] is passed to REGTRM[7-0]
1	1	0	P[13-6] is passed to LVDEN and LVDTHD[6-0]
1	1	1	P[13-6] is passed to REF30TM[7-0]

14.4 Function Test

Function test is performed by writing a target self-test program to perform real function test. It is not necessary to do this at wafer sort level. The self-test program and ISP program should be written to the flash at the same time. Then it is erased by sector erase at the last. So at the package level test, the sequence is as following.

i. Open/Short/Leakage
ii. ICC test
iii. PLLLPF=HH. Trimming.
iv. PLLLPF=HH. Program ISP and Self-Test program.
v. PLLLPF=FLOATING. Enter Normal mode, and perform Self-Test program.
vi. PLLLPF=HH. Erase Self-Test Program. Verify ISP program
vii. Finish

14.5 IFB Content

There is 128 x 16 IFB associated with E-Flash memory. The IFB is partitioned into two segments – One for manufacture data and one for user data, each is 64 x 16. In byte address, the manufacturer data resides in 00-7F, and the user data resides in 80-FF. The IFB can be erased only in WRITER mode, this prevent the user program to modify any of the manufacture data. For User data, it can only serve as one-time programmable data. The following list the manufacture data in byte unit.

00 – 0F	Device Name and Revision
10 – 1F	Die Record and FT date code
20	VDDC=1.8V Trim
22	IOSC=8MHz Trim
24	REF30 Trim (Not Needed)
26	REFPS=2.5V Trim
28	LVDT = 4.0V Trim
30	LVDT = 3.0V Trim
--	
70-7F	00 Retention Test
80-FF	User OTP Data