CS-7104

5V, 250mA Voice Coil Driver with H-bridge, 4:1 Gain Switch, and Head Retract Circuitry

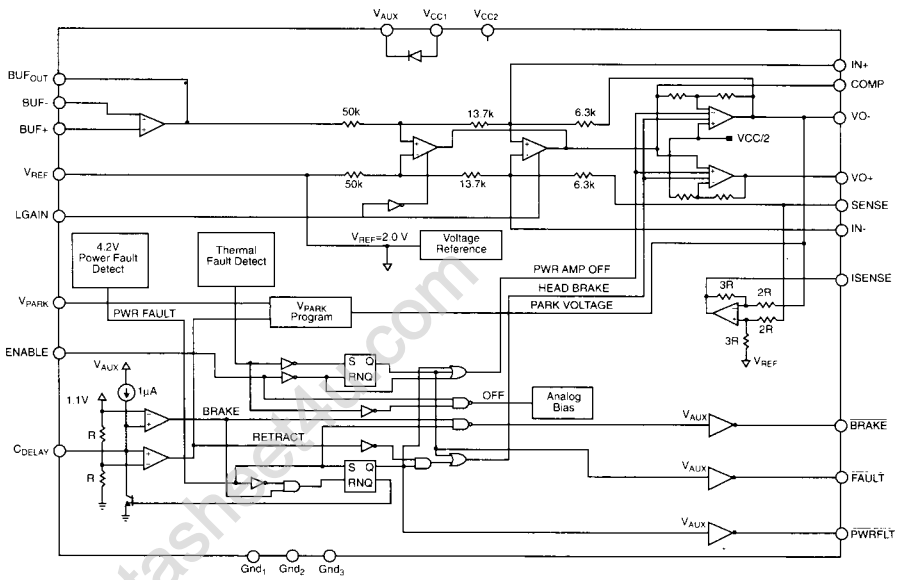
Description

The CS-7104 is a voice coil motor driver used in 5V, 2.5 inch hard disk drive servo systems. It contains the complete H-bridge power amplifiers and all control functions. Head retraction circuitry is present to allow controlled shutdown of the drive. Power fault and thermal fault detection are also included. A gain switch permits 4:1 transconductance changes.

Absolute Maximum Ratings

Supply Voltage	10V
Auxiliary Supply Voltage	17V
Logic Input Voltage	-0.3V to V_{AUX}
Logic Output Voltage (not FAULT pin)	-0.3V to 17V
Logic Output Voltage (not Brake pin)	-0.3V to 17V
H-Bridge Output Current	250mA
Maximum Power Dissipation	500mW
Electrostatic Discharge (Human Body Model)	2kV
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Maximum Junction Temperature	150°C

Block Diagram

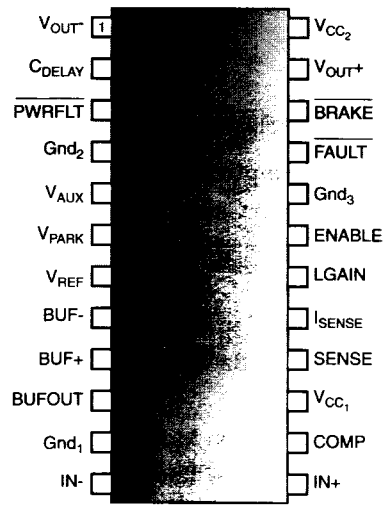


Features

- Single 5V Power Supply
- Full 250mA H-Bridge
- Low System Offset Current (4mA)
- Low Supply Current (6mA)
- Low Standby Current
- Internally Compensated Amplifiers
- No Crossover Distortion
- 4:1 Gain Switch
- Programmable Retract Voltage
- Programmable Bandwidth
- Power Fault Detector
- On Chip Transient Protection

Package Options

24 Lead SO Wide



CSC™ CHERRY SEMICONDUCTOR

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Electrical Characteristics: V_{CC} =4.5V to 5.5V; T_A=0°C to 70°C unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Supply					
Supply Voltage (V_{CC_1}, V_{CC_2})		4.5	5.0	5.5	V
Auxiliary Voltage, V_{AUX}		2.0		15.0	V
Auxiliary Current, I_{AUX}	Head Brake Mode V_{CC}=0; V_{AUX}=5.0V		13	20	mA
Total Supply Current	V_{ENABLE}=2.0V		12	25	mA
	V_{ENABLE}=0.8V			3	mA
■ Logic Inputs					
Input Current					
ENABLE=High	V_{IN}=2.0V			100	uA
ENABLE=Low	V_{IN}=0.8			-100	uA
LGAIN Low input Current	V_{IN}=0.8			-200	uA
Logic High Voltage			1.5	2.0	V
Logic Low Voltage		0.8	1.5		V
Transconductance					
(A_V=1; T_A=25°C)	I_{OUT}=100mA	95	100	105	mA/V
	I_{OUT}=25mA	23.7	25.0	26.3	mA/V
Transconductance					
(A_V=1; T_A=0°Cto 70°C)	I_{OUT}=100mA	93	100	107	mA/V
	I_{OUT}=25mA	23.2	25.0	26.8	mA/V
Output Offset Current	T_A=25°C			1.0	mA
	T_A=0°Cto 70°C			1.25	mA
Input Voltage Range	V_{REF}=2.0V	0.50		3.50	V
Frequency Response		30			kHz
■ Power Amplifier					
Voltage Gain			14		V/V
Frequency Response		60			kHz
Bridge Output Current		250			mA
Quiescent Bias Current per side			4		mA
Bridge Saturation Voltage	T_A=25°C; I_{OUT}=100mA			0.25	V
	T_A=25°C; I_{OUT}=200mA			0.50	V
	T_A=0°C to 70°C; I_{OUT}=200mA			0.60	V
Thermal Shutdown Temperature				160	°C
■ Buffer Amplifier					
Open Loop Gain		60			dB
Input Offset Voltage				5	mV
Input Offset Current			10	100	nA
Input Bias Current			1.0	5.0	uA
Unity Gain Bandwidth		300	1000		kHz
PSRR		50			dB
Input Common Mode Range		0.1		3.5	V
Output Voltage Range		0.1		3.5	V
■ I_{SENSE} Amplifier					
Closed Loop Gain	V_{IN}=V_{OUT}-SENSE	1.45	1.50	1.58	V/V
Input Offset Voltage				5	mV

Electrical Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Power Fault Detection and Timer					
V_{FAULT}		3.99	4.20	4.41	V
V_{FAULT} Hysteresis			100	200	mV
C_{DELAY} Charging Current		0.75	1.00	1.25	uA
C_{DELAY} Park Voltage Threshold		0.45	0.55	0.65	V
C_{DELAY} Break Voltage Threshold		0.90	1.10	1.30	V
■ Head Park					
V_{PARK}	R_{PARK}=5kΩ; I_{COIL}=1mA	0.4	0.5	0.6	V
Park Current Capability		10	20		mA
■ Voltage Reference					
V_{REF}		1.92	2.00	2.08	V
V_{REF} Output Current		2.0			V
PSRR		40			dB
■ Head Brake					
V_{OUT}+ Brake	I_{OUT}=50mA; V_{AUX}=3.0V			0.3	V
V_{OUT}+ Brake	I_{OUT}=50mA; V_{AUX}=3.0V			0.3	V
■ Logic Outputs					
$\overline{BRAKE}$ V_{OUT}	I_{OUT}=-10uA			0.4	V
$\overline{FAULT}$ V_{OUT}	I_{OUT}=-10uA			0.4	V
$\overline{PWRFLT}$ V_{OUT}	I_{OUT}=-10uA			0.4	V

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
24 Lead SO Wide		
1	V_{OUT}-	H-Bridge negative output
2	C_{DELAY}	An external capacitor on this pin sets the time intervals for Head Brake, HeadPark and Spin Brake
3	$\overline{PWRFLT}$	Digital output that signals a low supply voltage condition
4	Gnd2	Ground for H-bridge driver
5	V_{AUX}	Auxiliary power for head park during a VCC failure
6	V_{PARK}	Park voltage programming pin
7	V_{REF}	Internal voltage reference
8	BUF-	Buffer amplifier negative input
9	BUF+	Buffer amplifier positive input
10	BUF_{OUT}	Buffer amplifier output
11	Gnd1	Ground
12	IN-	Error amplifier negative input
13	IN+	Error amplifier positive input
14	COMP	Error amplifier compensation pin
15	V_{CC1}	Positive supply voltage
16	SENSE	VCM current sense input
17	I_{SENSE}	VCM current sense amplifier input

Package Pin Description: continued

PACKAGE PIN #	PIN SYMBOL	FUNCTION
24 Lead SO Wide		
18	LGAIN	Digital input that selects high or low transconductance
19	ENABLE	Digital input that selects standby or full power mode
20	Gnd_3	Ground for H-bridge driver
21	$\overline{FAULT}$	Digital signal indicating a thermal fault condition; the pin is reset through the ENABLE pin
22	$\overline{BRAKE}$	Digital output to brake the spin motor
23	$V_{OUT}+$	H-bridge positive output
24	V_{CC2}	Positive supply voltage for H-bridge driver

Circuit Description

Logic Functions

The ENABLE input is used to select full power mode or standby mode. When ENABLE is high, the circuit is full power mode. When ENABLE is low, the circuit is in standby mode with only the logic functions receiving power.

The LGAIN input selects high or low transconductance. When LGAIN is high, the circuit is in the low transconductance mode. The LGAIN input pin has a 50kΩ internal pull up resistor.

The $\overline{BRAKE}$ output is a PNP transistor with a 70 kΩ internal pull down resistor that is intended to drive an external FET spin brake circuit.

The $\overline{FAULT}$ line is an NPN transistor with a 70 kΩ internal pull up resistor.

The $\overline{PWRFLT}$ line is an NPN transistor with a 70 kΩ internal pull up resistor. Its correct logic state is maintained down to V_{CC}=1.0V.

Power Amplifier

The power amplifier is a full H-bridge with 250mA capability and built in protection diodes. The differential voltage gain of the bridge is 14.

The amplifier is protected from overload by thermal shutdown circuitry. If a thermal overload condition occurs, the amplifier is turned off and remains off until the ENABLE input line is toggled low then high.

Buffer Amplifier

The buffer amplifier is a low offset operational amplifier that can be used either as an additional gain stage or as a second order low pass filter.

Power Fault Detection

The power fault detection circuitry monitors V_{CC1}. If an under voltage condition occurs, a timed sequence of events happens. First the head brake is activated. The head park follows and finally the $\overline{BRAKE}$ line goes low, initiating the spin brake. If power recovers at any time during the sequence, the head brake and head park will complete their sequences. The spin brake will be canceled if the supply voltage recovers in time.

During head brake, both power NPN transistors in the H-bridge are turned on. Braking occurs in response to either a power fault or a thermal shutdown fault.

Head Park only occurs if there is a power fault. During head park, one side of the H-bridge is pulled low and a voltage, preset at the V_{PARK} pin, is applied across the VCM.

The timing of the head brake, head park and spin brake is controlled by the power fault timer. The timer uses an internally generated charge current and an external capacitor. Two threshold levels create the three timing sequences. While the capacitor is charging to the first threshold, the head brake is initiated. Head park is initiated as the capacitor passes to the second threshold. Once the capacitor's charge exceeds the second threshold, the spin brake function is activated.The $\overline{BRAKE}$ output is brought low and the timer remains in this state until power is restored. If power is restored while the timer is in this mode, the spin brake will be released.

Package Specification

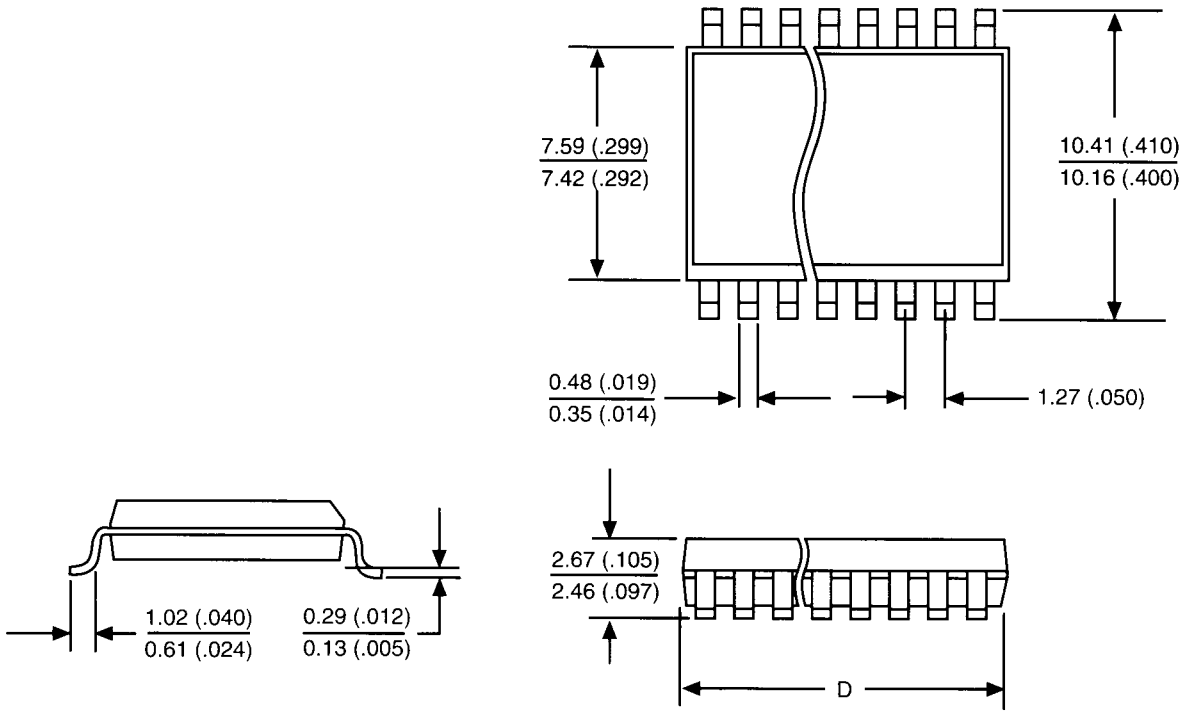
PACKAGE DIMENSIONS IN mm (INCHES)

	D			
Lead Count	**Metric**		**English**	
	Max	Min	Max	Min
24	15.54	15.29	.612	.602

PACKAGE THERMAL DATA

Thermal Data		**24L SO Wide**	
$R\Theta_{JC}$	typ	16	°C/W
$R\Theta_{JA}$	typ	80	°C/W

SO Wide



Ordering Information

Part Number	**Description**
CS-7104DW24	24 Lead SO Wide

Preliminary

This product is in the preproduction stages of the design process. The data sheet contains preliminary data. CSC reserves the right to make changes to the specifications without notice. Please contact CSC for the latest available information.