FEATURES

- 240 MSPS Throughput Rate
- Triple 10-Bit D/A Converters
- SFDR
- –70 dB at f_{CLK} = 50 M H_Z, f_{OUT} = 1 M H_Z
- –53 dB at f_{CLK} = 140 M H_Z, f_{OUT} = 40 M H_Z
- RS-343A/RS-170 Compatible Output
- Complementary Outputs
- DAC Output Current Range : 2 mA to 26 mA
- TTL-Compatible Inputs
- Internal Reference :1.23 V
- Single Supply +5 V/+3.3 V Operation
- Low Power Dissipation (30 mW min @ 3 V)
- Low Power Standby Mode (6 mW typ @ 3 V)
- Industrial Temperature Range (-40℃ to +85℃)

GENERAL DESCRIPTION

The CS7123 is a triple high speed, digital-to-analog converter on a single monolithic chip. It consists of three high speed, 10-bit, video D/A converters with complementary outputs, a standard TTL input interface and a high impedance, analog output current source .

The CS7123 has three separate 10-bit-wide input ports. A single +5 V/+3.3 V power supply and clock are all that are required to make the part functional. The CS7123 has addi-tional video control signals, composite SYNC and BLANK.

The CS7123 also has a power-save mode.

The CS7123 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. The CS7123 is available in a 48-lead LQFP package.

APPLICATIONS

- Digital Video Systems (1600×1200@ 100 Hz)
- High Resolution Color Graphics
- Digital Radio Modulation
- Image Processing
- Instrumentation
- Video Signal Reconstruction

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figure1. FUNCTIONAL BLOCK DIAGRAM

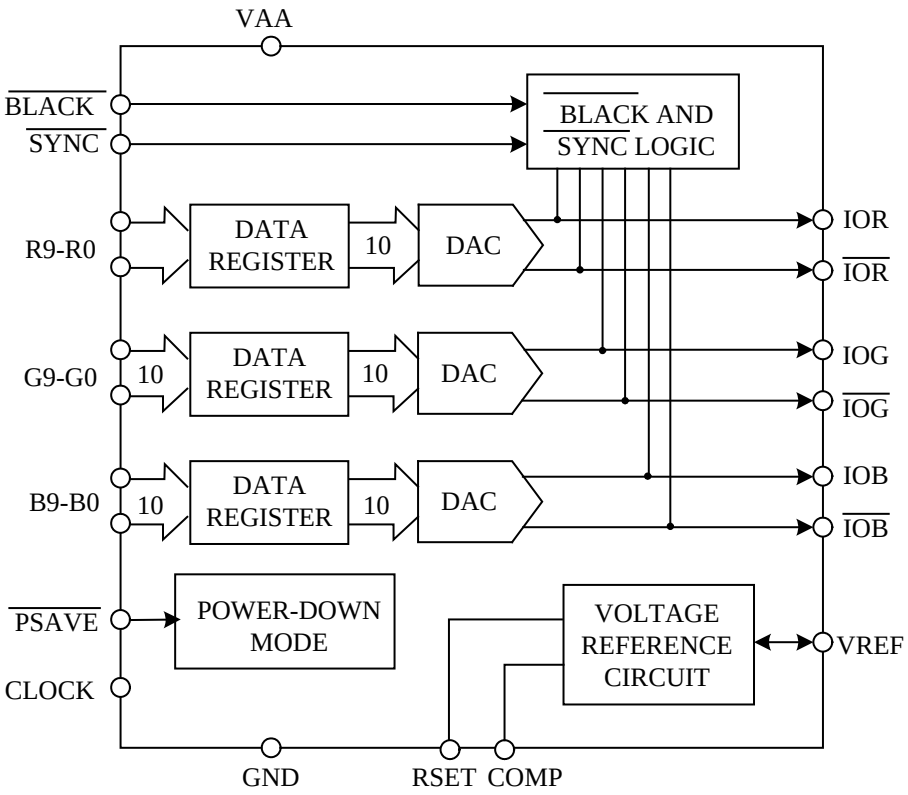

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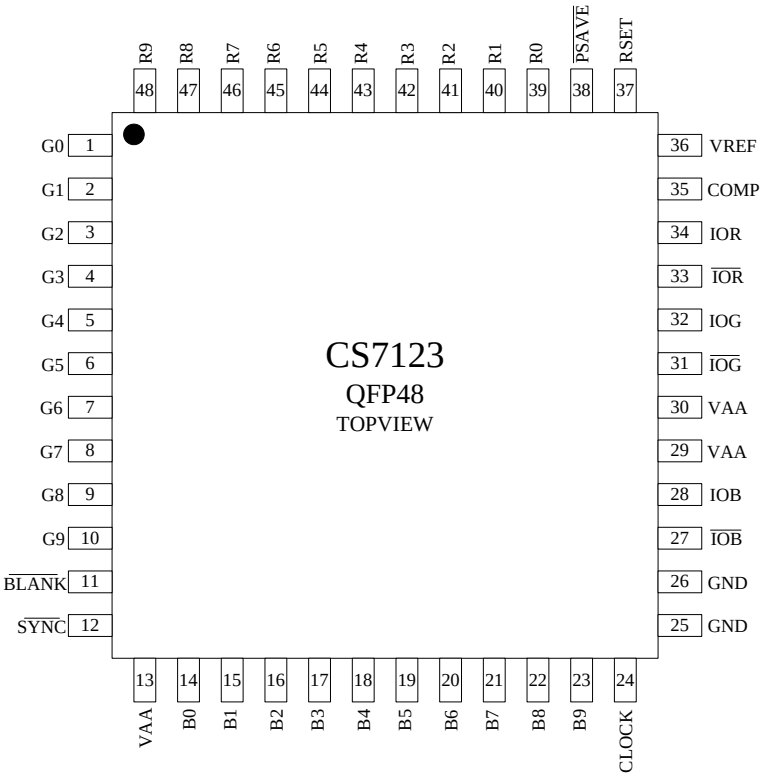
Figure 2. PIN CONFIGURATION



Pin order	Pin mnemonic	Pin name	Function
1-10	G0-G9	Green pixel data inputs	(TTL compatible)，Pixel data is latched on the rising edge of CLOCK.G0 is the least significant data bits.unused pixel data inputs should be connected to either the regular PCB power or ground plane.
11	$\overline{\text{BLANK}}$	Composite blank control input	(TTL compatible). A logic zero on this control input drives the analog outputs, IOR, IOB and IOG, to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While BLANK is a logical zero, the R0–R9, G0–G9 and R0–R9 pixel inputs are ignored.
12	$\overline{\text{SYNC}}$	Composite sync control input	(TTL compatible). A logical zero on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source. This is internally connected to the IOG analog output.

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Pin order	Pin mnemonic	Pin name	Function
			SYNC does not override any other control or data input, therefore, it should only be asserted during the blanking interval. SYNC is latched on the rising edge of CLOCK. If sync information is not required on the green channel, the $\overline{\text{SYNC}}$ input should be tied to logical zero.
13	$\mathbf{V_{AA}}$	Analog power supply	(5 V ± 5%). All V_{AA} pins on the CS7123 must be connected.
14-23	B0-B9	Bule pixel data inputs	(TTL compatible)，Pixel data is latched on the rising edge of CLOCK.B0 is the least significant data bits.unused pixel data inputs should be connected to either the regular PCB power or ground plane.
24	CLOCK	Clock input	(TTL compatible). The rising edge of CLOCK latches the R0–R9, G0–G9, B0–B9, $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
25、26	GND	Ground	All GND pins must be connected.
27	$\overline{\text{IOB}}$	Differential blue current outputs	(high impedance current sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into a doubly terminated 75Ω load. If the complementary outputs are not required, these outputs should be tied to ground.
28	IOB	blue current outputs	These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
29、30	$\mathbf{V_{AA}}$	Analog power supply	(5 V ± 5%). All V_{AA} pins on the CS7123 must be connected.
31	$\overline{\text{IOG}}$	Differential green current outputs	(high impedance current sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into a doubly terminated 75Ω load. If the complementary outputs are not required, these outputs should be tied to ground.

Pin order	Pin mnemonic	Pin name	Function
32	IOG	green current outputs	These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
33	$\overline{\text{IOR}}$	Differential red current outputs	(high impedance current sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into a doubly terminated 75Ω load. If the complementary outputs are not required, these outputs should be tied to ground.
34	IOR	Red current outputs	These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
35	COMP	Compensation pin	This is a compensation pin for the internal reference amplifier. A 0.1μF ceramic capacitor must be connected between COMP and V_{AA}.
36	V_{REF}	Voltage reference input	It is for DACs or voltage reference output (1.235 V)
37	R_{SET}	A resistor connected between this pin and GND	controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on IOG (assuming ISYNC is connected to IOG) is given by: $R_{SET} = 11.445 \times V_{REF} / IOG\ (mA)$ The relationship between R_{SET} and the full-scale output current on IOR, IOG and IOB is given by: $IOR,IOB(mA) = 7.992 \times V_{REF}\ (V)\ R_{SET}\ (\Omega)$
38	$\overline{\text{PSAVE}}$	Power Save Control Pin	Reduced power consumption is available on the CS7123 when this pin is active.
39-48	R0-R9	Red pixel data inputs	TTL compatible,Pixel data is latched on the rising edge of CLOCK.R0 is the least significant data bits.unused pixel data inputs should be connected to either the regular PCB power or ground plane.

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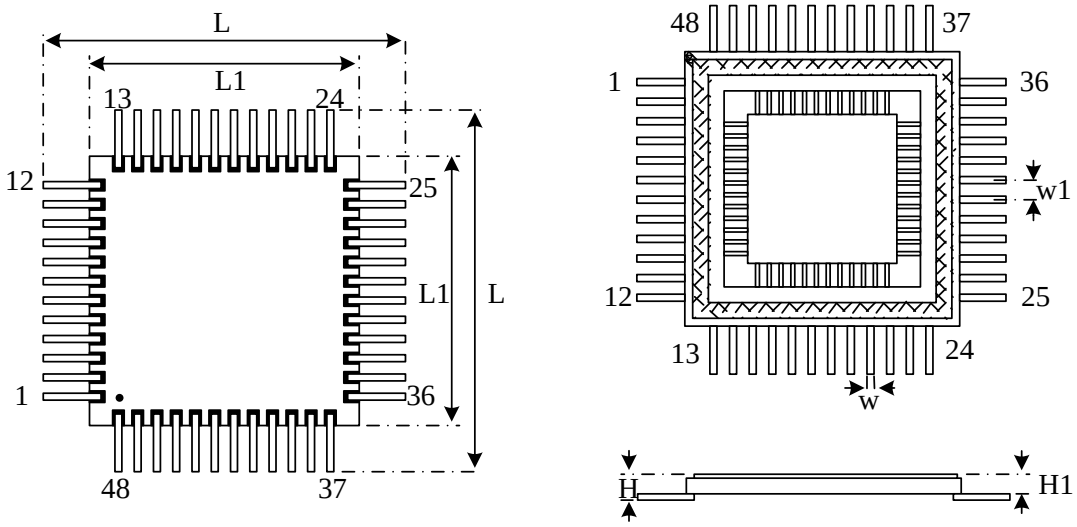
Figure 3. The figuration of CS7123



Electronic features :

5V SPECIFICATIONS(VAA=5V±5%, V_{REF}=1.235V, R_{SET}=560Ω, C_L=10pF, All specifications T_{MIN} to T_{MAX} unless otherwise noted, $T_{J\ MAX}$ = 110℃)

Parameter		Min	Typ	Max	Units	Test conditions
STATIC PERFORMANCE	Resolution (Each DAC)		10		Bits	Guaranteed Monotonic
	Integral Nonlinearity (INL)	−1	±0.4	+1	LSB	
	Differential Nonlinearity(DNL)	−1	±0.25	+1	LSB	
DIGITAL AND CONTROL INPUTS	Input highVoltage, V_{IH}	2			V	V_{IN}=0.0V or V_{IN}=VDD
	Input Low Voltage, V_{IL}			0.8	V	
	Input Current, I_{IN}	−1		+1	uA	
	PSAVE Pull-Up Current		20		uA	
	Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS	Output Current	2.0		26.5	mA	Green DAC Sync=High

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Parameter		Min	Typ	Max	Units	Test conditions
	Output Current	2.0		18.5	mA	R/G/B DAC Sync=Low
	DAC to DAC Matching		1.0	5	%	
	Output Compliance Range, V_{OC}	0		+1.4	V	
	Output Impedance, R_{OUT}		100		KΩ	
	Output Capacitance,C_{OUT}		10		pF	I_{OUT}=0mA
	Offset Error	-0.025		+0.025	%FSR	Test with DAC Output=0
	Gain Error2	-5.0		+5.0	%FSR	FSR=17.62mA
VOLTAGE REFERENCE (Ext. and Int.) Reference Range, VREF		1.12	1.235	1.35	V	
POWER DISSIPATION	Digital Supply Current		3.4	9	mA	f_{CLK}=50MHz
	Digital Supply Current		10.5	15	mA	f_{CLK}=140MHz
	Digital Supply Current		18	25	mA	f_{CLK}=240MHz
	Analog Supply Current		67	72	mA	R_{SET}=560Ω□
	Analog Supply Current		8		mA	R_{SET}=4933Ω□
	Standby Supply Current		2.1	5.0	mA	PSAVE=Low, Digital and Control Inputs at VDD
Power Supply Rejection Ratio			0.1	0.5	%	

5V DYNAMIC SPECIFICATIONS(VAA=5V±5%, V_{REF}=1.235V, R_{SET}=560Ω, C_L=10pF, All specifications T_{MIN} to T_{MAX} unless otherwise noted, $T_{J\,MAX}$ = 110℃**)**

	Min	Typ	Max	Units
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist2				
Single-Ended Output				
f_{CLK}=50MHz ; f_{OUT}=1.00MHz		67		dBc
f_{CLK}=50MHz ; f_{OUT}=2.51MHz		67		dBc
f_{CLK}=50MHz ; f_{OUT}=5.04MHz		63		dBc
f_{CLK}=50MHz ; f_{OUT}=20.2MHz		55		dBc
f_{CLK}=100MHz ; f_{OUT}=2.51MHz		62		dBc
f_{CLK}=100MHz ; f_{OUT}=5.04MHz		60		dBc

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	Min	Typ	Max	Units
f_{CLK}=100MHz ; f_{OUT}=20.2MHz		54		dBc
f_{CLK}=100MHz ; f_{OUT}=40.4MHz		48		dBc
f_{CLK}=140MHz ; f_{OUT}=2.51MHz		57		dBc
f_{CLK}=140MHz ; f_{OUT}=5.04MHz		58		dBc
f_{CLK}=140MHz ; f_{OUT}=20.2MHz		52		dBc
f_{CLK}=140MHz ; f_{OUT}=40.4MHz		41		dBc
Double-Ended Output				
f_{CLK}=50MHz ; f_{OUT}=1.00MHz		70		dBc
f_{CLK}=50MHz ; f_{OUT}=2.51MHz		70		dBc
f_{CLK}=50MHz ; f_{OUT}=5.04MHz		65		dBc
f_{CLK}=50MHz ; f_{OUT}=20.2MHz		54		dBc
f_{CLK}=100MHz ; f_{OUT}=2.51MHz		67		dBc
f_{CLK}=100MHz ; f_{OUT}=5.04MHz		63		dBc
f_{CLK}=100MHz ; f_{OUT}=20.2MHz		58		dBc
f_{CLK}=100MHz ; f_{OUT}=40.4MHz		52		dBc
f_{CLK}=140MHz ; f_{OUT}=2.51MHz		62		dBc
f_{CLK}=140MHz ; f_{OUT}=5.04MHz		61		dBc
f_{CLK}=140MHz ; f_{OUT}=20.2MHz		55		dBc
f_{CLK}=140MHz ; f_{OUT}=40.4MHz		53		dBc
Spurious-Free Dynamic Range Within a Window				
Single-Ended Output				
f_{CLK}=50MHz ; f_{OUT}=1.00MHz ; 1MHZ Span		77		dBc
f_{CLK}=50MHz ; f_{OUT}=5.04MHz ; 2MHZ Span		73		dBc
f_{CLK}=140MHz ; f_{OUT}=5.04 ; 4MHZ Span		64		dBc
Double-Ended Output				
f_{CLK}=50MHz ; f_{OUT}=1.00MHz ; 1MHZ Span		74		dBc
f_{CLK}=50MHz ; f_{OUT}=5.04MHz ; 2MHZ Span		73		dBc
f_{CLK}=140MHz ; f_{OUT}=5.04 ; 4MHZ Span		60		dBc
Total Harmonic Distortion				
f_{CLK}=50MHz ; f_{OUT}=1.00MHz ; T_A=25℃		66		dBc
f_{CLK}=50MHz ; f_{OUT}=1.00MHz ; T_{MIN} to T_{MAX}		65		dBc
f_{CLK}=50MHz ; f_{OUT}=2.00MHz		64		dBc
f_{CLK}=100MHz ; f_{OUT}=2.00MHz		63		dBc
f_{CLK}=140MHz ; f_{OUT}=2.00MHz		55		dBc
DAC PERFORMANCE				
Glitch Impulse		10		pVs
DACu Crosstalk (crosstalk)		23		dB
Data Feedthrough		22		dB
Clock Feedthrough		33		dB

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5 V TIMING–SPECIFICATIONS（VAA=5V±5%，V_{REF}=1.235V，R_{SET}=560Ω，C_L=10pF, All specifications T_{MIN} to T_{MAX} unless otherwise noted, $T_{J\,MAX}$ = 110℃）

Parameter	Min	Typ	Max	Units	Conditions
Analog Output Delay, t_6		5.5		ns	
Analog Output Rise/Fall Time, t_7		1.0		ns	
Analog Output Transition Time, t_8		15		ns	
Analog Output Skew t_9		1	2	ns	
CLOCK CONTROL					
f_{CLK}	0.5		50	MHz	50MHz Grade
f_{CLK}	0.5		140	MHz	140MHz Grade
f_{CLK}	0.5		240	MHz	240MHz Grade
Data and Control Setup t_1	1.5			ns	
Data and Control Hold t_2	2.5			ns	
Clock Pulsewidth High t_4	1.875	1.1		ns	f_{MAX}=240MHz
Clock Pulsewidth Low t_5	1.875	1.25		ns	f_{MAX}=240MHz
Clock Pulsewidth High t_4	2.85			ns	f_{MAX}=140MHz
Clock Pulsewidth Low t_5	2.85			ns	f_{MAX}=140MHz
Clock Pulsewidth High t_4	8.0			ns	f_{MAX}=50MHz
Clock Pulsewidth Low t_5	8.0			ns	f_{MAX}=50MHz
Pipeline Delay , t_{PD}	1.0	1.0	1.0	Clock Cycles	
PSAVE Up Time, t_{10}		2	10	ns	

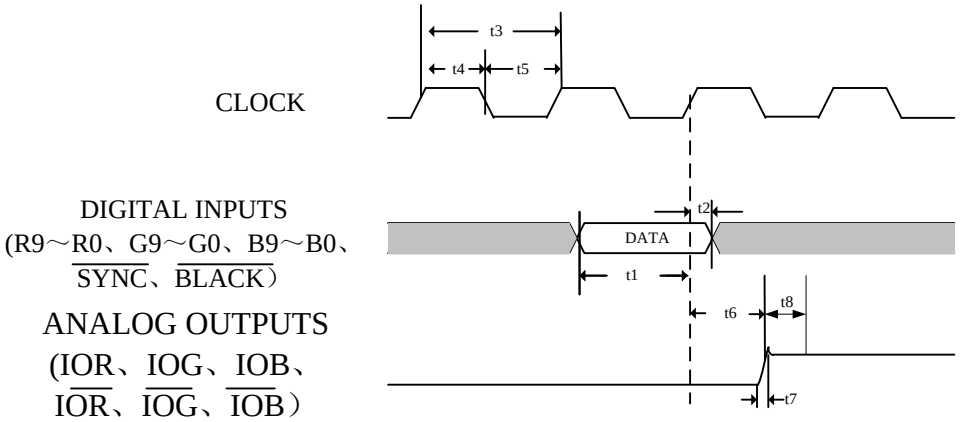

Figure 4. 5V Sequence Diagram

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3V SPECIFICATIONS（VAA=3V~3.6V, V_{REF}=1.235V, R_{SET}=560□, C_L=10pF, All specifications T_{MIN} to T_{MAX} unless otherwise noted, $T_{J\,MAX}$ = 110℃）

Parameter		Min	Typ	Max	Units	Test conditions
STATIC PERFORMANCE	Resolution (Each DAC)		10		Bits	Guaranteed Monotonic
	Integral Nonlinearity (INL)	-1	±0.4	+1	LSB	
	Differential Nonlinearity(DNL)	-1	±0.25	+1	LSB	
DIGITAL AND CONTROL INPUTS	Input High Voltage, V_{IH}	2			V	V_{IN}=0.0V 或V_{IN}=VDD
	Input Low Voltage, V_{IL}			0.8	V	
	Input Current, I_{IN}	-1		+1	uA	
	PSAVE Pull-Up Current		20		uA	
	Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS	Output Current	2.0		26.5	mA	Green DAC Sync=High
	Output Current	2.0		18.5	mA	R/G/B DAC Sync=Low
	DAC to DAC Matching		1.0	5	%	
	Output Compliance Range, V_{OC}	0		+1.4	V	
	Output Impedance, R_{OUT}		100		KΩ	
	Output Capacitance,C_{OUT}		10		pF	I_{OUT}=0mA
	Offset Error	-0.025		+0.025	%FSR	Test with DAC Output=0
	Gain Error2	-5.0		+5.0	%FSR	FSR=17.62mA
VOLTAGE REFERENCE (Ext. and Int.) Reference Range, VREF		1.12	1.235	1.35	V	
POWER DISSIPATION	Digital Supply Current		3.4	9	mA	f_{CLK}=50MHz
	Digital Supply Current		10.5	15	mA	f_{CLK}=140MHz
	Digital Supply Current		18	25	mA	f_{CLK}=240MHz
	Analog Supply Current		67	72	mA	R_{SET}=560□
	Analog Supply Current		8		mA	R_{SET}=4933□
	Standby Supply Current		2.1	5.0	mA	PSAVE=Low, Digital and Control Inputs at VDD
Power Supply Rejection Ratio			0.1	0.5	%	

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3V DYNAMIC SPECIFICATIONS(VAA=3V~3.6V，V_{REF}=1.235V，R_{SET}=560Ω，C_L=10pF, All specifications T_{MIN} to T_{MAX} unless otherwise noted, $T_{J\,MAX}$ = 110℃**)**

Parameter	Min	Typ	Max	Units
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist2				
Single-Ended Output				
f_{CLK}=50MHz；f_{OUT}=1.00MHz		67		dBc
f_{CLK}=50MHz；f_{OUT}=2.51MHz		67		dBc
f_{CLK}=50MHz；f_{OUT}=5.04MHz		63		dBc
f_{CLK}=50MHz；f_{OUT}=20.2MHz		55		dBc
f_{CLK}=100MHz；f_{OUT}=2.51MHz		62		dBc
f_{CLK}=100MHz；f_{OUT}=5.04MHz		60		dBc
f_{CLK}=100MHz；f_{OUT}=20.2MHz		54		dBc
f_{CLK}=100MHz；f_{OUT}=40.4MHz		48		dBc
f_{CLK}=140MHz；f_{OUT}=2.51MHz		57		dBc
f_{CLK}=140MHz；f_{OUT}=5.04MHz		58		dBc
f_{CLK}=140MHz；f_{OUT}=20.2MHz		52		dBc
f_{CLK}=140MHz；f_{OUT}=40.4MHz		41		dBc
Double-Ended Output				
f_{CLK}=50MHz；f_{OUT}=1.00MHz		70		dBc
f_{CLK}=50MHz；f_{OUT}=2.51MHz		70		dBc
f_{CLK}=50MHz；f_{OUT}=5.04MHz		65		dBc
f_{CLK}=50MHz；f_{OUT}=20.2MHz		54		dBc
f_{CLK}=100MHz；f_{OUT}=2.51MHz		67		dBc
f_{CLK}=100MHz；f_{OUT}=5.04MHz		63		dBc
f_{CLK}=100MHz；f_{OUT}=20.2MHz		58		dBc
f_{CLK}=100MHz；f_{OUT}=40.4MHz		52		dBc
f_{CLK}=140MHz；f_{OUT}=2.51MHz		62		dBc
f_{CLK}=140MHz；f_{OUT}=5.04MHz		61		dBc
f_{CLK}=140MHz；f_{OUT}=20.2MHz		55		dBc
f_{CLK}=140MHz；f_{OUT}=40.4MHz		53		dBc
Spurious-Free Dynamic Range Within a Window				
Single-Ended Output				
f_{CLK}=50MHz；f_{OUT}=1.00MHz；1MHZ Span		77		dBc
f_{CLK}=50MHz；f_{OUT}=5.04MHz；2MHZ Span		73		dBc
f_{CLK}=140MHz；f_{OUT}=5.04；4MHZ Span		64		dBc
Double-Ended Output				
f_{CLK}=50MHz；f_{OUT}=1.00MHz；1MHZ Span		74		dBc
f_{CLK}=50MHz；f_{OUT}=5.04MHz；2MHZ Span		73		dBc
f_{CLK}=140MHz；f_{OUT}=5.04；4MHZ Span		60		dBc
Total Harmonic Distortion				

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Parameter	Min	Typ	Max	Units
f_{CLK}=50MHz ; f_{OUT}=1.00MHz ; T_A=25℃		66		dBc
f_{CLK}=50MHz ; f_{OUT}=1.00MHz ; T_{MIN} to T_{MAX}		65		dBc
f_{CLK}=50MHz ; f_{OUT}=2.00MHz		64		dBc
f_{CLK}=100MHz ; f_{OUT}=2.00MHz		63		dBc
f_{CLK}=140MHz ; f_{OUT}=2.00MHz		55		dBc
DAC PERFORMANCE				
Glitch Impulse		10		pVs
DACu Crosstalk (crosstalk)		23		dB
Data Feedthrough		22		dB
Clock Feedthrough		33		dB

3V TIMING–SPECIFICATIONS (VAA=3V~3.6V, V_{REF}=1.235V, R_{SET}=560□, C_L=10pF, All specifications T_{MIN} to T_{MAX} unless otherwise noted, $T_{J\ MAX}$ = 110℃)

Parameter	Min	Typ	Max	Units	Conditions
Analog Output Delay, t_6		7.5		ns	
Analog Output Rise/Fall Time, t_7		1.0		ns	
Analog Output Transition Time, t_8		15		ns	
Analog Output Skew t_9		1	2	ns	
CLOCK CONTROL					
f_{CLK}	0.5		50	MHz	50MHz Grade
f_{CLK}	0.5		140	MHz	140MHz Grade
f_{CLK}	0.5		240	MHz	240MHz Grade
Data and Control Setup t_1	1.5			ns	
Data and Control Hold t_2	2.5			ns	
Clock Pulsewidth High t_4	1.875	1.1		ns	f_{MAX}=240MHz
Clock Pulsewidth Low t_5	1.875	1.25		ns	f_{MAX}=240MHz
Clock Pulsewidth High t_4	2.85			ns	f_{MAX}=140MHz
Clock Pulsewidth Low t_5	2.85			ns	f_{MAX}=140MHz
Clock Pulsewidth High t_4	8.0			ns	f_{MAX}=50MHz
Clock Pulsewidth Low t_5	8.0			ns	f_{MAX}=50MHz
Pipeline Delay , t_{PD}	1.0	1.0	1.0	Clock Cycles	
PSAVE Up Time, t_{10}		2	10	ns	

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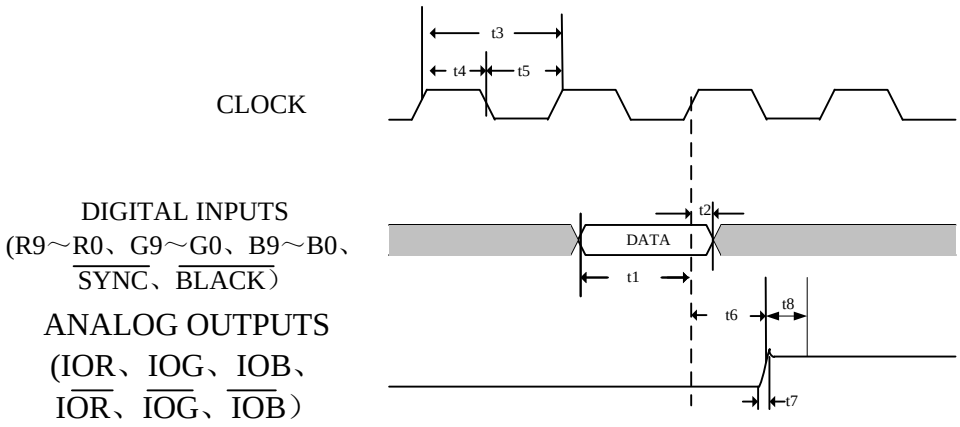

Figure 5. 3.3V Sequence Diagram

CIRCUIT DESCRIPTION

The CS7123 contains three 10-bit D/A converters, with three input channels, each containing a 10-bit register.

Digital inputs

Thirty bits of pixel data (color information) R0–R9, G0–G9 and B0–B9 are latched into the device on the rising edge of each clock cycle. This data is presented to the three 10-bit DACs and then converted to three analog (RGB) output waveforms. See Figure 6.

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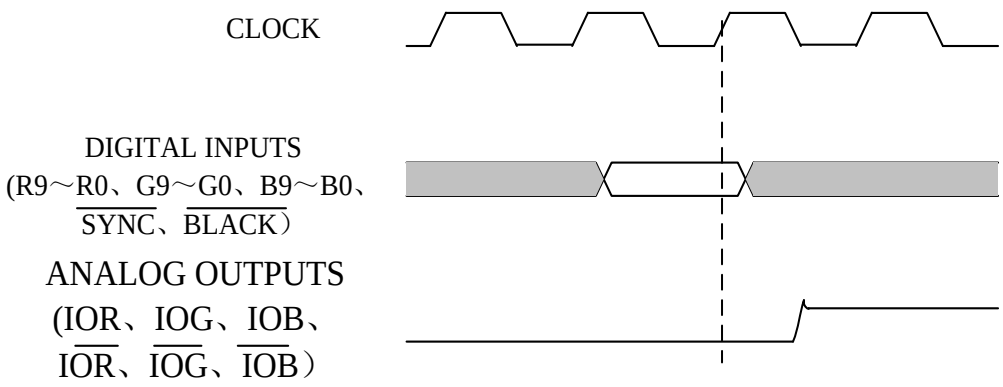

Figure 6. CS7123 Sequence Diagram

The CS7123 has two additional control signals that are latched to the analog video outputs in a similar fashion. BLANK and SYNC are each latched on the rising edge of CLOCK to maintain synchronization with the pixel data stream.

The $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ functions allow for the encoding of these video synchronization signals onto the RGB video output. This is done by adding appropriately weighted current sources to the analog outputs, as determined by the logic levels on the BLANK and SYNC digital inputs.

Figure 7 shows the analog output, RGB video waveform of the CS7123. The influence of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ on the analog video waveform is illustrated. Table I details the resultant effect on the analog outputs of $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$.

All these digital inputs are specified to accept TTL logic levels.

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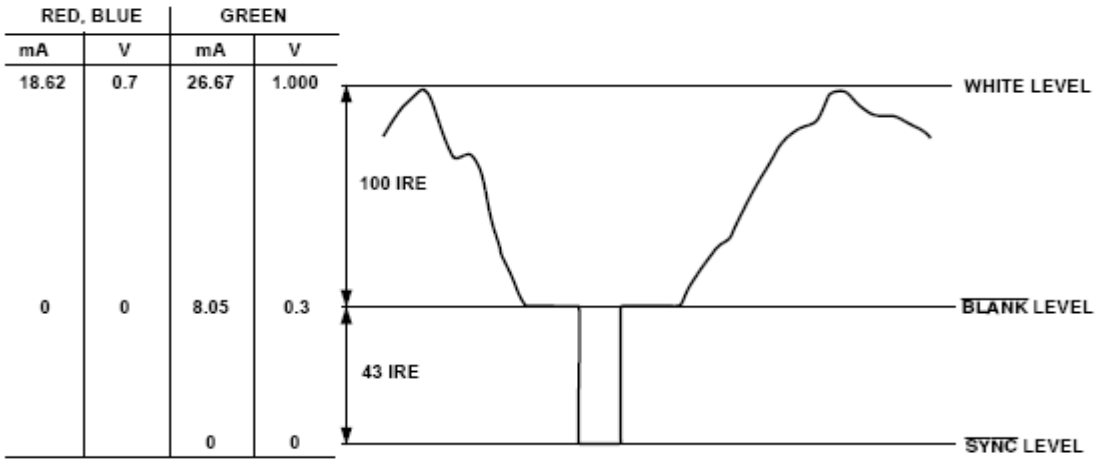

NOTES:
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75V LOAD.
2. VREF = 1.235V, RSET = 530V.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 7. RGB video Output waveform

Table 1. Video Output Truth Table(（R_{SET}=530□，R_{LOAD}=37.5□）

Description	IOG(mA)	$\overline{IOG}$(mA)	IOB/IOR	$\overline{IOB}$ / $\overline{IOR}$	$\overline{SYNC}$	$\overline{BLANK}$	DAC data inputs
WHITE LEVEL	26.67	0	18.62	0	1	1	3FFH
VIDEO	Video+ 8.05	18.62- Video	Video	18.62- Video	1	1	Data
VIDEO to BLANK	Video	18.62- Video	Video	18.62- Video	0	1	Data
BLACK LEVEL	8.05	18.62	0	18.62	1	1	000H
BLACK to BLANK	0	18.62	0	18.62	0	1	000H
BLANK LEVEL	8.05	18.62	0	18.62	1	0	xxxH
SYNC LEVEL	0	18.62	0	18.62	0	0	xxxH

Clock Input

The CLOCK input of the CS7123 is typically the pixel clock rate of the system. It is also known as the dot rate. The dot rate, and hence the required CLOCK frequency, will be determined by the on-screen resolution, according to the following equation:

Dot Rate =(Horz Res)×(Vert Res) ×(Refresh Rate)/(Rerace Factor)
Horiz Res = Number of Pixels/line.(Line)
Vert Res = Number of Pixels/Frame.(Frame)
Refresh Rate = Horizontal Scan Rate. This is the rate at which the screen must be refreshed, typically 60 Hz for a noninterlaced system or 30 Hz for an interlaced system.
Retrace Factor = Total Blank Time Factor. This takes into account that the display is blanked for a certain fraction of the total duration of each frame (e.g., 0.8).

Therefore, if we have a graphics system with a 1024 × 1024 resolution, a noninterlaced 60Hz refresh rate and a retrace factor of 0.8, then:

Dot Rate = 1024×1024×60/0.8
= 76.8MHz

The required CLOCK frequency is thus 78.6 MHz.

All video data and control inputs are latched into the CS7123 on the rising edge of CLOCK, as previously described in the Digital Inputs section. It is recommended that the CLOCK input to the CS7123 be driven by a TTL buffer (e.g., 74F244).

Video Synchronization and Control

The CS7123 has a single composite sync ($\overline{\text{SYNC}}$) input con-trol. Many graphics processors and CRT controllers have the ability of generating horizontal sync (HSYNC), vertical sync (VSYNC) and composite $\overline{\text{SYNC}}$.

In a graphics system that does not automatically generate a composite $\overline{\text{SYNC}}$ signal, the inclusion of some additional logic circuitry will enable the generation of a composite $\overline{\text{SYNC}}$ signal.

The sync current is internally connected directly to the IOG output, thus encoding video synchronization information onto the green video channel. If it is not required to encode sync information onto the CS7123, the SYNC input should be tied to logic low.

Reference Input

The CS7123 contains an onboard voltage reference. The V_{REF} pin is normally terminated to V_{AA} through a 0.1 µF capacitor. Alternatively, the part could, if required, be overdriven by an external 1.23 V reference (AD1580).

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A resistance R_{SET} connected between the R_{SET} pin and GND determines the amplitude of the output video level according to Equations for the CS7123:

$IOG = 11.445 \times V_{REF} / R_{SET}$

$IOB,IOR = 7.992 \times V_{REF} / R_{SET}$

D/A Converters

The CS7123 contains three matched 10-bit D/A converters. The DACs are designed using an advanced, high speed, seg-mented architecture. The bit currents corresponding to each digital input are routed to either the analog output (bit = “1”) or GND (bit = “0”) by a sophisticated decoding scheme. As all this circuitry is on one monolithic device, matching between the three DACs is optimized. As well as matching, the use of identi-cal current sources in a monolithic design guarantees monoto-nicity and low glitch. The onboard operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Analog Outputs

The CS7123 has three analog outputs, corresponding to the red, green and blue video signals. The red, green and blue analog outputs of the CS7123 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω coaxial cable. Figure 8 shows the required configuration for each of the three RGB outputs con-nected into a doubly terminated 75Ω load. This arrangement will develop RS-343A video output voltage levels across a 75Ω monitor.

A suggested method of driving RS-170 video levels into a 75Ω monitor is shown in Figure 9. The output current levels of the DACs remain unchanged, but the source termination resistance, $Z_{S,}$ on each of the three DAC outputs is increased from 75Ωto 150Ω.

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an Application Note entitled “Video Formats & Required Load Terminations” available from Analog Devices.

Figure 7 shows the video waveforms associated with the three RGB outputs driving the doubly terminated 75Ω load of Figure 8. As well as the gray scale levels, Black Level to White Level, the diagram also shows the contributions of SYNC and BLANK for the CS7123. These control inputs add appropriately weighted currents to the analog outputs,

producing the spe-cific output level requirements for video applications.

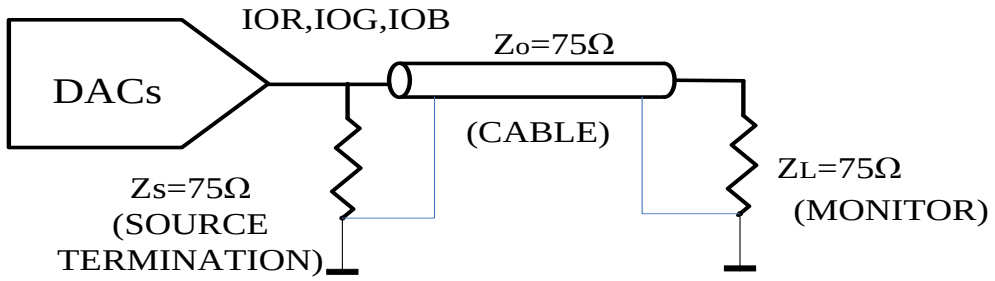

Figure 8 Analog Output Termination For RS-343A

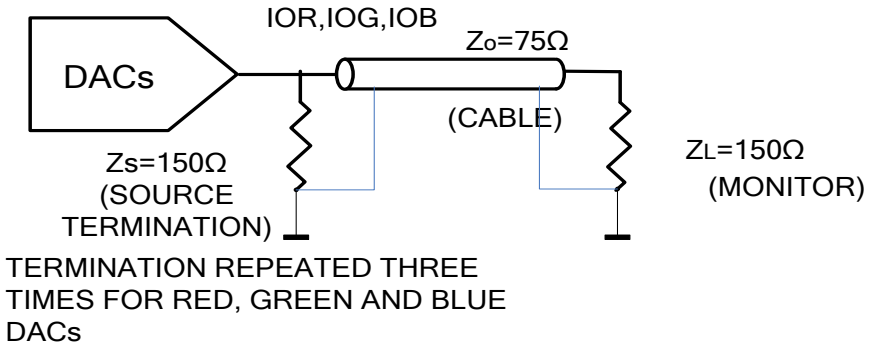

Figure 9. Analog Output Termination For RS-170

Gray Scale Operation

The CS7123 can be used for stand-alone, gray scale (mono-chrome) or composite video applications (i.e., only one channel used for video information). Any one of the three channels, RED, GREEN or BLUE can be used to input the digital video data. The two unused video data channels should be tied to logical zero. The unused analog outputs should be terminated with the same load as that for the used channel. In other words, if the red channel is used and IOR is terminated with a doubly terminated 75Ω load (37.5Ω), IOB and IOG should be termi-nated with 37.5 Ω resistors.

Video Output Buffers

The CS7123 is specified to drive transmission line loads, as are most monitors rated. The analog output configurations to drive such loads are described in the Analog Interface

section .However, in some applications it may be required to drive long “transmission line” cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. The inclusion of output buffers will compensate for some cable distortion. Buffers with large full power bandwidths and gains between two and four will be required. These buffers will also need to be able to sup-ply sufficient current over the complete output voltage swing. Analog Devices produces a range of suitable op amps for such applications. These include the AD84x series of monolithic op amps. In very high frequency applications (80 MHz), the AD9617 is recommended. More information on line driver buffering circuits is given in the relevant op amp data sheets.

Use of buffer amplifiers also allows implementation of other video standards besides RS-343A and RS-170. Altering the gain components of the buffer circuit will result in any desired video level.

PC Board Layout Considerations

The CS7123 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the CS7123, it is imperative that great care be given to the PC board layout. Figure 25 shows a recommended connection diagram for the CS7123.

The layout should be optimized for lowest noise on the CS7123 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should by minimized to minimize inductive ringing.

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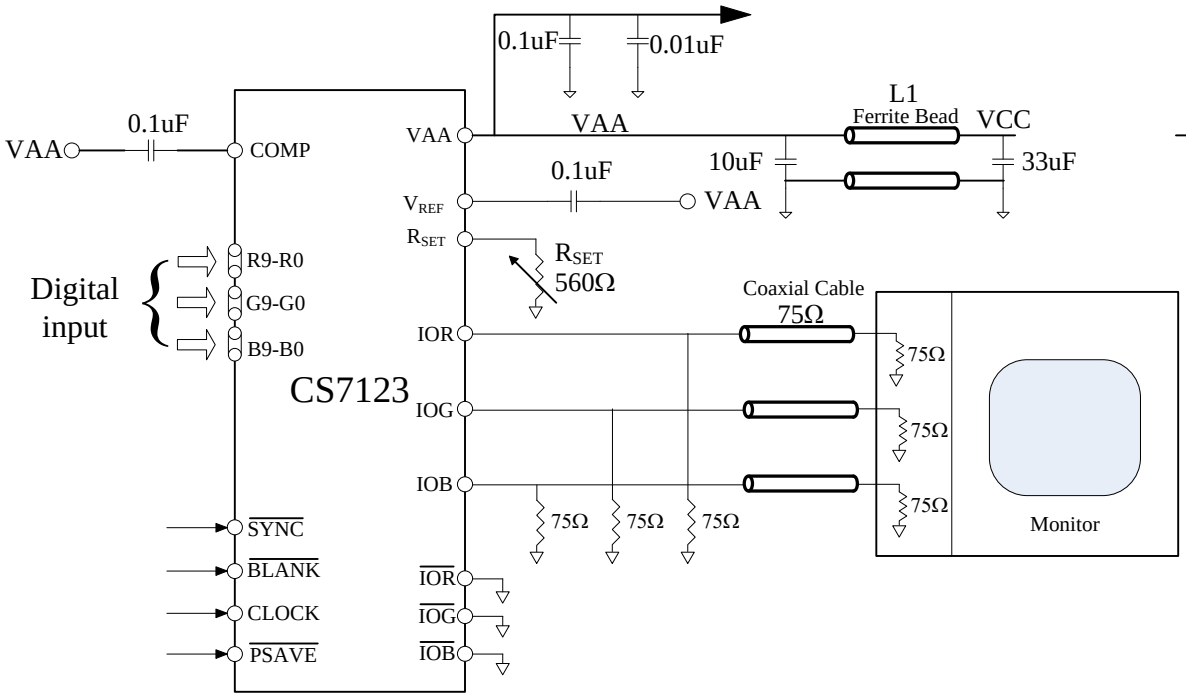

Figure 10. Typital Connection Diagram

Ground Planes

The CS7123 and associated analog circuitry, should have a separate ground plane referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 25. This bead should be located as close as possible (within three inches) to the CS7123.

The analog ground plane should encompass all CS7123 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the CS7123.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry

and one for digital circuitry. The analog power plane should encompass the CS7123 (V_{AA}) and all associated analog circuitry. This power plane should be con-nected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figure 25. This bead should be located within three inches of the CS7123.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all CS7123 power pins, voltage reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors .

Optimum performance is achieved by the use of 0.1 μF ceramic capacitors. Each of the two groups of V_{AA} should be individually decoupled to ground. This should be done by placing the ca-pacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the CS7123 contains cir-cuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power sup-ply noise. A dc power supply filter (Murata BNX002) will pro-vide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the CS7123 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the CS7123 should be avoided to minimize noise pickup.

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Analog Signal Interconnect

The CS7123 should be located as close as possible to the reflections. output connectors thus minimizing noise pickup and reflections due to impedence mismatch.

The video output signals should overlay the ground plane and System for Reduced EMI." This application note is available not the analog power plane, thereby maximizing the high fre-from Analog Devices, publication no. E1309–15–10/89. quency power supply rejection.

For optimum performance, the analog outputs should each have should be connected to the regular PCB power plane (V_{CC}) and a source termination resistance to ground of 75 Ω (doubly not the analog power plane. terminated 75 Ω configuration). This termination resistance Analog Signal Interconnect should be as close as possible to the CS7123 to minimize reflections.

Additional information on PCB design is available in an application note entitled "Design and Layout of a Video Graphics

The video output signals should overlay the ground plane and System for Reduced EMI." This application note is available from Analog Devices, publication no. E1309–15–10/8

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