



CS830 A4RD

General Description:

CS830 A4RD, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-252, which accords with the RoHS standard.

Features:

- l **Fast Switching**
- l **ESD Improved Capability**
- l **Low Gate Charge** (Typical Data:14.5nC)
- l **Low Reverse transfer capacitances**(Typical:7.5pF)
- l **100% Single Pulse avalanche energy Test**

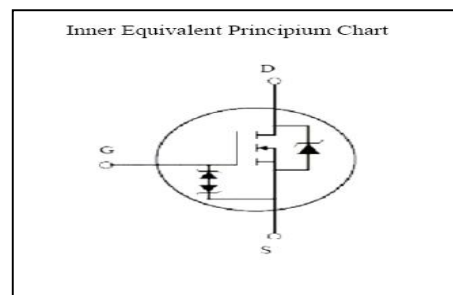
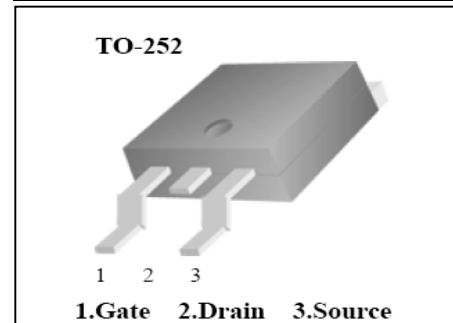
Applications:

Power switch circuit of adaptor and charger.

Absolute (Tc= 25°C unless otherwise specified):

Symbol	Parameter	Rating	Units
V _{DSS}	Drain-to-Source Voltage	500	V
I _D	Continuous Drain Current	5	A
	Continuous Drain Current T _C = 100 °C	3.4	A
I _{DM} ^{a1}	Pulsed Drain Current	20	A
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS} ^{a2}	Single Pulse Avalanche Energy	200	mJ
E _{AR} ^{a1}	Avalanche Energy ,Repetitive	30	mJ
I _{AR} ^{a1}	Avalanche Current	2.5	A
dv/dt ^{a3}	Peak Diode Recovery dv/dt	5.0	V/ns
P _D	Power Dissipation	75	W
	Derating Factor above 25°C	0.6	W/°C
V _{ESD(G-S)}	Gate source ESD (HBM-C= 100pF, R=1.5kΩ)	3000	V
T _J , T _{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	°C
T _L	Maximum Temperature for Soldering	300	°C

V _{DSS}	500	V
I _D	5	A
P _D (T _C =25°C)	75	W
R _{DS(ON)Typ}	1.25	Ω



Electrical Characteristics (Tc= 25°C unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Unit s
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	500	--	--	V
ΔBV _{DSS} /ΔT _J	Bvdss Temperature Coefficient	ID=250uA, Reference 25°C	--	0.67	--	V/°C
I _{DSS}	Drain to Source Leakage Current	V _{DS} =500V, V _{GS} = 0V, T _a = 25°C	--	--	1	μA
		V _{DS} =400V, V _{GS} = 0V, T _a = 125°C	--	--	100	μA
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} =+20V	--	--	10	μA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} =-20V	--	--	-10	μA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R _{DS(ON)}	Drain-to-Source On-Resistance	V _{GS} =10V, I _D =2.5A	--	1.25	1.5	Ω
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.0		4.0	V
Pulse width tp≤300μs, δ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g _{fs}	Forward Trans conductance	V _{DS} =15V, I _D =2.5A		4	--	S
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz	--	540		pF
C _{oss}	Output Capacitance		--	68		
C _{rss}	Reverse Transfer Capacitance		--	7.5		

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
t _{d(ON)}	Turn-on Delay Time	I _D =5A V _{DD} = 250V R _G =9.1Ω	--	9	--	ns
t _r	Rise Time		--	11	--	
t _{d(OFF)}	Turn-Off Delay Time		--	29	--	
t _f	Fall Time		--	16	--	
Q _g	Total Gate Charge	I _D =5A V _{DD} =250V V _{GS} = 10V	--	14.5		nC
Q _{gs}	Gate to Source Charge		--	3		
Q _{gd}	Gate to Drain (“Miller”)Charge		--	6.5		

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	5	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	20	A
V_{SD}	Diode Forward Voltage	$I_S=5.0A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=5.0A, T_J = 25^\circ C$	--	388	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt=100A/us, V_{GS}=0V$	--	1720	--	nC
Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	1.67	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	62.5	$^\circ C/W$

Gate-source Zener diode						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{GSO}	Gate-source breakdown voltage	$I_{GS} = \pm 1mA (Open Drain)$	30			V
<p>The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.</p>						

^{a1}: Repetitive rating; pulse width limited by maximum junction temperature

^{a2}: $L=10mH, I_D=6.3A, Start T_J=25^\circ C$

^{a3}: $I_{SD}=5A, di/dt \leq 100A/us, V_{DD} \leq BV_{DS}, Start T_J=25^\circ C$

Characteristics Curve:

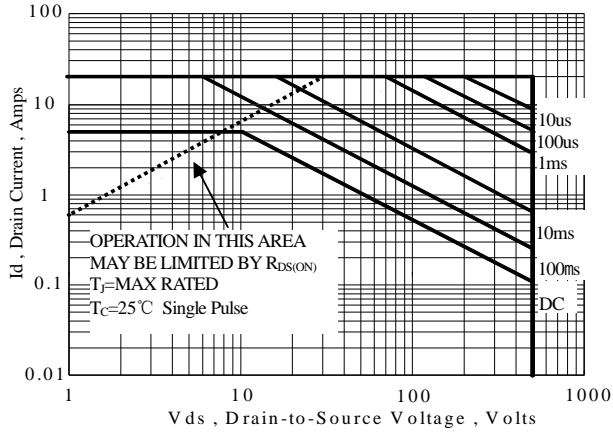


Figure 1 Maximum Forward Bias Safe Operating Area

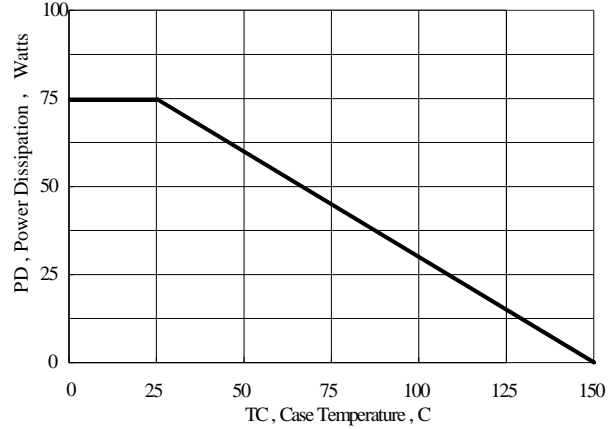


Figure 2 Maximum Power Dissipation vs Case Temperature

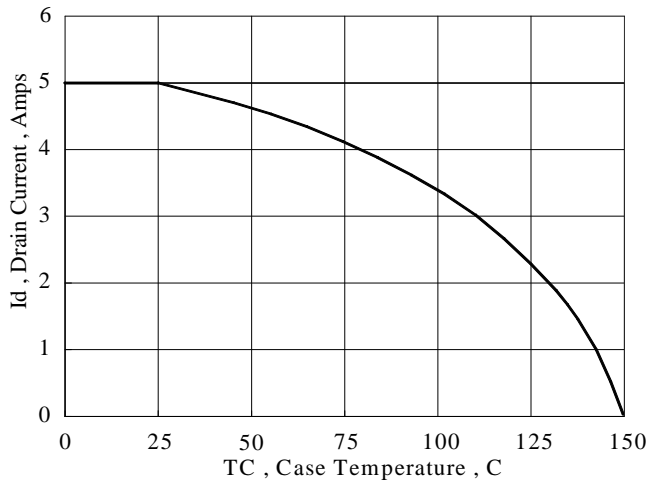


Figure 3 Maximum Continuous Drain Current vs Case Temperature

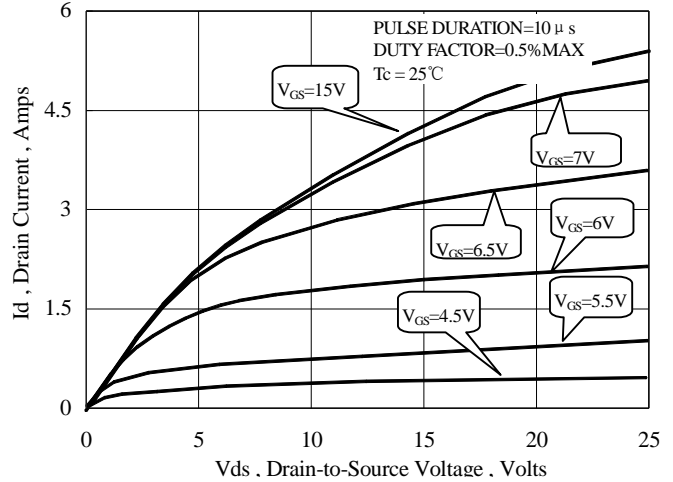


Figure 4 Typical Output Characteristics

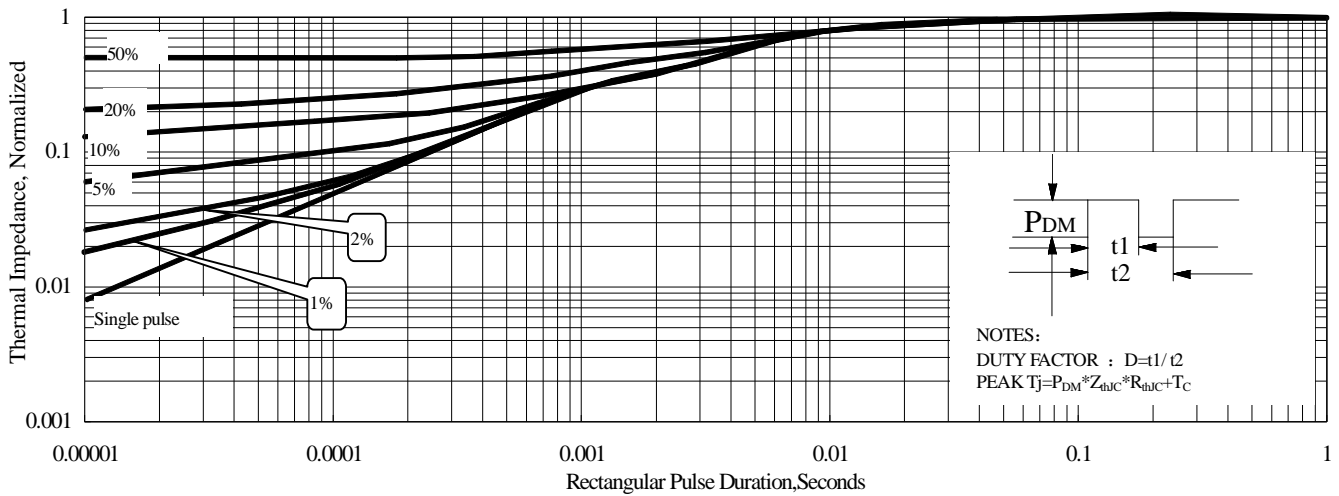


Figure 5 Maximum Effective Thermal Impedance, Junction to Case

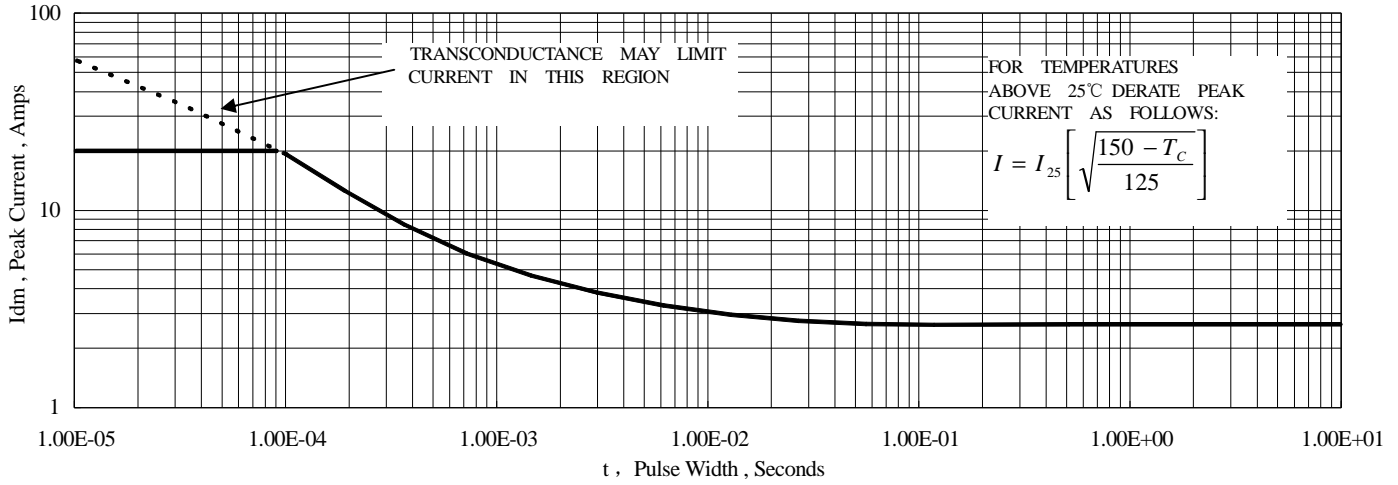


Figure 6 Maximum Peak Current Capability

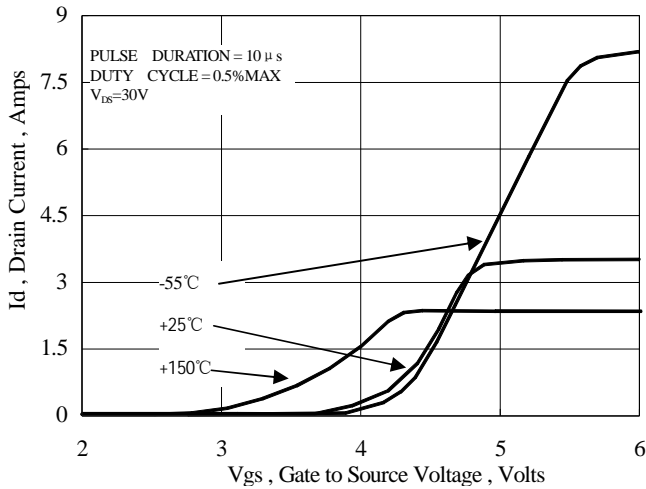


Figure 7 Typical Transfer Characteristics

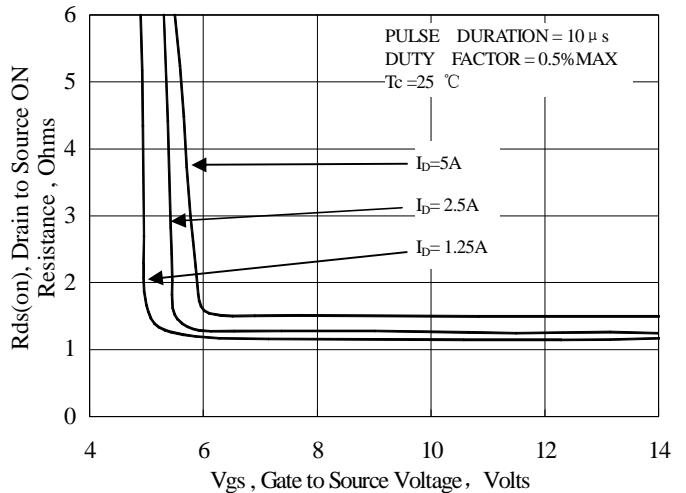


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

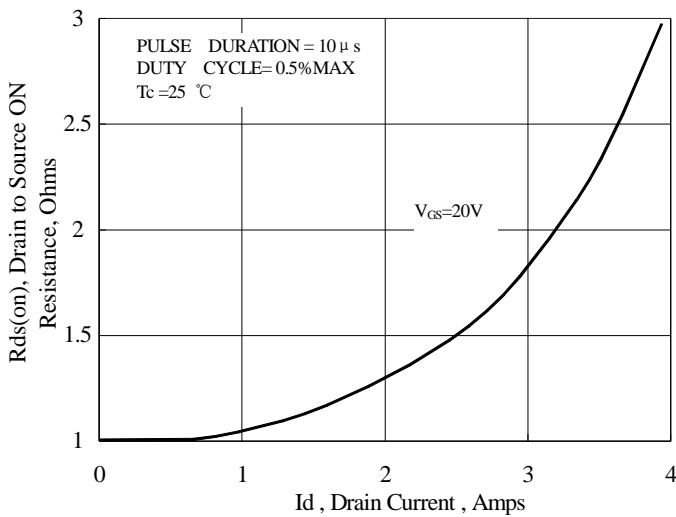


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

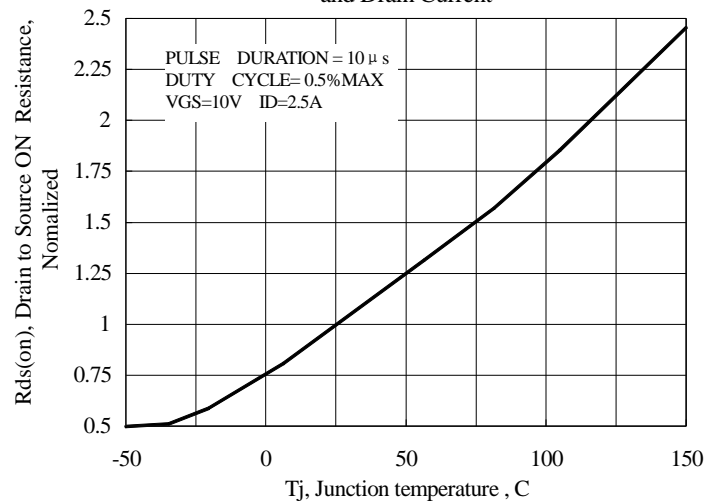


Figure 10 Typical Drain to Source on Resistance vs Junction Temperature

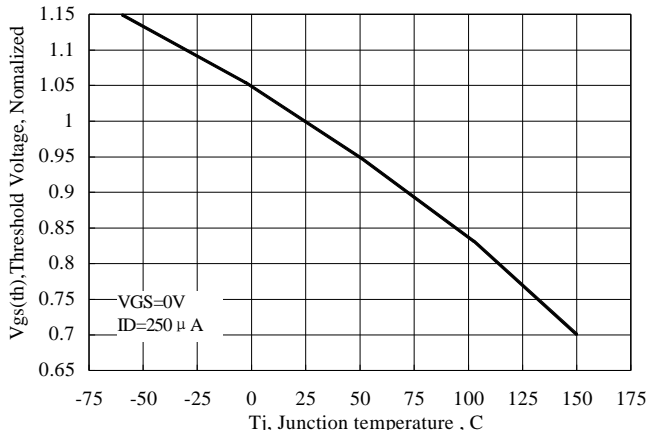


Figure 11 Typical Theshold Voltage vs Junction Temperature

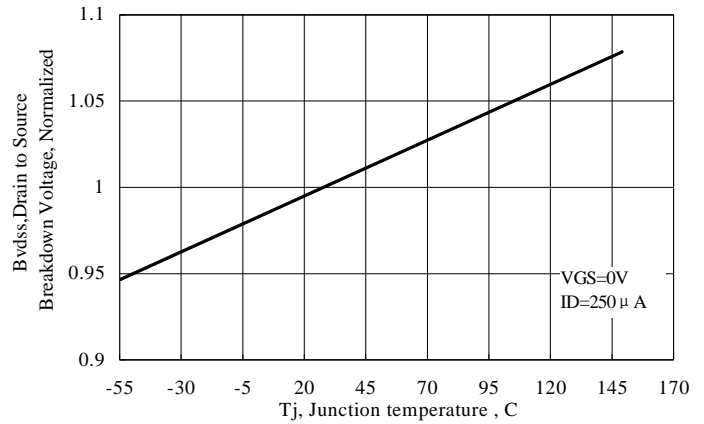


Figure 12 Typical Breakdown Voltage vs Junction Temperature

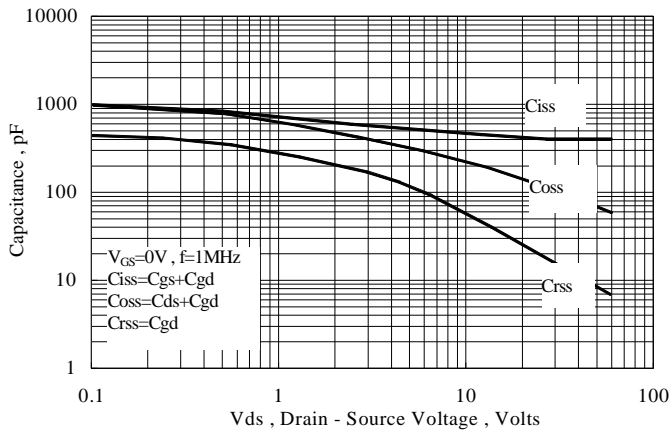


Figure 13 Typical Capacitance vs Drain to Source Voltage

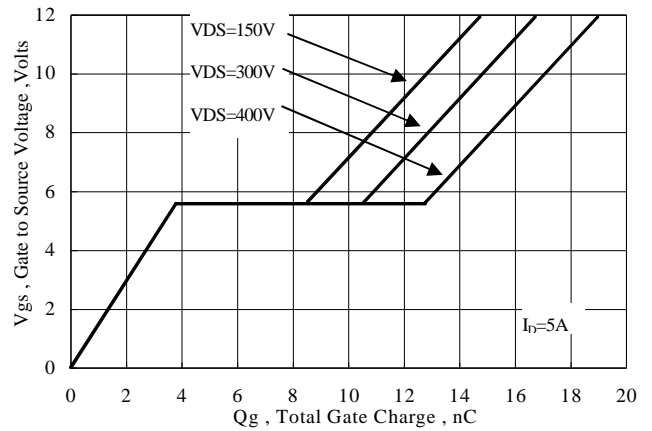


Figure 14 Typical Gate Charge vs Gate to Source Voltage

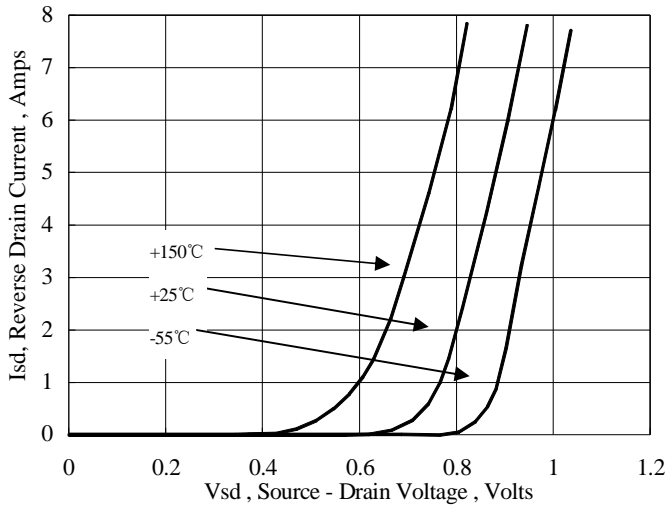


Figure 15 Typical Body Diode Transfer Characteristics

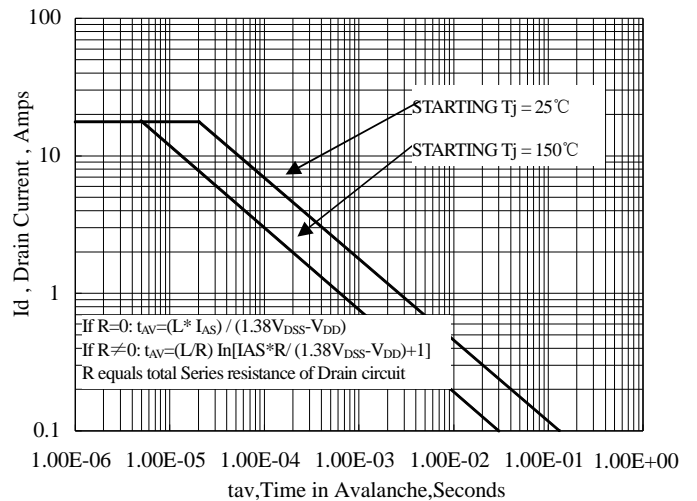


Figure 16 Unclamped Inductive Switching Capability

Test Circuit and Waveform

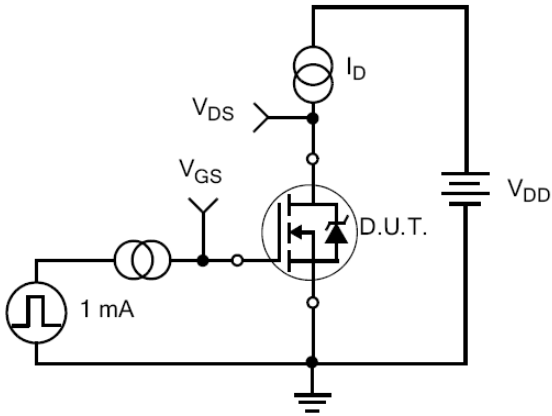


Figure 17. Gate Charge Test Circuit

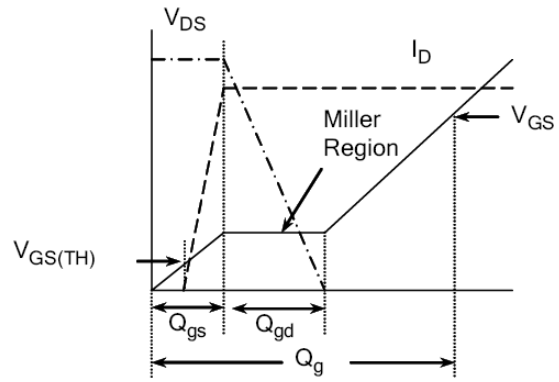


Figure 18. Gate Charge Waveform

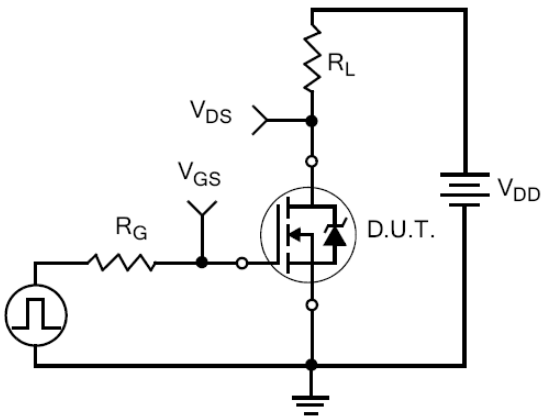


Figure 19. Resistive Switching Test Circuit

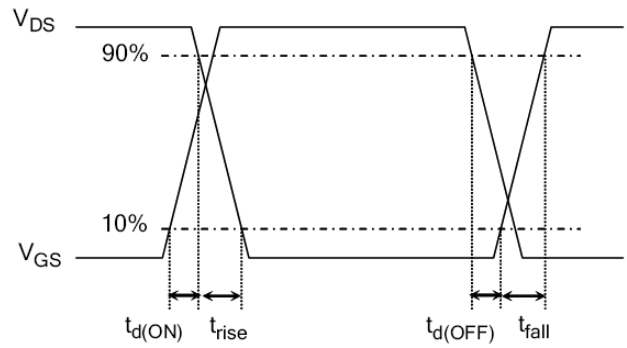


Figure 20. Resistive Switching Waveforms

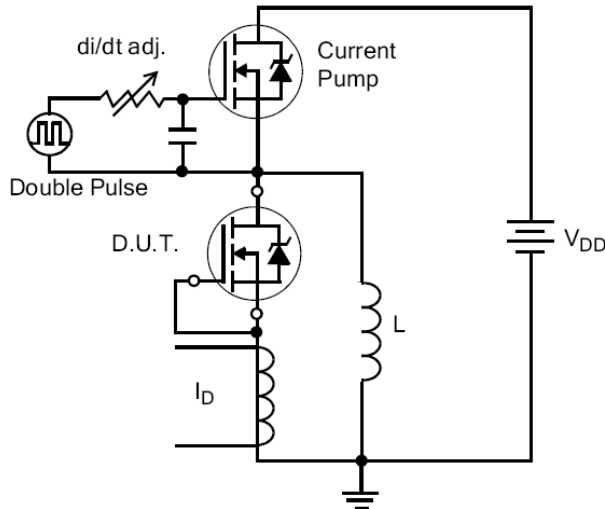


Figure 21. Diode Reverse Recovery Test Circuit

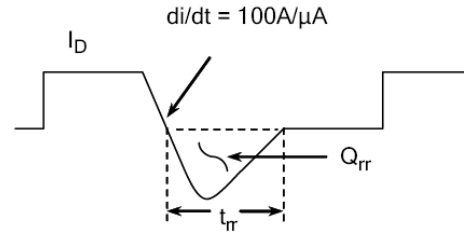


Figure 22. Diode Reverse Recovery Waveform

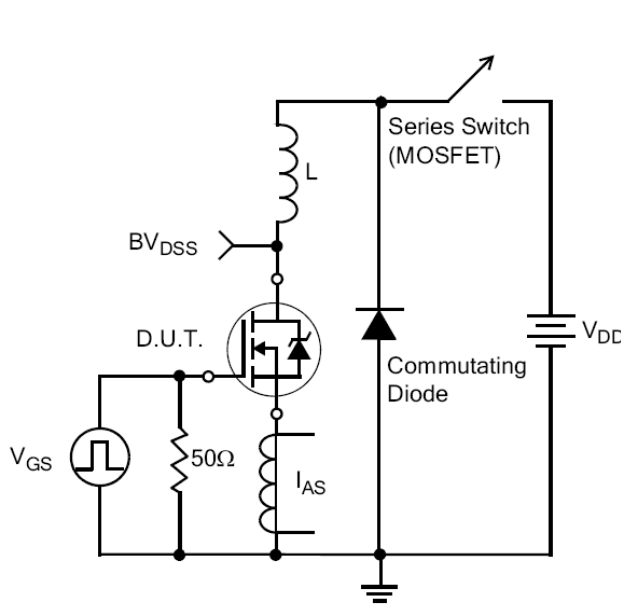


Figure 23. Unclamped Inductive Switching Test Circuit

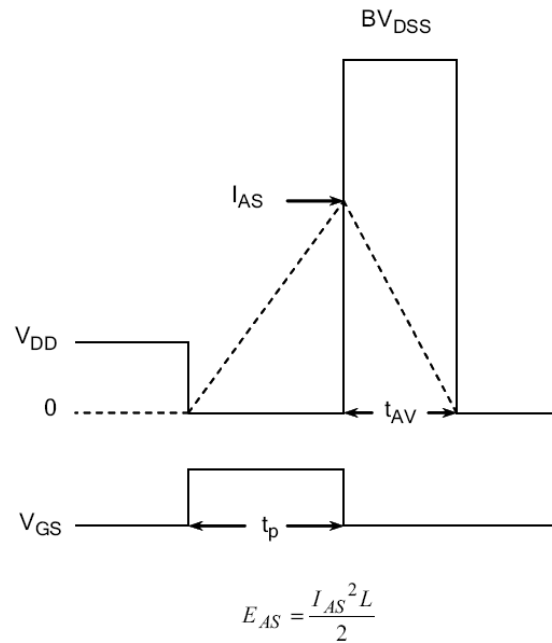
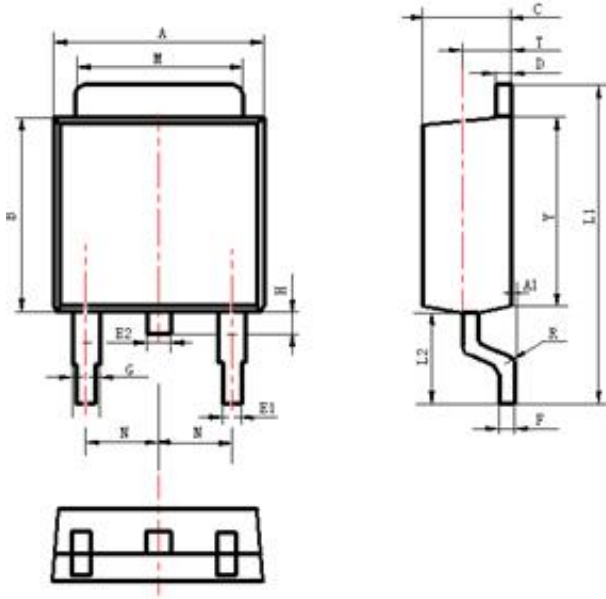


Figure 24. Unclamped Inductive Switching Waveforms

Package Information:



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.13
B	5.70	6.30
C	2.10	2.50
D	0.30	0.60
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.00
L1	9.60	10.30
L2	2.70	3.10
H	0.60	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package

