Coaxial Transceiver Interface

Features

- Implemented in High Voltage, Low Power CMOS
- Compatible with National's DP8392A
- CS83C92C is Compliant With ISO/IEEE 802.3 10Base5 (Ethernet) and 10Base2 (Cheapernet)
- All Transceiver Functions Integrated Except Signal and Power Isolation
- Squelch Circuitry Rejects Noise
- CD Heartbeat Externally Selectable Allowing Operation with IEEE 802.3 Compatible Repeaters
- Receive & Transmit Mode Collision Detection
- Standard 16-pin DIP Package & 28 pin PLCC

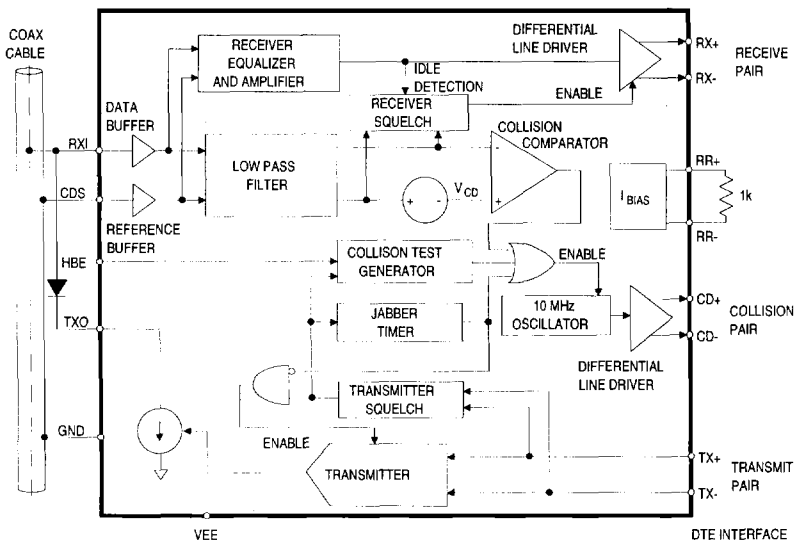
General Description

The CS83C92 Ethernet Transceiver interfaces an Ethernet or Cheapernet Local Area Network (LAN) to a LAN Adapter board, and may be located up to 50 meters from the station equipment. The Transceiver operates with the Crystal LAN components CS8005 Ethernet Data Link Controller and the CS8023A Manchester Code Converter. The CS83C92A is fully compatible with the DP8392A but the CS83C92A is built in CMOS technology (hence the 83"C"92). The CS83C92C is a higher performance grade which is compliant with IEEE 802.3 specifications.

For Ethernet applications, the CS83C92 is mounted on the COAX cable, and connects to the station equipment via an AUI cable. In a Cheapernet network, the CS83C92 is usually mounted on the LAN adapter card in the station equipment where it connects to the thin COAX through a BNC connector.

ORDERING INFORMATION:

CS83C92A-CP	PDIP	CS83C92C-CP	PDIP
CS83C92A-CL	PLCC	CS83C92C-CL	PLCC



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to ground)	VEE	-	-12.0	V
Package Power Rating at 25°C (Note 1)	P_P	-	3.5	W
Input Voltage (All pins except RXI)	V_{IN}	GND + 0.3	VEE - 0.3	V
Input Voltage on RXI	V_{IN}	GND + 0.3	-12	V
I/O Current (RXI, RR+, TX+, TX-, CDS, HBE)	I_{OUT}	-	±10	mA
(TXO)		-	+10 / -100	mA
(Note 2) (CD+, CD-, RX+, RX-)		-	+40 / -10	mA
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	-65	150	°C
ESD Protection (All pins)		1000	-	V

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Plastic DIP package only, package is PC board mounted. Derate at the rate of 28.6 mW/°C.
2. Transient currents of up to 200mA will not cause SCR latch-up.

CS83C92A ELECTRICAL CHARACTERISTICS (T_A = 0° to 70°C, VEE = -9.0V ±5%, GND = 0V, CD±, RX± pull downs = 510Ω)

Parameter	Symbol	Min	Typ	Max	Units
Recommended Supply Voltage	VEE	-	-9.0	-	V
Supply Current (V_{EE} to GND) Nontransmitting	I_{EE}	-	-55	-70	mA
Transmitting		-	-100	-120	mA
Receiver Input Bias Current (RXI)	I_{RXI}	-2	-	+25	µA
Transmitter Output DC Current (TXO)	I_{TDC}	37	41	45	mA
Transmitter Output AC Current (TXO)	I_{TAC}	±28	-	I_{TDC}	mA
Collision Threshold (Receive Mode)	V_{CD}	-1.45	-1.53	-1.58	V
Differential Output Voltage (RX±, CD±) (Note 3)	V_{OD}	±475	-	±1200	mV
DC Common Mode Output Voltage (RX±, CD±) (Note 4)	V_{OC}	-	-2.0	-	V
Idle State Differential Offset Voltage (RX±, CD±)	V_{OB}	-	-	±40	mV
Transmitter Squelch Threshold (TX±) (Note 5)	V_{TS}	-175	-225	-300	mV
RXI Capacitance	C_X	-	1.2	-	pF
Shunt Resistance - Nontransmitting (RXI)	R_{RXI}	100	-	-	kΩ
Shunt Resistance - Transmitting	R_{TXO}	10	-	-	kΩ

Notes: 3. Improved Spec. as required to meet ISO/IEEE 802.3 specifications.
4. V_{OC} has no impact on system performance since twisted pairs are transformer isolated.
5. For a minimum pulse width of ≥ 40 ns.

2

CS83C92C ELECTRICAL CHARACTERISTICS (T_A = 0° to 70°C, VEE = -9.0V ±5%, GND = 0V, CD±, RX± pull downs = 510Ω)

Parameter		Symbol	Min	Typ	Max	Units
Recommended Supply Voltage		VEE	-	-9.0	-	V
Supply Current (V_{EE} to GND)	Nontransmitting	I_{EE}	-	-55	-65	mA
	Transmitting		-	-100	-120	mA
Receiver Input Bias Current (RXI)		I_{RXI}	-2	-	+25	µA
Transmitter Output DC Current (TXO)		I_{TDC}	37	41	45	mA
Transmitter Output AC Current (TXO)		I_{TAC}	±28	-	I_{TDC}	mA
Collision Threshold (Receive Mode)		V_{CD}	-1.45	-1.53	-1.58	V
Differential Output Voltage (RX±, CD±)	(Note 3)	V_{OD}	±550	-	±1200	mV
DC Common Mode Output Voltage (RX±, CD±)	(Note 4)	V_{OC}	-	-2.0	-	V
Idle State Differential Offset Voltage (RX±, CD±)		V_{OB}	-	-	±40	mV
Transmitter Squelch Threshold (TX±)	(Note 5)	V_{TS}	-175	-225	-300	mV
Tap Capacitance	(Note 6)	C_X	-	1.2	4	pF
Shunt Resistance - Nontransmitting (RXI)		R_{RXI}	100	-	-	kΩ
Shunt Resistance - Transmitting		R_{TXO}	10	-	-	kΩ
Current Sink Limit (-10 V on coax)	(Notes 3, 6)	It_{10}	-	-	±250	mA
Harmonic Content Relative to Fundamental	(Note 7)					
2nd and 3rd Harmonics		-20	-	-	-	dB
4th and 5th Harmonics		-30	-	-	-	dB
6th and 7th Harmonics		-40	-	-	-	dB

Notes:
3. Improved Spec. as required to meet ISO/IEEE 802.3 specifications.
4. V_{OC} has no impact on system performance since twisted pairs are transformer isolated.
5. For a minimum pulse width of ≥ 40 ns.
6. Measured with external diode in place (between coax center conductor and TXO pin). The maximum diode capacitance is 1pF. Tap capacitance guaranteed by characterization.
7. Guaranteed through characterization, and production measurement of rise and fall times.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
DC Supply Voltage, VEE (GND = 0V)	8.55	-	9.45	V
Operating Temperature	0	-	70	°C
RR± Resistor	990	-	1010	Ω

CS83C92A SWITCHING CHARACTERISTICS (TA = 0° to 70°C, VEE = -9.0 V ±5%, GND = 0V, CD±, RX± pull downs = 510Ω)

Parameter	Symbol	Min	Typ	Max	Units
Receiver Startup Delay (RXI to RX±)	t_{RON}	-	4	5	bits
Receiver Propagation Delay (RXI to RX±)	t_{Rd}	-	15	50	ns
Differential Outputs Rise Time (RX±, CD±)	t_{Rr}	-	4	7	ns
Differential Outputs Fall Time (RX±, CD±)	t_{Rf}	-	4	7	ns
Receiver and Cable Total Jitter	t_{RJ}	-	±2	-	ns
Transmitter Start-up Delay	t_{TST}	-	1	-	bits
Transmitter Propagation Delay	t_{Td}	-	25	50	ns
Transmitter Rise Time - 10% to 90% (TXO)	t_{Tr}	20	25	30	ns
Transmitter Fall Time - 10% to 90% (TXO)	t_{Tf}	20	25	30	ns
t_{Tr} and t_{Tf} Mismatch	t_{TM}	-	0.5	-	ns
Transmitter Skew (TXO) (Note 8)	t_{TS}	-	±0.5	-	ns
Transmit Turn-on Pulse Width at V_{TS} (TX±) (Note 9)	t_{TON}	-	20	40	ns
Transmit Turn-off Pulse Width above V_{TS} (TX±)	t_{TOFF}	-	250	-	ns
Collision Turn-on Delay	t_{CON}	-	7	-	bits
Collision Turn-off Delay	t_{COFF}	-	-	20	bits
Collision Frequency (CD±)	f_{CP}	8.0	-	12.5	MHz
Collision Pulse Width (CD±)	t_{CP}	35	-	70	ns
CD Heartbeat Delay (TX± to CD±)	t_{HON}	0.6	-	1.6	µs
CD Heartbeat Duration (CD±)	t_{HW}	0.5	1.0	1.5	µs
Jabber Activation Delay (TX± to TXO and CD±)	t_{JA}	20	29	60	ms
Jabber Reset Timeout (TX± to TXO and CD±)	t_{JR}	250	500	750	ms

Notes: 8. Difference in propagation delay in outputing a positive edge as opposed to a negative edge.
9. For minimum pulse amplitude of ≥ -300mV.

2

CS83C92C SWITCHING CHARACTERISTICS (T_A = 0° to 70°C, VEE = -9.0 V ±5%, GND = 0V, CD±, RX± pull downs = 510Ω)

Parameter		Symbol	Min	Typ	Max	Units
Receiver Startup Delay (RXI to RX±)		t_{RON}	-	4	5	bits
Receiver Propagation Delay (RXI to RX±)		t_{Rd}	-	15	50	ns
Differential Outputs Rise Time (RX±, CD±)	(Note 3)	t_{Rr}	-	4	7	ns
Differential Outputs Fall Time (RX±, CD±)	(Note 3)	t_{Rf}	-	4	7	ns
Receiver and Cable Total Jitter	(Note 10)	t_{RJ}	-	±2	±6	ns
Transmitter Start-up Delay	(Note 3)	t_{TST}	-	1	2	bits
Transmitter Propagation Delay		t_{Td}	5	25	50	ns
Transmitter Rise Time - 10% to 90% (TXO)	(Note 3)	t_{Tr}	20	25	30	ns
Transmitter Fall Time - 10% to 90% (TXO)	(Note 3)	t_{Tf}	20	25	30	ns
t_{Tr} and t_{Tf} Mismatch	(Note 3)	t_{TM}	-	0.5	2.0	ns
Transmitter Skew (TXO)	(Note 8, 10)	t_{TS}	-	±0.5	±2	ns
Transmit Turn-on Pulse Width at V_{TS} (TX±)	(Note 9)	t_{TON}	15	20	40	ns
Transmit Turn-off Pulse Width above V_{TS} (TX±)	(Note 11)	t_{TOFF}	200	-	-	ns
Collision Turn-on Delay	(Note 3)	t_{CON}	-	7	13	bits
Collision Turn-off Delay		t_{COFF}	-	-	20	bits
Collision Frequency (CD±)		f_{CP}	8.5	-	11.5	MHz
Collision Pulse Width (CD±)		t_{CP}	40	-	60	%
CD Heartbeat Delay (TX± to CD±)		t_{HON}	0.6	-	1.6	µs
CD Heartbeat Duration (CD±)		t_{HW}	0.5	1.0	1.5	µs
Jabber Activation Delay (TX± to TXO and CD±)		t_{JA}	20	29	60	ms
Jabber Reset Timeout (TX± to TXO and CD±)		t_{JR}	250	500	750	ms

Notes: 10. Maximum spec guranteed by design and characterization.
11. Represents 802.3 requirement for IDL condition. CS83C92 will recognize IDL condition in the range of 130ns to 200ns.

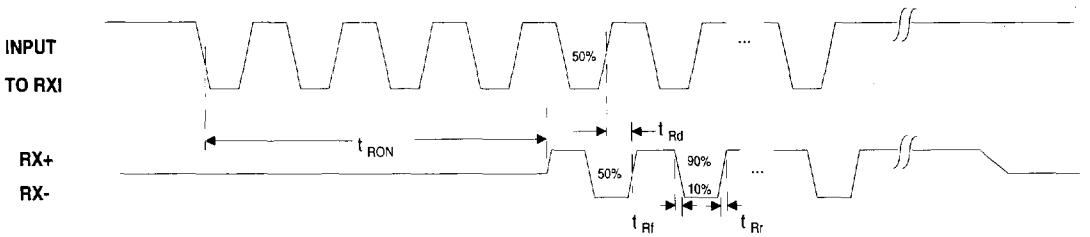


Figure 1. Receiver Timing

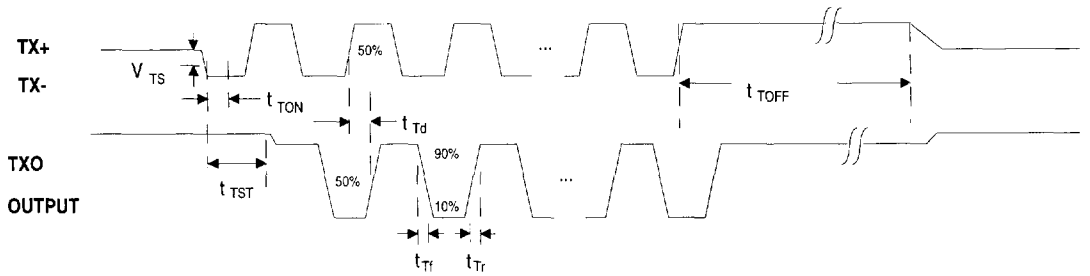


Figure 2. Transmitter Timing

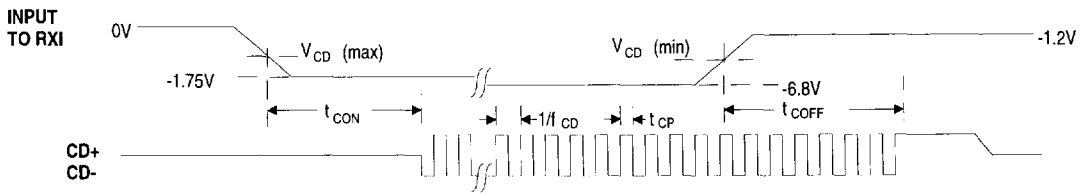


Figure 3. Collision Timing and Test Ciruit

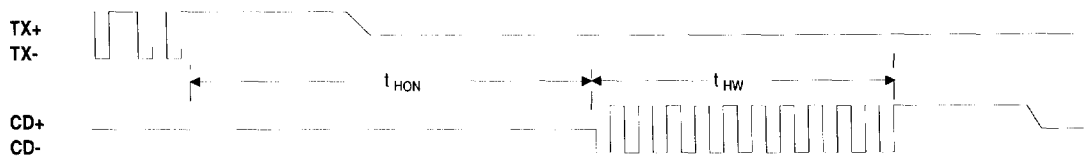


Figure 4. Heartbeat Timing

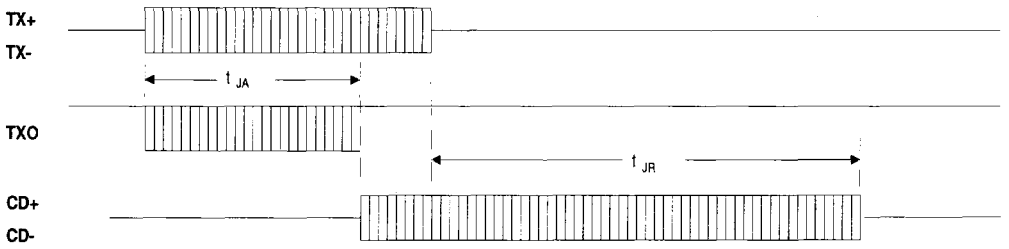


Figure 5. Jabber Timing

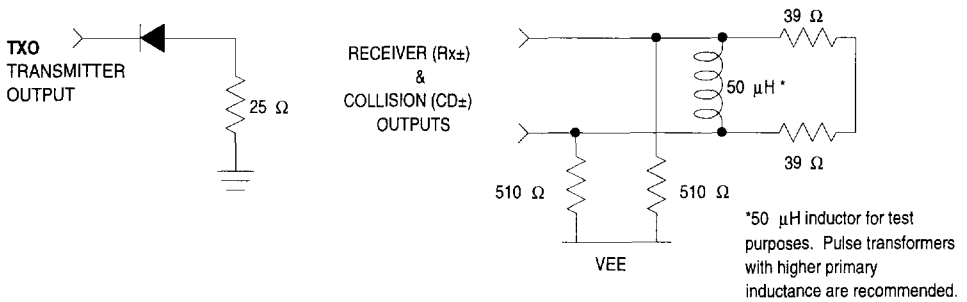


Figure 6. Test Loads

THEORY OF OPERATION

The CS83C92 interfaces the LAN station equipment to an Ethernet or Cheapernet COAX cable. The CS83C92 transmitter provides the current drive and pulse shaping required to drive signals onto the COAX, as well as squelch for signals received from the transmit pair, TX±. The receiver section provides equalization and squelch for signals on the COAX. Collisions are continually monitored and indicated by a 10MHz clock output on the CD± pair. The device also has a jabber timer which disables the transmitter and signals the DTE if packets longer than the legal length are transmitted.

In an Ethernet LAN, the CS83C92 mounts on the COAX cable, and connects to the station equipment through a transceiver drop cable (AUI cable). The transceiver drop cable can be up to 50 meters long. For Cheapernet applications, the CS83C92 is usually located in the station equipment, and connects to the Cheapernet COAX (such as RG58) through a BNC connector.

Transmitter

The transmitter accepts differential signals at the TX± inputs from the Manchester Code Converter, and drives these signals onto the network from the TXO output at the signal levels required by IEEE 802.3.

The TXO pin is open drain, and is pulled up to ground by the COAX termination resistors. The rise and fall times of the output pulses are internally conditioned to achieve slew rates of 25ns to reduce harmonics in the transmitted signal. Output drive current levels are set by a bandgap voltage reference and an external 1kΩ 1% resistor connected between the RR± pins. When not transmitting, the TXO output is disabled to prevent noise on the network. An external 1N916 diode must be added to reduce loading and capacitance (in both powered and unpowered conditions) to comply with ISO and IEEE specifications. With the diode in place, the tap capacitance contributed by the CS83C92 is typically less than 3 pF.

The transmit squelch circuit blocks signals input from TX± with pulse widths of less than 15ns or amplitudes of less than -175mV. The squelch circuit turns the transmitter off if the signal stays more positive than -175mV for more than 200ns (end of packet detection).

The TX± pins are transformer coupled to the Manchester Code Converter. In Ethernet applications where a transceiver drop cable (or Access Unit Interface, AUI) is used, a 78Ω resistor should be placed across the end of the cable, near the transformer. This resistor may be eliminated for Cheapernet applications where no AUI cable is used.

Receiver

The receiver input, RXI, connects to the COAX center conductor. The CS83C92 amplifies and equalizes the input signal and passes signals which exceed the receiver squelch level to the Receiver Pair, RX±. Up to five bits may be received at RXI and not transmitted on the RX± pair. The sixth bit will be transmitted, but may have code violations. The seventh and subsequent bits will be transmitted according to specificaton.

The receiver squelch circuit prevents false triggering of the receiver due to noise on the COAX. Signals input to the RXI pin that cause the output of an internal low-pass filter to exceed -140mV$_{DC}$ (typical) will exceed the DC squelch level, and be passed through to the RX± pair. Should the positive pulse width exceed 200ns (typical) the receiver will turn off (end of packet detection). The receiver will stay off if the output of the low-pass filter rises above the squelch threshold within 1µs.

RX± comprise a differential line driver which interfaces to the Manchester Code Converter via an isolation transformer. RX± go to a differential zero state when idle to prevent DC current from saturating the isolation transformer.

For Ethernet applications, the RX± pins are tied to the VEE supply through 500Ω or 510Ω resistors. In Cheapernet applications, the CS83C92 is generally located on the same card as the Manchester Code Conveter, and 1500Ω pull-down resistors may be used to reduce power consumption.

Collison Detection

The collison detector monitors the COAX center conductor and senses the voltage conditions indicative of a collison. A collison can be detected when two or more stations are concurrently transmitting, whether or not the local transmitter is activated. The detector signals a collison by sending a 10MHz clock signal out on the Collison Pair, CD±, to the Manchester Code Converter.

The CDS pin provides a coaxial ground reference voltage for the collision detector. This pin should be connected to the shield of the COAX, rather than power supply ground, to prevent inaccuracies due to ground drops. A collison is detected when the output voltage of the receiver low-pass filter exceeds the collison voltage threshold, V_{CD}.

The 10MHz clock is internally generated, and used for collison indication and the heartbeat test. This oscillator requires no external components.

If enabled (HBE high), the Heartbeat Test will cause transmission of the 10MHz clock on the CD± pair for 1.0µs, 1.1µs after the end of each transmission if: both the transmitter and receiver were enabled; there was not a collision detected; jabber has not occured.

For Ethernet applications, the CD± pins are tied to the VEE supply through 500Ω or 510Ω resistors. In Cheapernet applications, the CS83C92 is generally located on the same card as the Manchester Code Converter, and the use of 1500Ω pull-down resistors will reduce power consumption.

Jabber Timer

The Jabber Timer monitors the operation of the transmitter using an internal oscillator as a time base. If the transmitter operates continuously for more than 29ms, the jabber timer disables the transmitter and enables the Collison Detector outputs. The Jabber Timer continues to monitor the transmitter squelch output. After the Manchester Code Converter has been silent for 750ms, the output on CD± is terminated, and the transmitter is reenabled for the next valid packet.

P. C. Board Layout

The CS83C92 is built in CMOS technology. It consumes and dissipates far less power than equivalent bipolar circuits. Still, heat dissipation and device reliability will be improved if the VEE pins are connected to a copper plane on the PC board. However, the application demands that the CS83C92 handle significant currents in the process of driving signals onto the cable. Soldering all of the VEE pins onto a copper plane is required to provide a surface area which aids in heat dissipations.

For Ethernet applications, the isolation transformers, the DC to DC converter, and the transceiver are located in the Transceiver assembly, attached to the COAX. For Cheapernet applications, these components are usually mounted on the same board as the Ethernet Controller (CS8900). The 78Ω and 39.2Ω load

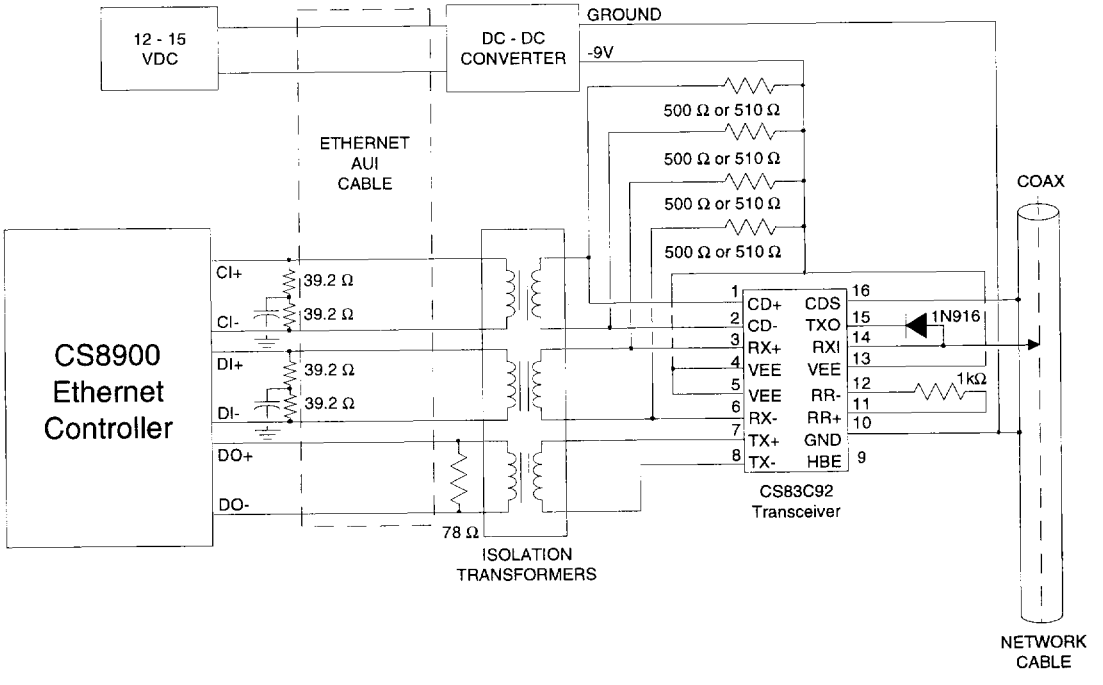


Figure 7. CS83C92 System Connection Diagram

resistors terminate the AUI cable, and are not required in systems where the AUI cable is not used (where the distance between the CS8900 and Transceiver is short).

For the PLCC package, it is recommended that a small printed circuit board V_{EE} plane be connected to pins 5-11, and a second one be connected to pins 20-25. To reduce the thermal resistance, the area of the plane on each set of pins should be ≥ 0.19 square inches (approx. 0.5" x 0.375"). Figure 8 illustrates a recommended component side layout for these planes.

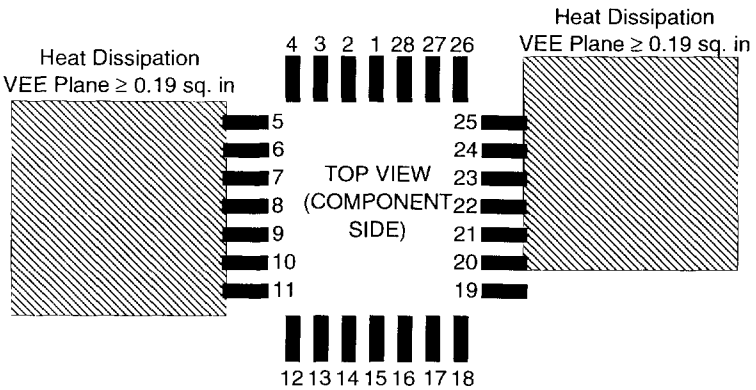
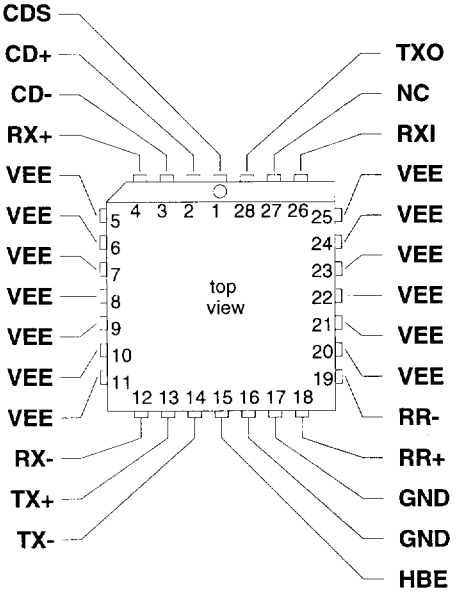


Figure 8. Recommended Dissipation Planes for PLCC

PIN DESCRIPTIONS

CS83C92

Collison Detect Output +	CD+	1	16	CDS	Collison Detect Sense
Collison Detect Output -	CD-	2	15	TXO	Transmitter Output
Receive Data Output +	RX+	3	14	RXI	Receive Input
Negative Power Supply	VEE	4	13	VEE	Negative Power Supply
Negative Power Supply	VEE	5	12	RR-	External Resistor -
Receive Data Output -	RX-	6	11	RR+	External Resistor +
Transmit Data Input+	TX+	7	10	GND	Ground
Transmit Data Input -	TX-	8	9	HBE	Heartbeat Enable



Power Supplies

VEE - Negative Power Supply

The -9V supply is connected to these pins. A 0.1µF decoupling capacitor should be connected between this pin and GND. All of the VEE pins should be soldered to a copper VEE plane.

GND - Ground

Power supply ground; connects to COAX shield.

Inputs

TX+, TX- - Transmit Inputs

Balanced differential line receiver which accepts the signal from the Manchester Code Converter. Signals exceeding transmitter squelch limits are output at TXO with the proper pulse shape. The common mode voltage on TX± is internally set and must not be externally established.

RXI - Network Receiver Input

Connects to the COAX center conductor. Signals meeting receiver squelch limits are recovered and output on RX±. RXI also detects the collison voltage level.

Outputs

TXO - Network Transmitter Output

TXO connects to the coax center conductor, and drives signals which meet TX± squelch requirements onto the coax. An external 1N916 diode, or equivalent, must be placed between the TXO pin and the coax center conductor to reduce capacitance and inhibit current flow at the TXO pin when the voltage on the coax center conductor is more negative than the power supply voltage applied to the CS83C92.

CD+, CD- - Collison Outputs

A balanced differential output which drives an internally generated 10MHz signal to the station equipment when a collison is detected, when excessive transmission occurs, or during a CD heartbeat condition. These outputs are open source: when driving a 78Ω transmission line, these pins should be pulled to VEE with 500Ω or 510Ω resistors; for Cheapernet applications, where the CS83C92 is not driving a 78Ω load, use of 1.5kΩ resistors will save power.

RX+, RX- - Receive Data Outputs

A balanced differential output which drives the data recovered from the network to the MCC. These outputs are open source: when driving a 78Ω transmission line, these pins should be pulled to VEE with 500Ω or 510Ω resistors; for Cheapernet applications, where the CS83C92 is not driving a 78Ω load, use of 1.5kΩ resistors will save power.

Control

HBE - Heartbeat Enable

When the HBE pin is connected to ground, the Collision Detect Heartbeat test is enabled. Connecting the HBE pin to VEE disables the Collision Detect test.

RR+, RR- - External Resistor

A 1kΩ, 1% resistor should be connected across these pins to set internal operating current levels.

CDS - Collision Detect Sense

The CDS pin connects directly to the COAX shield, providing a reference for the collision detection voltage level.

Miscellaneous

NC - No Connect (PLCC only).

This pin should be left floating.