Revision History

Rev. No.	History	Issue Date
1.0	New issue	Aug. 01, 2016
1.1	Revise error typing in Page 1, Description:16-Pin SOP/SSOP to **16-pin SSOP** Page 2, Block Diagram: OUT8 to **OUT7** Page 3, 3.1 Pin Description: 16 constant.. to **8** constant….. 3.2 Equivalent Circuit of I/O Pins: INPUNT / OUTPUNT to **INPUT** / **OUTPUT**	Aug. 03, 2016

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■ Description

The CS8819, 8 channel constant current LED driver operates over a 3 ~ 5.5V input voltage range. The device provides total 8 open-drain constant current sinking outputs that are rated to 17V and delivers up to 120mA of high accuracy current to each string of LED. The current at each output is programmable by means of one external resistor.

The CS8819 features the fast 25MHz DCK input, allowing large amount data transfer and a wide LED dimming (on/off) range to be implemented. The CS8819 also offers 4-wire serial interface, 8-bit shift registers, and 8-bit latches. The serial interface allows a microcontroller to configure the output channels using four inputs (DI, DCK, LAT, and ENB) and a data output (DO). DO allows multiple drivers to be cascaded and operated together.

The CS8819's on-board pass elements minimize the need for external components, while at the same time, providing ±1.5% LED current accuracy. Additional features include a ±0.1% regulated output current capability and 50ns fast output transient response. The CS8819 is available in a 16-pinSSOP-150mil package and operating over the -40°C to +85°C ambient temperature range.

■ Feature

- 8 Constant current output channels
- 3 ~ 5.5V Operating supply voltage
- 3~120mA/5V Constant current output range
- 3~115mA/3.3V Constant current output range
- 17V Rated output channels for long LED strings
- ±1.5% (typ.) LED Current accuracy between channels
- ±3% (typ.) LED Current accuracy between chips
- ±0.1% Output current regulation capability
- 25MHz Clock frequency for data transfer
- 50ns fast current transient response
- Output current setting by external resister
- Schmitt trigger input
- Power on reset
- Stagger output delay for EMI reduction
- -40°C to +85°C Ambient temperature rang

■ Product Family

CS8819AD ------- 16SSOP (150mil, 0.635mm lead-pitch)

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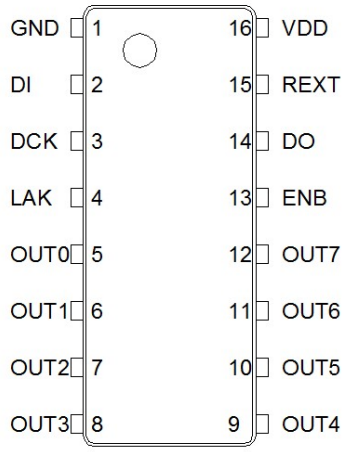
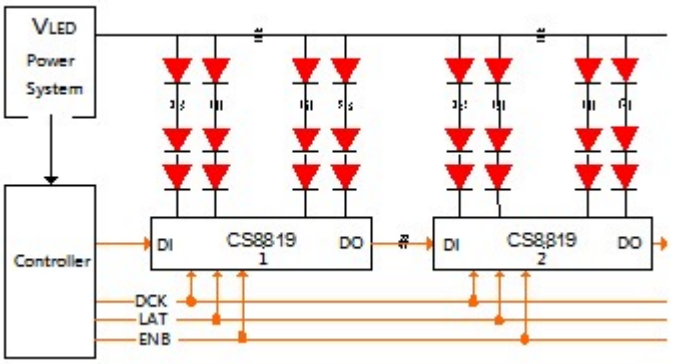
■ Pin Assignment

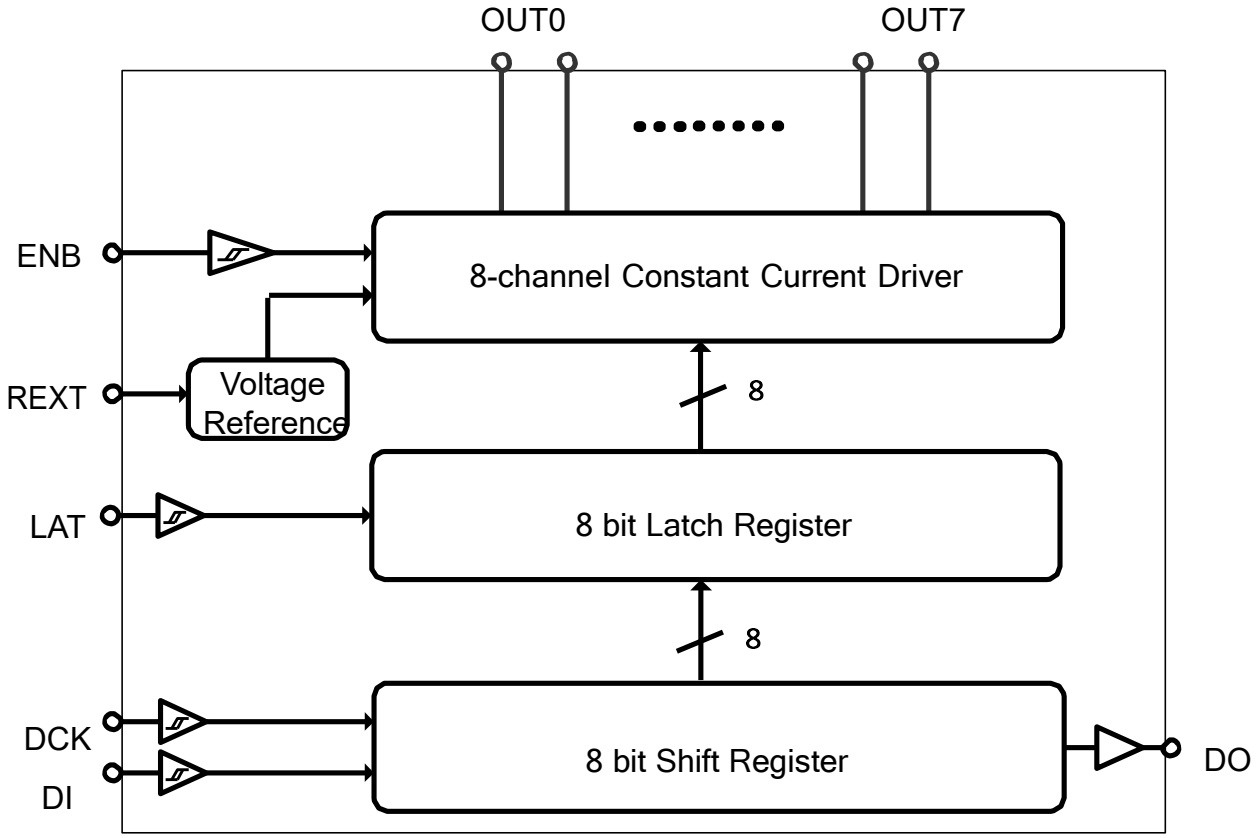


16L SSOP

■ Typical Operating Circuits



■ Block Diagram



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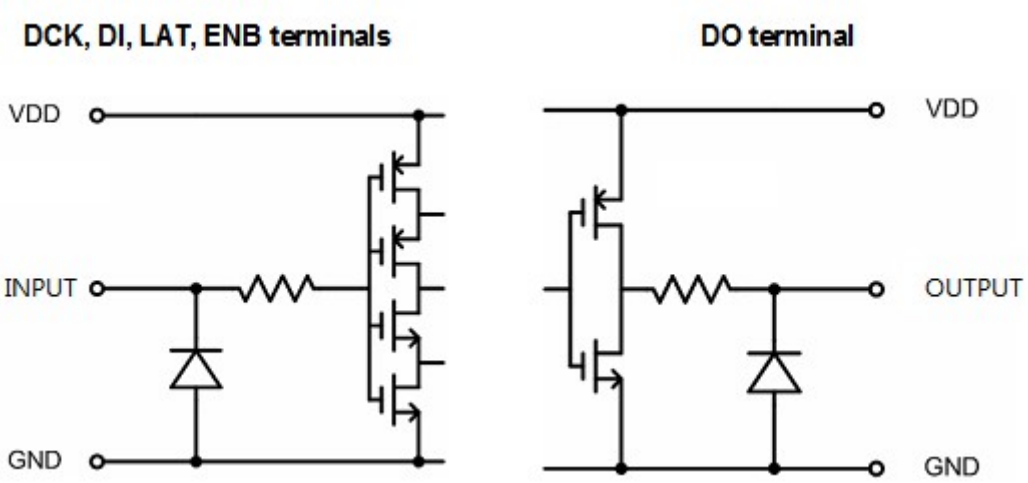
■ Pin Description

Pin No.	Pin Name	Function
1	GND	GND Pin.
2	DI	Serial input data pin.
3	DCK	Clock input terminal for shift register, rising edge trigger.
4	LAT	Input terminal of data strobe.
5~12	OUT0~OUT7	8 constant current output pin to drive common anode LEDs.
13	ENB	Data output enable pin, when ENABLE=High-level, all OUT0~OUT7 are turned off, and when ENABLE=Low-level, all OUT0~OUT7 are enabled.
14	DO	Serial data output pin for cascade operation.
15	REXT	The external resistor connection pin to adjust the output current.
16	VDD	3.3V~5.5V supply voltage pin.

■ Equivalent Circuits of I/O Pins



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■ Absolute Maximum Ratings (Ta=25 °C, Tj (max) = 150 °C)

Characteristics	Symbol	Rating	Unit
Supply Voltage	VDD	-0.3~7.0	V
Input Voltage	Vin	-0.3 to VDD+0.3	V
Output Current	Iout	130	mA
Output Voltage	Vout	-0.3 to 17	V
GND Pin Current	IGND	1100	mA
Clock Frequency	FDCK	25	MHz
Thermal Resistance (On PCB)	Rth (j-a)	16SSOP: 80	℃/W
Operating Temperature	Top	-40 to 85	℃
Storage Temperature	Tstg	-55 to 150	℃

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.
(2) All voltage values are with respect to ground terminal.

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■ Electrical Characteristics (VDD = 3.3 V, Ta = 25 °C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1.43 mA	—	—	0.4	V
	VOH	IOH= 1.43 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel)	dIOUT1	VOUT = 1.0 V Rrext = 720 Ω	—	±1.5	±3.0	%
Output Current Skew (Chip-to-Chip)	dIOUT2		—	±3.0	±6.0	%
Output Current Skew (Channel-to-Channel)	dIOUT3	VOUT = 1.0 V Rrext = 6 KΩ	—	±1.5	±3.0	%
Output Current Skew (Chip-to-Chip)	dIOUT4			±3.0	±6.0	%
Output Voltage Regulation	% / VOUT	Rrext = 720 Ω, VOUT = 1V ~ 3V	—	—	±0.1	% / V
Supply Voltage Regulation	% / VDD	Rrext = 720 Ω, VDD = 3V ~ 5.5 V	—	±0.7	±1	
Supply Current	$I_{DD1\ (off)}$	All pins are open unless VDD and GND	—	1.13	—	mA
	$I_{DD2\ (off)}$	input signal is static Rrext = 6.0 KΩ all outputs turn off	—	1.49	—	
	$I_{DD3\ (on)}$	input signal is static Rrext = 6.0 KΩ all outputs turn on	—	1.51	—	
	$I_{DD4\ (off)}$	input signal is static Rrext = 720 Ω all outputs turn off	—	4.21	—	
	$I_{DD5\ (on)}$	input signal is static Rrext = 720 Ω all outputs turn on	—	4.27	—	

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■ Electrical Characteristics (VDD = 5.0 V, Ta = 25 °C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1.85 mA	—	—	0.4	V
	VOH	IOH= 1.85 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel)	dIOUT1	VOUT = 1.0 V Rrext = 720 Ω	—	±1.5	±3.0	%
Output Current Skew (Chip-to-Chip)	dIOUT2		—	±3.0	±6.0	%
Output Current Skew (Channel-to-Channel)	dIOUT3	VOUT = 1.0 V Rrext = 6 KΩ	—	±1.5	±3.0	%
Output Current Skew (Chip-to-Chip)	dIOUT4			±3.0	±6.0	%
Output Voltage Regulation	% / VOUT	Rrext = 720 Ω, VOUT = 1 V ~ 3 V	—	—	±0.1	% / V
Supply Voltage Regulation	% / VDD	Rrext = 720 Ω, VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current	$I_{DD1\ (off)}$	All pins are open unless VDD and GND	—	1.28	—	mA
	$I_{DD2\ (off)}$	input signal is static Rrext = 6.0 KΩ all outputs turn off	—	1.57	—	
	$I_{DD3\ (on)}$	input signal is static Rrext = 6.0 KΩ all outputs turn on	—	1.63	—	
	$I_{DD4\ (off)}$	input signal is static Rrext = 720 Ω all outputs turn off	—	4.37	—	
	$I_{DD5\ (on)}$	input signal is static Rrext = 720 Ω all outputs turn on	—	4.46	—	

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■ Switching Characteristics (VDD = 3.3 V, Ta = 25 °C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	ENB-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 720 Ω VL =5.0 V RL = 150 Ω CL = 13 pF		50	—	ns
	LAT-to-OUT0	tpLH2		—	48	—	
	DCK-to-DO	tpLH3		—	31	—	
Propagation Delay ('H' to 'L')	ENB-to-OUT0	tpHL1		—	45	—	
	LAT-to-OUT0	tpHL2		—	37	—	
	DCK-DO	tpHL3		—	31	—	
Pulse Duration	ENB	$tw_{(ENB)}$		50	—	—	
	LAT	$tw_{(LAT)}$		20	—	—	
	DCK	$tw_{(DCK)}$		20	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		5	—	—	
	DI	$tsu_{(DI)}$		4	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(DI)}$		4	—	—	
DO Rise Time		$tr_{(DO)}$		—	14	—	
DO Fall Time		$tf_{(DO)}$		—	13	—	
Output Current Rise Time		tor		—	21	—	
Output Current Fall Time		tof		—	15	—	
Output Delay Time (OUT(n)-to-OUT(n+4))		tod		—	25	—	

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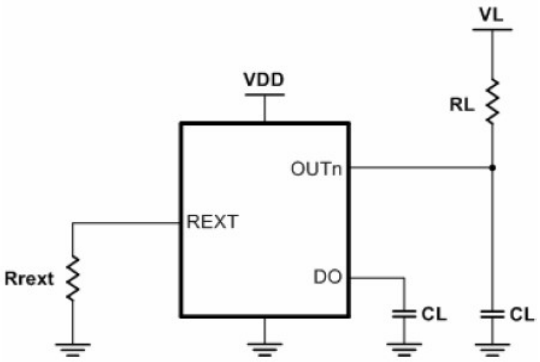
■ Switching Characteristics (VDD = 5.0 V, Ta = 25 °C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	ENB-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 720 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	29	—	ns
	LAT-to-OUT0	tpLH2		—	30	—	
	DCK-DO	tpLH3		—	26	—	
Propagation Delay ('H' to 'L')	ENB-to-OUT0	tpHL1		—	25	—	
	LAT-to-OUT0	tpHL2		—	23	—	
	DCK-DO	tpHL3		—	27	—	
Pulse Duration	ENB	$t_{w(ENB)}$		50	—	—	
	LAT	$t_{w(LAT)}$		20	—	—	
	DCK	$t_{w(DCK)}$		20	—	—	
Setup Time	LAT	$t_{su(LAT)}$		5	—	—	
	DI	$t_{su(DI)}$		4	—	—	
Hold Time	LAT	$t_{h(LAT)}$		20	—	—	
	DI	$t_{h(DI)}$		4	—	—	
DO Rise Time		$t_{r(DO)}$		—	11	—	
DO Fall Time		$t_{f(DO)}$		—	11	—	
Output Current Rise Time		tor		—	18	—	
Output Current Fall Time		tof		—	16	—	
Output Delay Time (OUT(n)-to-OUT(n+4))		tod		—	16	—	



Switching Characteristics Test Circuit

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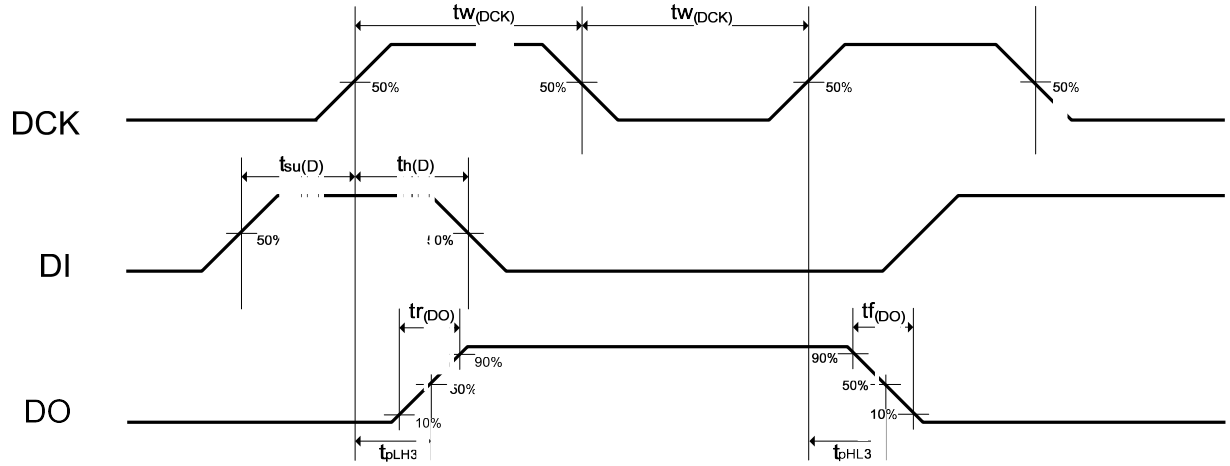
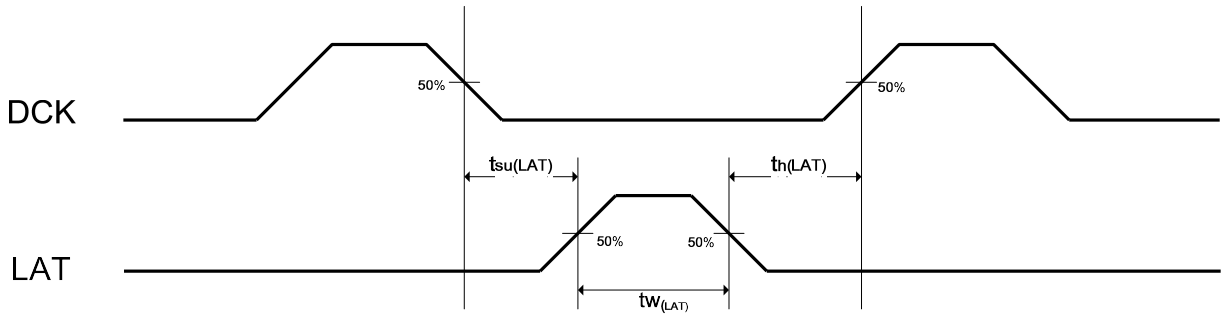
■ Timing Diagram

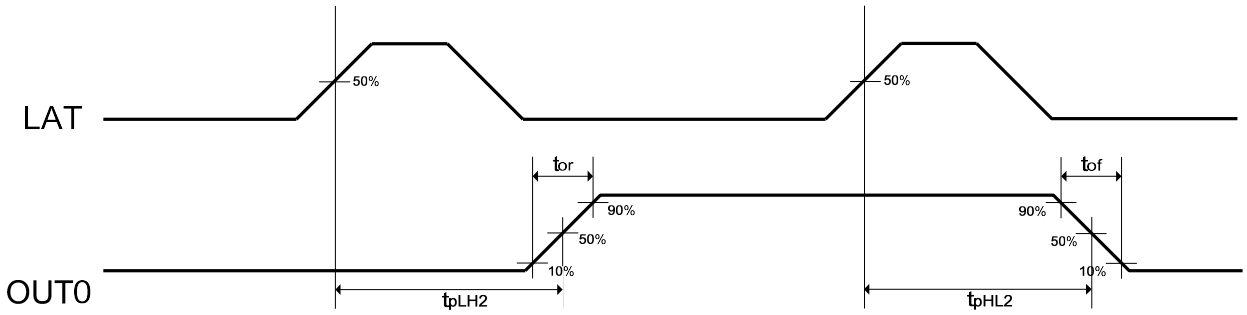
DCK-DI, DO



DCK-LAT



LAT-OUT0



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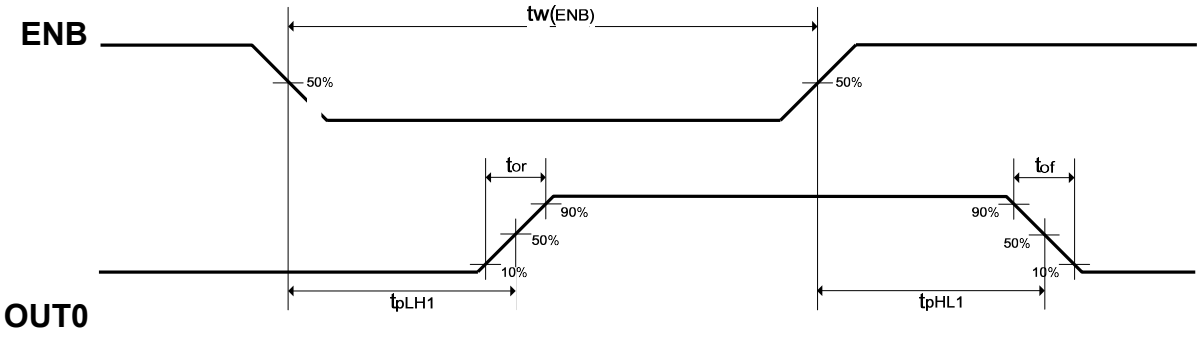
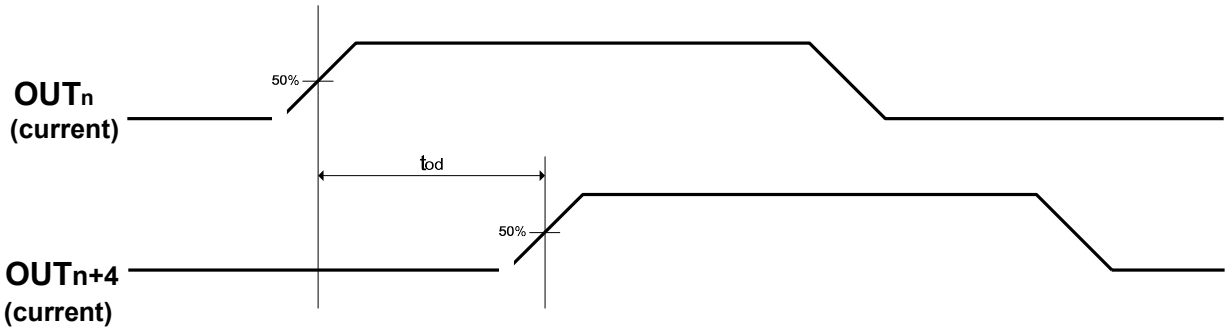
ENB-OUT0



OUTn-OUTn+4



■ Fast Transient Response

The CS8819 supports the fast transient response to make high image resolution possible. The ENB pulse width of 50ns is guaranteed to get a complete Vout waveform.
Test condition: VL=5V, RL=150Ω, CL=13pF, Rrext=720Ω

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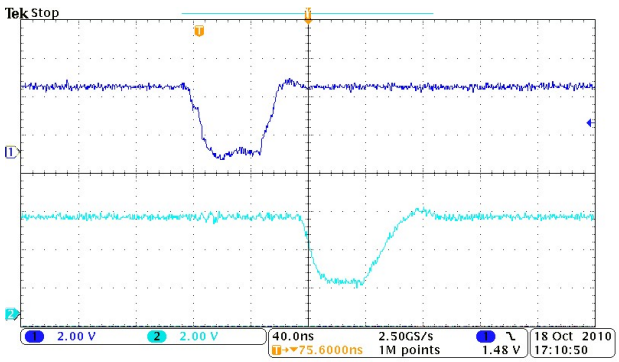
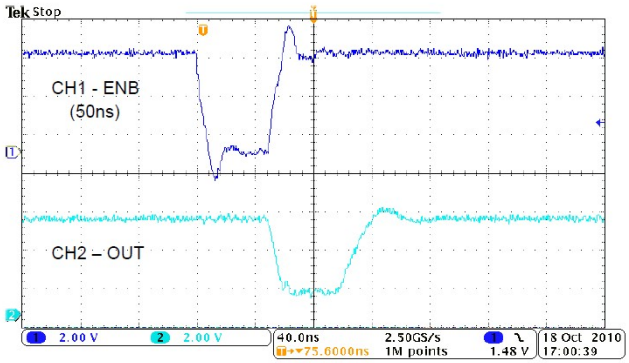
Output Voltage Waveform @VDD=3.3V



Output Voltage Waveform @VDD=5V



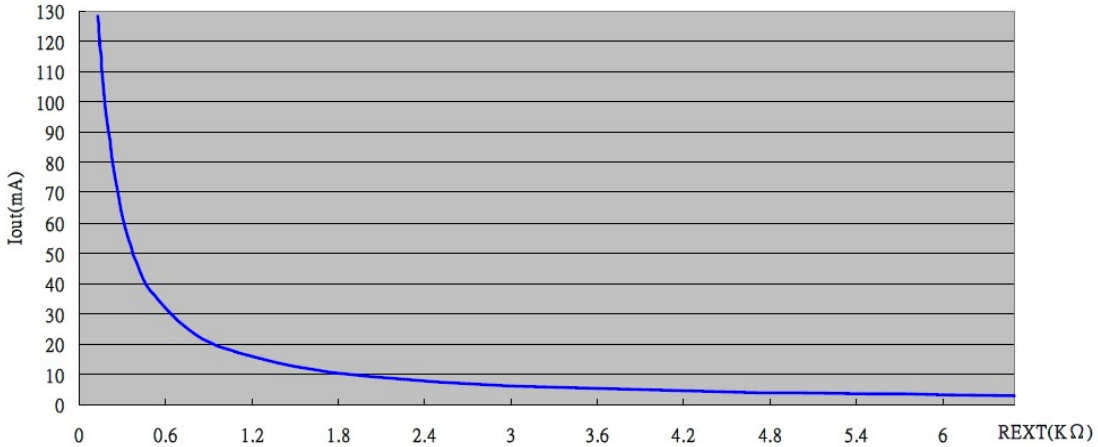
■ Reference Resistor

The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$I\ out\ (mA) = 18.3 / R rext\ (K\Omega)$$

Where Rrext is a resistor placed between REXT and GND
For example, Iout is 25.4mA when Rrext=720Ω and Iout is 3mA when Rrext=6KΩ

CS8819 Iout v.s. Rext Curve



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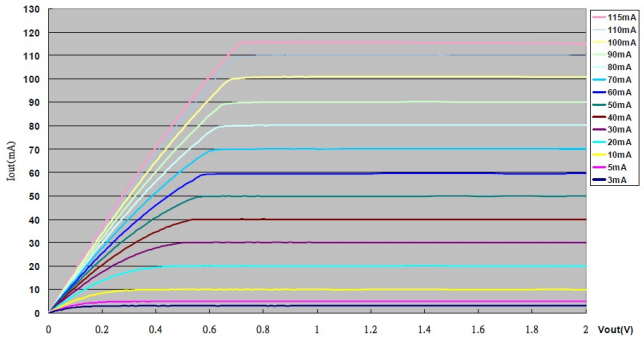
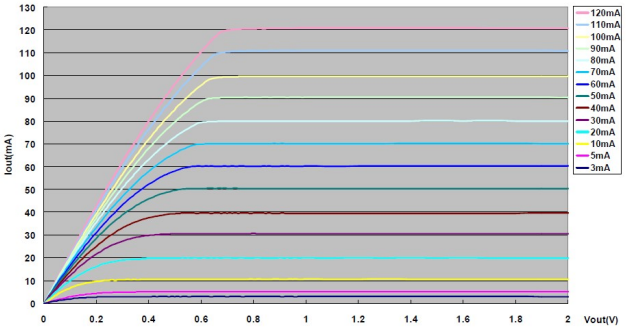
■ Constant-Current Output

The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the CS8819 could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage should be determined in order to keep an excellent performance.

CS8819 Iout V.S. Vout Curve@VDD=3.3V



CS8819 Iout V.S. Vout Curve@VDD=5V



■ Serial Data Interface

CS8819 shifts the image data to the register from the DI pin on the rising edge of data clock (DCK). After whole given image data are transferred into 8bits shift register, the image data are loaded into the latch register by a strobe signal (LAT). The latch action is triggered at the rising edge of LAT signal. And the serial data will be shifted out from the DO pin on the synchronization of the rising edge of DCK. Furthermore, the enable signal (ENB) will turn off all outputs when it is set to the high level.

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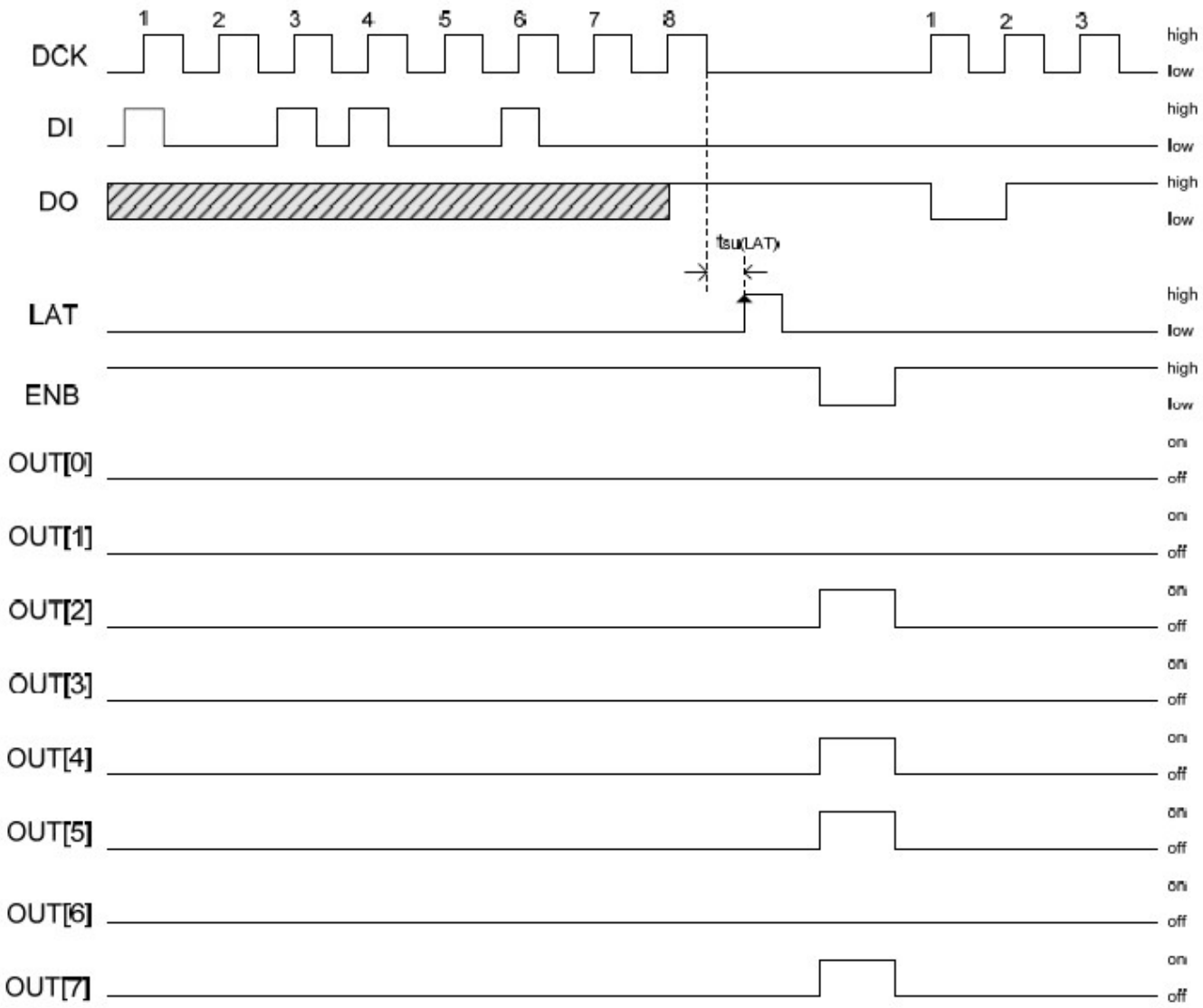

■ Stagger Outputs Delay

Large in-rush currents will be induced when the system activates all the outputs at once. To reduce this interference of EMI, the CS8819 is designed to have a constant length of delay time (around 16ns) between two output groups. The two output groups individually are the first group from OUT0 to OUT3 and the second group from OUT4 to OUT7.

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■ Power Dissipation

When the 8 output channels are turned on, the practical power dissipation is determined by the following equation:

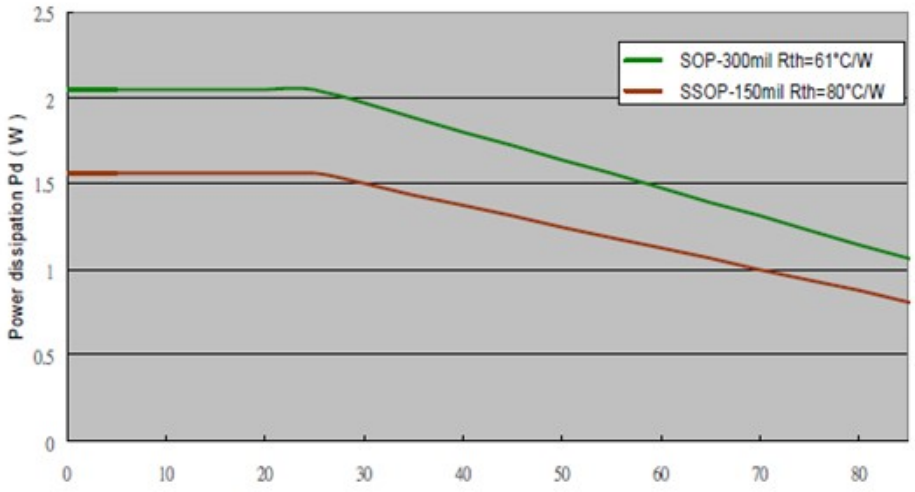
$$PD\ (practical) = VDD \times IDD + Vout_{(0)} \times Iout_{(0)} \times Duty_{(0)} + \cdots + Vout_{(N)} \times Iout_{(N)} \times Duty_{(N)} \quad (where\ N=0\ to\ 7)$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package types and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD\ (max) = \frac{Tj(max)(^{\circ}C) - Ta(^{\circ}C)}{Rth(j\text{-}a)(^{\circ}C/Watt)}$$

The PD(max) declines as the ambient temperature raises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in the four different packages.

Maximum Power Dissipation v.s. Ambient Temperature



Ambient Temperature Ta (°C)

■ Order Information

Part No.	Package Type	Lead Pitch
CS8819AD	16L SSOP(150mil)	0.635mm

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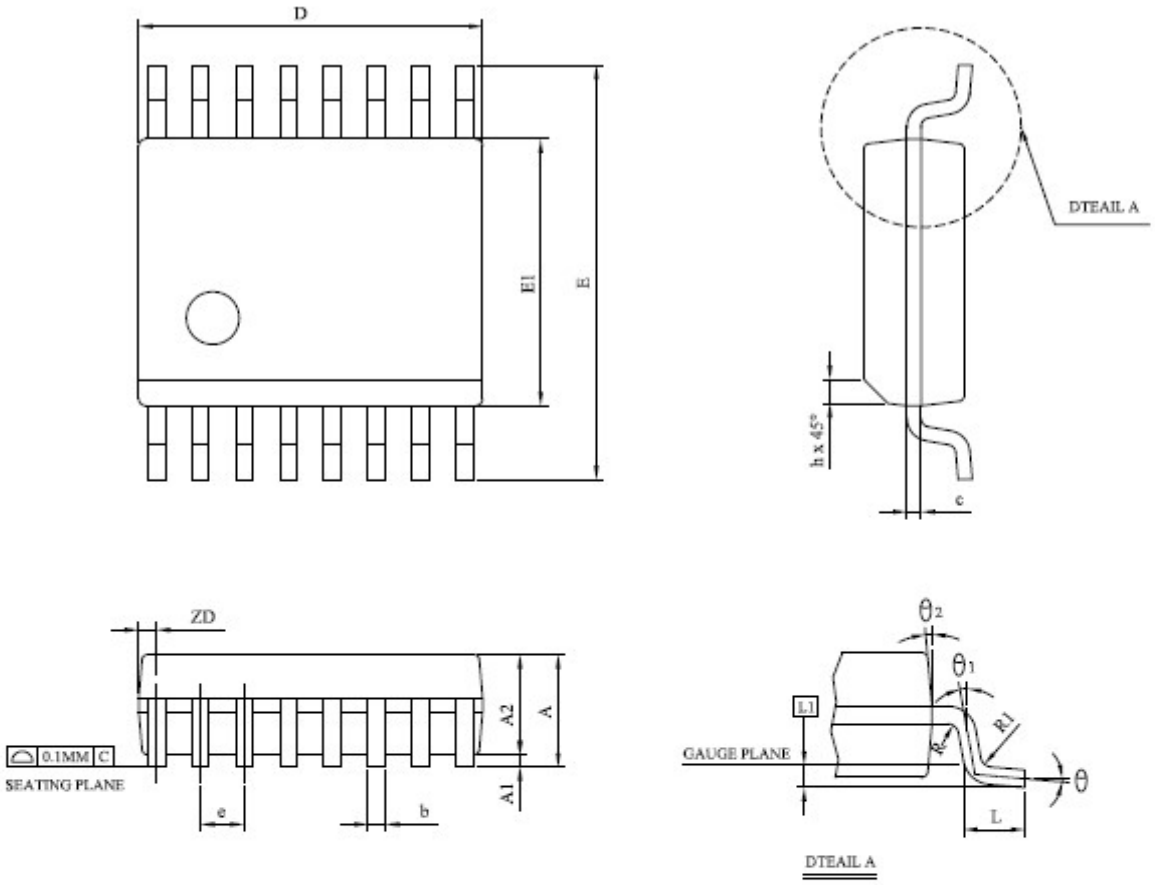
■ Package Outline

16L SSOP-150mil



Note:

1.Dimension D does not include mold protrusions or gate burrs.

2.Mold protrusions and gate burrs shall not exceed 0.006 inch per side.

3. JEDEC : MO-137(AB).

3.Plating thickness : 0.3 ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b	c	e	D	E	E1	L	h	L1	ZD	R1	R	θ	θ1	θ2
MM	Min.	1.35	0.10	—	0.20	0.18	0.635 BASIC	4.80	5.79	3.81	0.41	0.25	0.254 BASIC	0.229 REF	0.20	0.20	0°	0°	5°
	Nor.	1.63	0.15	—	—	—		4.90	5.99	3.91	0.635	—			—	—	—	—	10°
	Max.	1.75	0.25	1.50	0.30	0.25		5.00	6.20	3.99	1.27	0.50			0.33	—	8°		15°
INCH	Min.	0.053	0.004	—	0.008	0.007	0.025 BASIC	0.189	0.228	0.150	0.016	0.010	0.010 BASIC	0.009 REF	0.008	0.008	0°	0°	5°
	Nor.	0.064	0.006	—	—	—		0.193	0.236	0.154	0.025	—			—	—	—	—	10°
	Max.	0.069	0.010	0.059	0.012	0.010		0.197	0.244	0.157	0.050	0.020			0.013	—	8°	—	15°

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