Semiconductor Corporation

CS8870

DTMF Receiver

Features

- Full Receiver Implementation
- Central Office Quality
- Adjustable Receive Sensitvity
- Adjustable Detection and Release Time
- Single Supply Operation
- Low Power Consumption
- 18 Pin Package
- Pin Compatible with MT8870B

General Description

The CS8870 is a fully integrated DTMF (Dual Tone Multifrequency) receiver for decoding tone pairs generated by a tone dialing telephone. The decoded signal is output as a four bit binary code. All of the functions needed to decode the 16 DTMF tone pairs are integrated in the CS8870 using Crystal's CMOS double-poly process, taking advantage of the low power and high performance offered by this technology.

ORDERING INFORMATION
CS8870-IP - 18 Pin Plastic DIP

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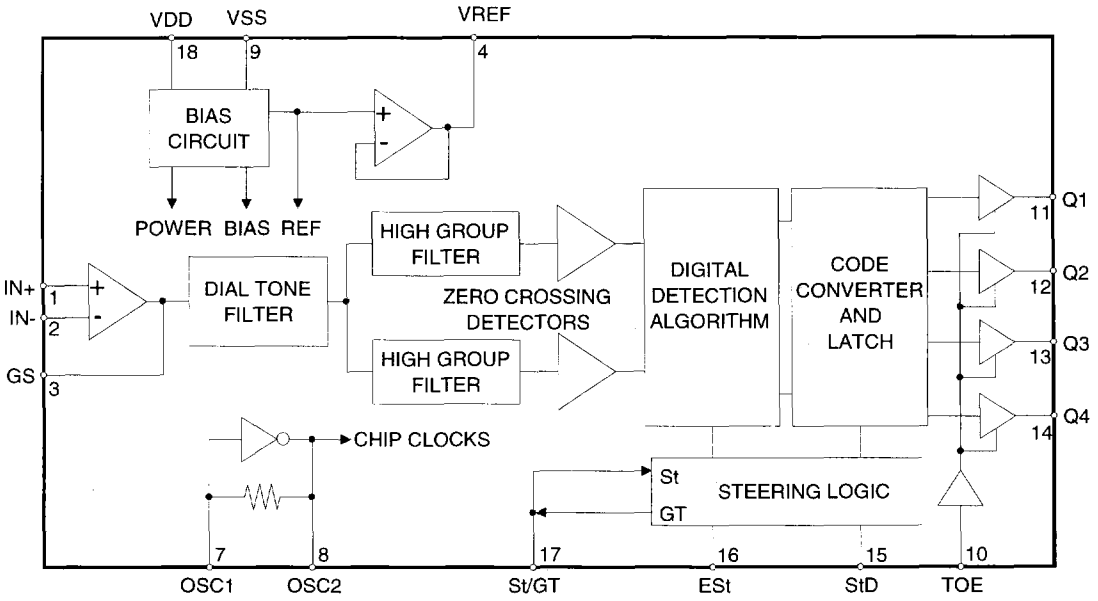

NOT RECOMMENDED FOR NEW DESIGNS

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ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply		V_{DD}-V_{SS}	-	6.0	V
Input Voltage		V_{in}	V_{SS} - 0.3	V_{DD} + 0.3	V
Input Current, Any Pin	(Note 1)	I_{in}	-	10	mA
Power Dissipation	(Note 2)	P_D	-	1000	mW
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Transient currents of up to 100mA will not cause latch-up.
2. Derate above 75°C at 16 mW/°C; all leads soldered to board.

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V_{DD}-V_{SS}	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	0	25	70	°C
Crystal Frequency	f_C	3.5759	3.5795	3.5831	MHz

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; f_C = 3.579545MHz)

Parameter	Symbol	Min	Typ	Max	Units
Supply Current	I_{DD}	-	6.0	10.0	mA
Power Consumption		-	30	45	mW
Input Impedance, pins 1 & 2 (Note 3)	R_{IN}	-	10	-	MΩ
Steering Threshold Voltage	V_{TSt}	2.2	-	2.5	V
Signal Levels for Valid Input (Notes 4, 5, 6, 7, 8, and 9) (each tone of composite signal)		-29 27.5	- -	+1 883	dBm mV_{rms}
Twist (Notes 5, 6, 8, 9, and 10)		-	±10	-	dB
Frequency Detect Bandwidth (Notes 5, 6, 7, and 9)		±1.5%±2Hz	-	±3.5%	
Third Tone Tolerance (Notes 5, 6, 7, 9, 11, and 12)		-	-16	-	dB
Noise Tolerance (Notes 5, 6, 7, 9, 11, 12, and 13)		-	-12	-	dB
Dial Tone Tolerance (Notes 5, 6, 7, 9, 11, 14, and 15)		-	+22	-	dB
Clock Output (OSC 2, pin 8) Capacitive Load		-	-	30	pF
V_{REF} Output Voltage No Load	V_{REF}	2.4	-	2.8	V
V_{REF} Output Resistance	R_{OR}	-	10	-	kΩ

Parameters measured using test circuit shown in Figure 4.

Notes:
3. Input frequency of 1kHz.
4. dBm referenced to power of 1mW into 600Ω load.
5. Digit sequence consists of all 16 DTMF tones.
6. Tone duration of 40ms, tone pause of 40ms.
7. Both tones of the composite signal have equal amplitudes.
8. Tone pair is deviated by ±1.5%±2Hz.
9. For error rate of better than 1 in 10,000.
10. Twist = high tone/low tone.
11. Nominal DTMF frequencies are used.
12. Referenced to lowest frequency component of DTMF signal.
13. Bandwidth limited to 3kHz Gaussian noise.
14. Precise dial tone frequencies of 350Hz±2% and 440Hz±2%.
15. Referenced to minimum valid accept level.

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ANALOG CHARACTERISTICS - Gain Setting Amplifier

(T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; voltages referenced to V_{SS})

Parameter		Symbol	Min	Typ	Max	Units
Input Leakage Current	(Note 16)	I_{IN}	-	100	-	nA
Input Resistance		R_{IN}	-	10	-	MΩ
Input Offset Voltage		V_{OS}	-	25	-	mV
Common Mode Rejection	(Note 17)	CMRR	-	60	-	dB
Power Supply Rejection	(Note 18)	PSRR	-	60	-	dB
DC Open Loop Voltage Gain		A_{VOL}	-	65	-	dB
Open Loop Unity Gain Bandwidth		f_C	-	1.5	-	MHz
Output Voltage Swing	(Note 19)	V_O	-	4.5	-	V_{p-p}
Tolerable Capacitive Load, GS pin		C_L	-	100	-	pF
Tolerable Resistive Load, GS pin		R_L	-	50	-	kΩ
Common Mode Range	(Note 20)	V_{CM}	-	3.0	-	V_{p-p}

Notes: 16. $V_{SS} \le V_{IN} \le V_{DD}$
17. -3.0V ≤ V_{IN} ≤ +3.0V
18. At 1kHz
19. $R_L \ge 100k\Omega$ to V_{SS}
20. Unloaded

SWITCHING CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; f_C = 3.579545MHz)

Parameter			Symbol	Min	Typ	Max	Units
Tone Present Detection Time			t_{DP}	5	11	14	ms
Tone Absent Detection Time			t_{DA}	0.5	4	8.5	ms
Tone Duration Accept		(Note 21)	t_{REC}	-	-	40	ms
Tone Duration Reject		(Note 21)	t_{REC}	20	-	-	ms
Interdigit Pause Accept		(Note 21)	t_{ID}	-	-	40	ms
Interdigit Pause Reject		(Note 21)	t_{DO}	20	-	-	ms
Propagation Delay (St to Q)		(Note 22)	t_{PQ}	-	8	11	µs
Propagation Delay (St to StD)		(Note 22)	t_{PStD}	-	12	-	µs
Output Data Set Up (Q to StD)		(Note 22)	t_{QStD}	-	3.4	-	µs
Propagation Delay (TOE to Q)	ENABLE	(Note 23)	t_{PTE}	-	50	-	ns
	DISABLE	(Note 23)	t_{PTD}	-	300	-	ns
Clock Input Rise Time			t_{LHCL}	-	-	110	ns
Clock Input Fall Time			t_{HLCL}	-	-	110	ns
Clock Input Duty Cycle			DC_{CL}	40	50	60	%

Parameters measured using test circuit shown in Figure 4.

Notes: 21. User adjustable; see *General Description* on page 5-9.
22. TOE = V_{DD}
23. R_L = 10kΩ, C_L = 50pF

DIGITAL CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; voltages referenced to V_{SS})

Parameter			Symbol	Min	Typ	Max	Units
Digital Inputs	"0" level		V_{IL}	-	-	1.5	V
	"1" level		V_{IH}	3.5	-	-	V
Digital Outputs	"0" level	(Note 24)	V_{OL}	-	-	0.03	V
	"1" level	(Note 24)	V_{OH}	4.97	-	-	V
Output Low (Sink) Current		(Note 25)	I_{OL}	1	2.5	-	mA
Output High (Source) Current		(Note 26)	I_{OH}	0.4	0.8	-	mA
Input Leakage Current		(Note 27)	I_{IH}, I_{IL}	-	0.1	-	µA
Pull Up Source Current		(Note 28)	I_{SO}	-	7.5	15	µA

Notes: 24. No Load
25. V_{OUT} = 0.4V
26. V_{OUT} = 4.6V
27. V_{IN} = V_{SS} or V_{DD}
28. TOE (pin 10) = 0V

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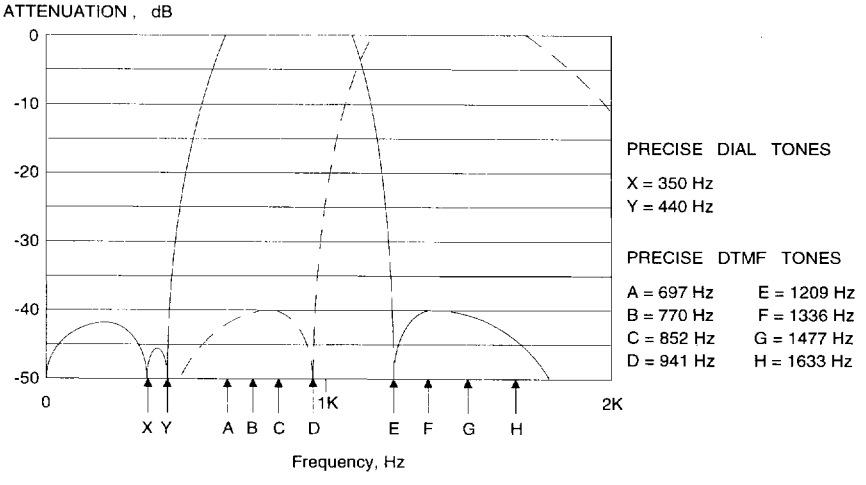
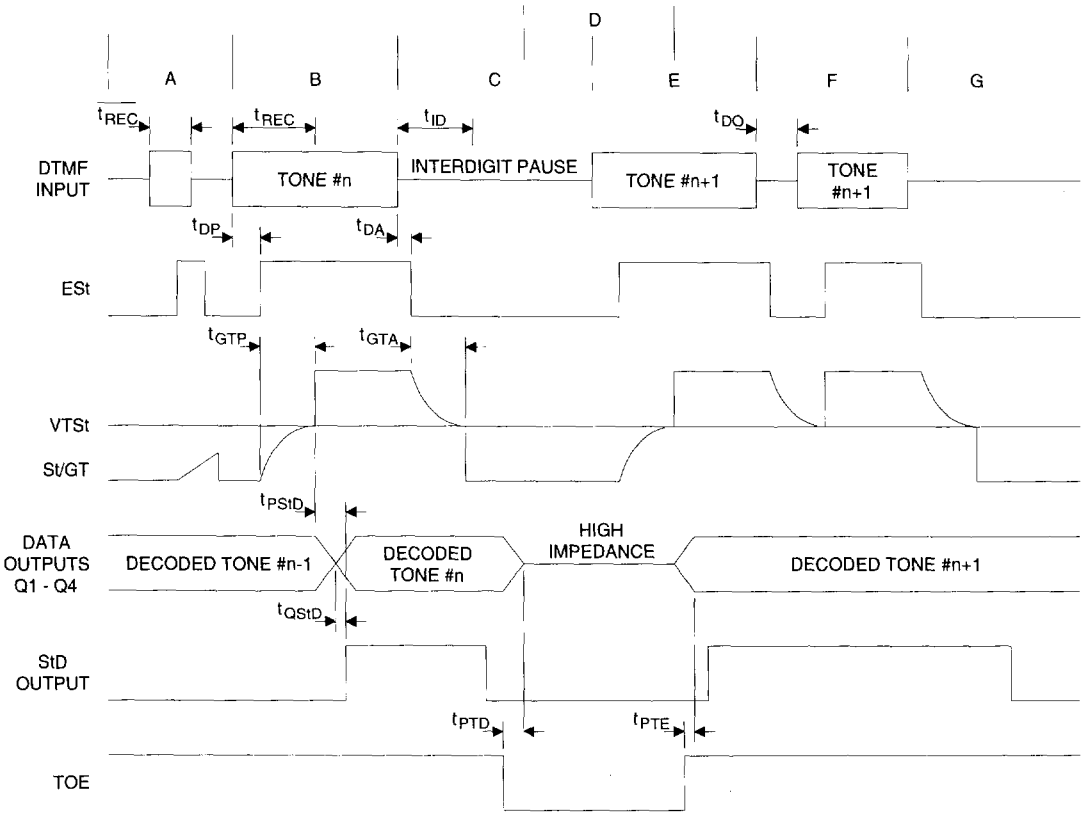


Figure 1. Filter Characteristics



EXPLANATION OF EVENTS

A. Short tone burst is detected, but duration is invalid.
B. Tone #n is detected, and duration is valid. Decoded to outputs.
C. End of tone #n detected and duration is valid. Outputs remain latched until next valid tone.
D. Three state outputs are disabled (high impedance).
E. Tone #n+1 is detected and validated. Decoded to outputs.
F. Three state outputs are enabled. Momentary dropout of tone #n+1 does not register at outputs.
G. End of tone #n+1 detected and validated. Outputs remain latched until next valid tone.

DEFINITION OF SYMBOLS

ESt - EARLY STEERING OUTPUT - Indicates detection of valid DTMF signal.
St/GT - STEERING INPUT/GUARD TIME OUTPUT - Drives external timing circuit.
Q1 - Q4 - DATA OUTPUTS - Gives code corresponding to decoded tone pair.
StD - DELAYED STEERING OUTPUT - Indicates that valid signals have been present (or absent) for the required time.
TOE - TONE OUTPUT ENABLE (Input) - Holding TOE low causes Q1 - Q4 to go to high impedance state.

$\overline{t_{REC}}$ - DTMF singal duration too short to be detected as valid.
t_{REC} - Minimum signal duration required for valid recognition.
t_{ID} - Minimum acceptable time between valid signals.
t_{DO} - Maximum allowable dropout of DTMF signal.
t_{PTD} - Propagation Delay, Disable
t_{PTE} - Propagation Delay, Enable
t_{DP} - Time to detect presence of valid signal.
t_{DA} - Time to detect absence of valid signal.
t_{GTP} - Tone Present Guard Time
t_{GTA} - Tone Absent Guard Time
t_{QStD} - Output Data Setup (Q to StD)
t_{PStD} - Propagation Delay (St to StD)

GENERAL DESCRIPTION

The CS8870 is a complete Dual Tone Multifrequency (DTMF) receiver designed to detect all 16 tone pairs and output a corresponding four bit binary code. This device provides all necessary filtering and requires a minimum of external components. Low power CMOS technology provides the highest performance for the lowest cost.

Filter Section

The CS8870's on chip filtering provides excellent signal-to-noise performance. The DTMF signal is separated into high and low groups using two six pole, bandpass switched capacitor filters. The bandpass filters are elliptical designs with notches placed at 350 Hz and 440 Hz for exceptional dial tone rejection. The output of each bandpass filter contains frequency components from only one DTMF tone group. The filter outputs are smoothed and then limited by high gain comparators, which have hysteresis to reduce sensitivity to unwanted low level signals, jitter, and noise. The comparators' outputs swing from rail to rail at the frequencies of the incoming tones.

Decoder Section

The decoder uses a digital detection algorithm to determine the frequencies of the two tones. The decoder measures the period of the square wave output of the comparators. The period measurement is averaged over a number of cycles and compared to a range of period measurements representing the four possible tones in either band. This averaging prevents DTMF simulation by extraneous signals such as voice, while allowing small frequency deviations in the signal. The averaging algorithm has been optimized to provide excellent immunity to "talk-off" and tolerance to the presence of interfering frequencies (third tones) and noise. When both bands simultaneously decode a valid tone, the Early Steering (ESt) output goes high. Should the DTMF signal be lost, the ESt pin will go low.

Steering Circuit

The receiver verifies that the duration of a valid signal is sufficient before registering a decoded tone pair. Tone detection timing is controlled by an external resistor and capacitor (see Figure 2). After a valid tone is present for t_{DP} (Tone Present Detection Time), ESt goes high, and the capacitor discharges through resistor R. The voltage on the St/GT pin changes as a function of the RC time constant, providing the DTMF signal remains valid. When the capacitor voltage (and the voltage on St/GT) reaches the Steering Threshold Voltage, V_{TSt}, the GT output drives the capacitor voltage to VDD. At this point, the four bit code corresponding to the DTMF signal is latched to the outputs. GT remains high as long as ESt remains high. After the output latches settle, the Delayed Steering Output, StD, goes high, indicating that a valid tone pair has been registered. The code is made available at outputs Q1 - Q4 by pulling the three state control input, TOE, to a logic high.

The steering circuit works in reverse to sense the interdigit pause between signals. When the DTMF signal is removed, the capacitor charges. When the Steering Threshold Voltage is reached, GT is pulled to V_{SS}. This circuit also enables the receiver to tolerate signal dropouts too short to be considered a valid pause.

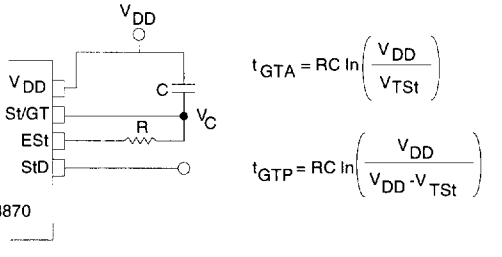


Figure 2 - Basic Steering Circuit

Guard Time Adjustment

The external timing circuitry shown in Figures 2 and 3, enables the user to adjust the timing to meet specific needs. The following formulas, along with the formulas given in Figure 2, are used to determine the resistor and capacitor values.

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

t_{REC} is the minimum signal duration accepted by the receiver. t_{DP} is the Tone Present Detection Time (the time a valid tone must be present before ESt goes high). t_{ID} is the Interdigit Pause Time. t_{DA} is the Tone Absent Detection Time. Values for t_{DP} and t_{DA} are given in the Switching Characteristics Table. Using the configuration shown in Figure 2, and the recommended capacitor value of 0.1µF, a t_{REC} of 40ms is achieved by using a 390kΩ resistor.

Different circuit configurations may be used to independently select Tone Present Guard Time, t_{GTP}, and Tone Absent Guard Time, t_{GTA}, durations. Using the equations and circuits shown in Figure 3, the designer can meet system specifications which place limits on accept and reject times for tone and pause durations, and tailor system parameters such as "talk-off" and noise immunity. For example, increasing recognition time improves talk-off performance (speech immunity) since it reduces the probability that tones simulated by speech remain valid long enough to register.

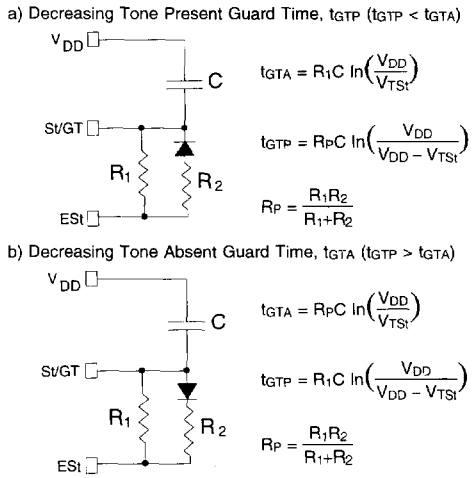


Figure 3 - Steering Circuits for Guard Time Adjustment

Input Configuration

Input signals to the CS8870 pass through an on-chip operational amplifier. A voltage reference, VREF, is provided to bias the input near mid-supply. Figure 4 shows a single ended input configuration with the inputs biased at VREF, and for unity gain. A differential input configuration is shown in Figure 5. The feedback resistor, R5, connected to the op-amp output, GS, can be used to control the gain.

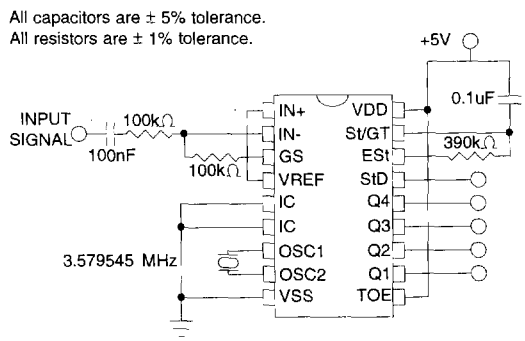
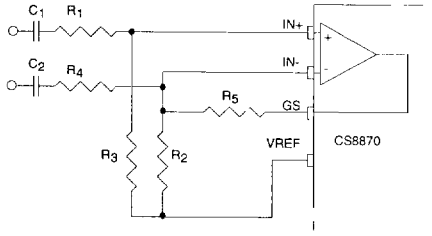


Figure 4 - Single Ended Input Configuration



$C_1 = C_2 = 0.01\mu F$
$R_1 = R_4 = R_5 = 100k\Omega$
$R_2 = 60k\Omega$
$R_3 = 37.5k\Omega$

$$R_3 = \frac{R_2 R_5}{R_2 + R_5}$$

$$\text{Voltage Gain (Av diff)} = \frac{R_5}{R_1}$$

$$\text{Input Impedance } (Z_{IN} \text{ diff}) = 2\sqrt{R_1 + \left(\frac{1}{\omega C}\right)^2}$$

Figure 5 - Differential Input Configuration

F_{LOW}	F_{HIGH}	KEY	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L - LOGIC LOW H - LOGIC HIGH
Z - HIGH IMPEDANCE

Table 1 - Functional Decoding

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Crystal Oscillator

An external 3.579545 MHz (TV colorburst) crystal must be connected across pins OSC1 and OSC2 to complete the internal clock circuit. Up to ten CS8870s may be driven by one crystal by connecting the oscillator output, OSC2, with the oscillator input, OSC1, of another device through a 30pf capacitor. Refer to Figure 6.

Logic high on TOE enables the data output pins to output code for the last valid DTMF signal received. Q1 is the LSB. These outputs go to a high impedance state when TOE is low. See the Functional Decode table, Table 1.

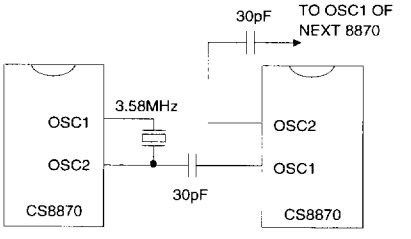


Figure 6 - Oscillator Interconnection

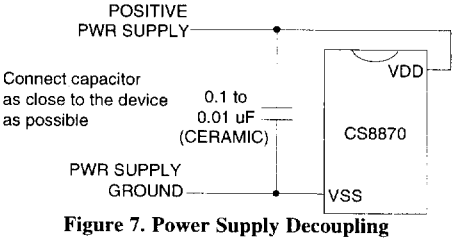
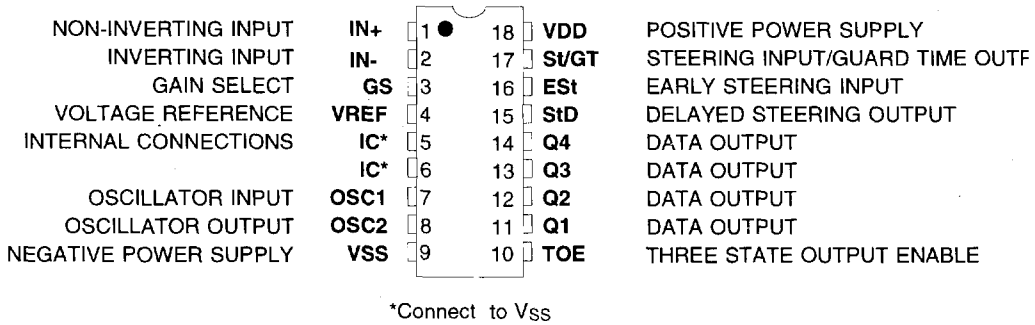


Figure 7. Power Supply Decoupling

PIN DESCRIPTIONS



*Connect to V_{SS}

Power Supplies

VDD - Positive Power Supply Input, PIN 18.

Normally connected to +5 volts. A 0.01µF to 0.1µF ceramic capacitor should be connected as close to the device as possible across V_{DD} and V_{SS}. (See Figure 7).

VSS - Negative Power Supply Input, PIN 9.

Normally connected to 0 volts.

Oscillator

OSC1; OSC2 - Oscillator Input, PIN 7; Oscillator Output, PIN 8.

A 3.579545 MHz crystal connected across these pins completes the internal clock circuit.

Inputs

St/GT - Steering Input/Guard Time Output, PIN 17.

When the voltage on this pin rises past the Steering Threshold Voltage, V_{TSt}, the device registers the detected tone pair, updates the output latch, and drives this pin to a logic high. When the voltage on this pin falls below V_{TSt}, this pin goes to a logic low, freeing the device to accept a new tone pair. The Guard Time Output's function is to reset the external steering time constant. The state of GT is a function of ESt and St.

IN+ - Non-Inverting Input, PIN 1.

Non-inverting input to the front end operational amplifier.

IN- - Inverting Input, PIN 2.

Inverting input to the front end operational amplifier.

TOE - Three State Output Enable, PIN 10.

Logic high on this pin enables outputs Q1 - Q4. Internal pull up.

Outputs

GS - Gain Select, PIN 3.

Connected to the output of the front end operational amplifier. Gain applied to the input can be controlled by a feedback resistor at this pin.

VREF - Voltage Reference, PIN 4.

Voltage on this pin is nominally 2.5 VDC independent of power supply, and may be used to bias inputs at mid supply.

Q1, Q2, Q3, Q4 - Data Outputs, PINS 11, 12, 13, 14.

Logic high on TOE enables pins to output code for last valid DTMF signal received. Q1 is the LSB. These outputs go to a high impedance state when TOE is low. See Functional Decode Table.

StD - Delayed Steering Output, PIN 15.

Outputs a logic high when voltage on St/GT exceeds V_{TSt} and the output latch has been updated with code from the received tone pair. StD goes to a logic low when voltage on St/GT falls below V_{TSt}.

ESt - Early Steering Output, PIN 16.

Goes to a logic high whenever the detection algorithm detects a valid tone pair. Any loss of a valid DTMF signal causes the output to go to a logic low

IC, IC - Internal Connection, PINS 5, 6.

Both pins must be tied to V_{SS}.