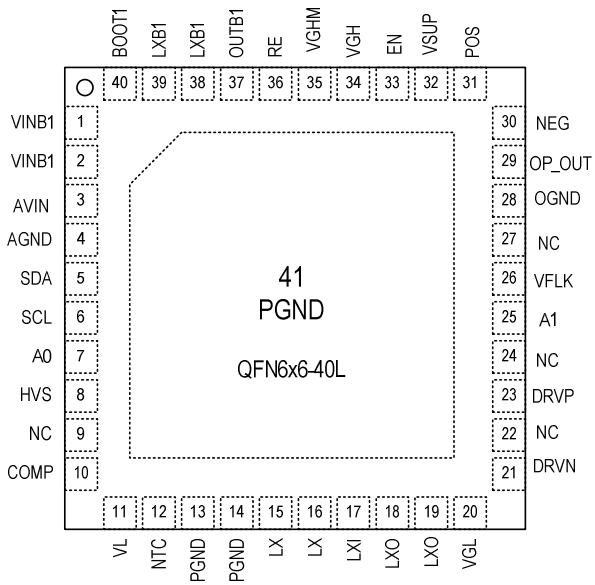
General Description

The CS902-A-R offers a compact power supply solution to provide all voltages required by a TFT-LCD panel. With its high current capabilities, the device is ideal for large screen LCD monitors panels and TV applications with 12V supply voltage. CS902-A-R is available in a QFN 6x6-40L package.

Feature

- **8V to 14V Input Supply Voltage**
- **Sync-Boost Regulator for AVDD with 13.5V to 19.8V Programmable Output and Current Limit**
- **Buck Regulator for VI/O with 2.2V to 3.7V Programmable Output**
- **Positive Charge Pump Regulator for VGH with 20V to 40V Programmable Output and 0V to 15V Gate Shaping Voltage**
- **Negative Charge Pump Regulator for VGL with -4.5V to -13.5V Programmable Output**
- **20V OPAMP with ±300mA Output Short Current**
- **Temperature Compensation for VGH**
- **Isolation Switch Function for AVDD**
- **Programmable Sequencing**
- **Fixed Switching Frequency 750kHz**
- **Over-Temperature Protection**
- **I²C-Compatible Interface for Register Control**
- **Thin QFN 6x6 40-Lead Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Pin Configurations



Applications

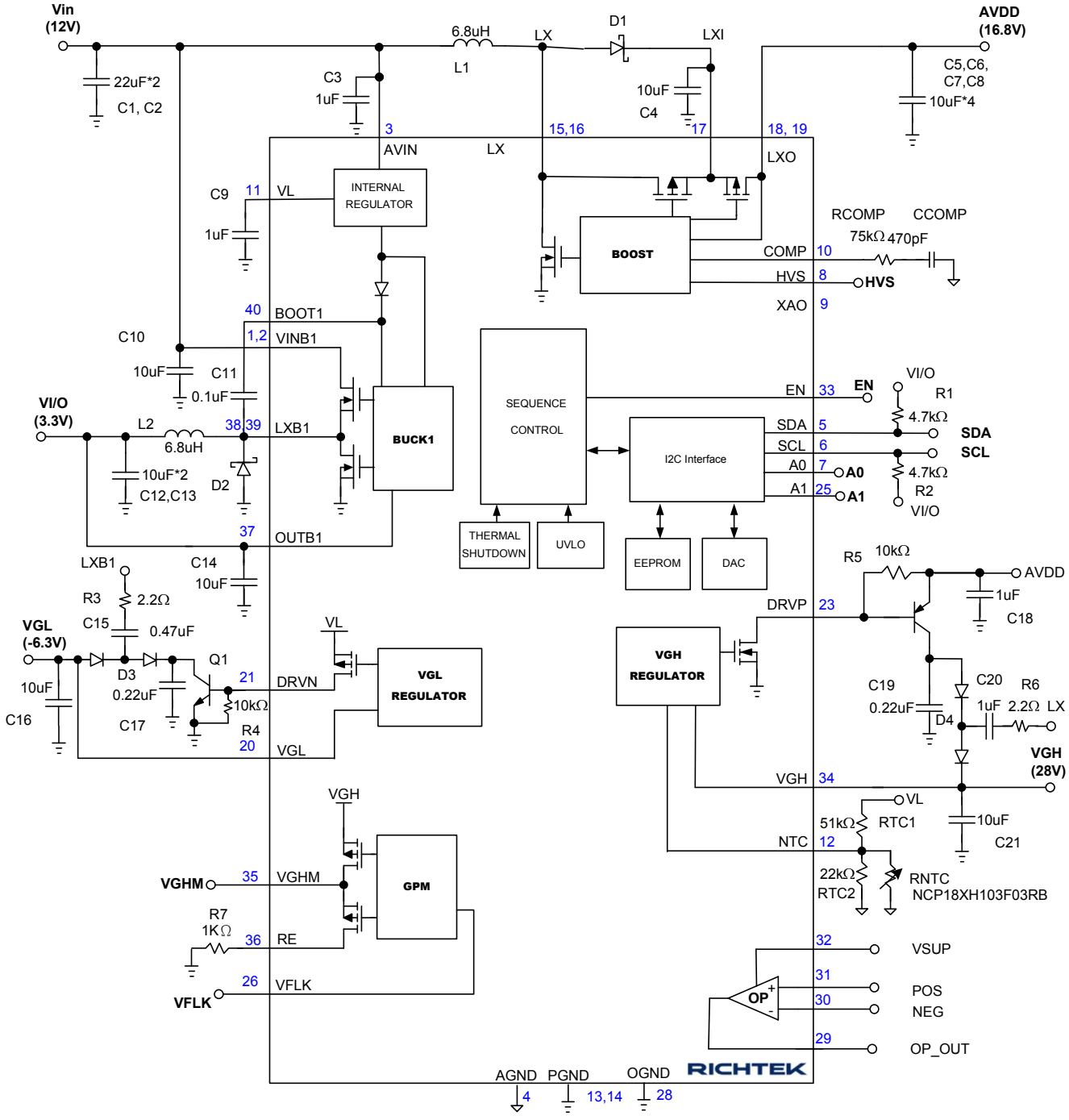
- **TFT LCD Monitor Panel**
- **TFT LCD TV Panel**

Pin Assignment

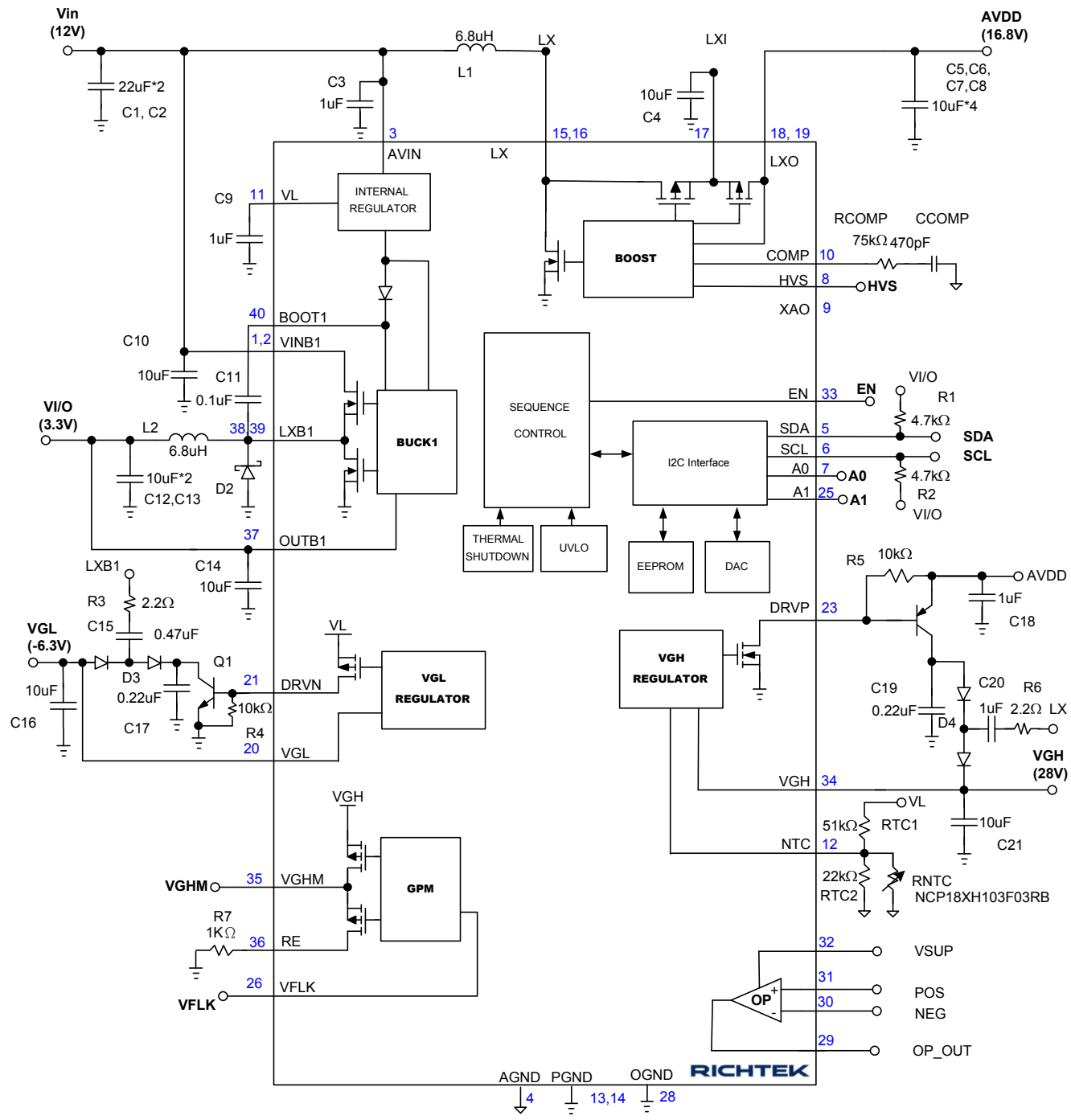
Pin Number	Pin Name	Pin Function
1,2	VINB1	Power input voltage pins for the VI/O buck converter. VINB1 is internally connected to VINB3.
22,24,27	NC	Not connected. Should be floating or connected to GND
3	AVIN	Analog input voltage of the device. This is the input for the analog circuits. Connect this pin with a decoupling capacitor.
4	AGND	Analog ground.
5	SDA	I^2C compatible serial-data input/output.
6	SCL	I^2C compatible serial-clock input.
7	A0	I^2C compatible device address bit 0.
8	HVS	Boost HVS enable.
9	NC	Not connected. Should be floating.
10	COMP	Compensation pin for the boost converter.
11	VL	Internal logic regulator output. Connect this pin with a decoupling capacitor.
12	NTC	Temperature compensation pin for VGH.
13,14	PGND	Power ground.
15,16	LX	Switch pins of the boost converter.
17	LXI	High side switch input pin.
18,19	LXO	High side switch output pin. Also used for feedback of the boost converter
20	VGL	Output sensing pin of the VGL negative charge pump.
21	DRVN	Base drive of the external NPN transistor for the VGL negative charge pump.
23	DRVP	Base drive of the external PNP transistor for the VGH positive charge pump.
25	A1	I^2C compatible device address bit 1.
26	VFLK	Gate Shaping Control Input. When VFLK is high, the switch between VGH and VGHM is on and the switch between VGHM and RE is off. When VFLK is low, the switch between VGH and VGHM is off and the switch between VGHM and RE is on.
28	OGND	GND of OPAMP.
29	OP_OUT	OUTPUT of OPAMP.
30	NEG	Negative Input of OPAMP
31	POS	Positive Input of OPAMP

32	VSUP	VDD of OPAMP.
33	EN	Chip enable
34	VGH	Output sensing pin for the VGH positive charge pump and power input voltage pin for the GPM.
35	VGHM	Switch output for gate shaping function.
36	RE	Discharge pin for gate shaping function.
37	OUTB1	Output sensing pin of the VI/O buck converter.
38,39	LXB1	Switch pins of the VI/O buck converter.
40	BOOT1	N-channel MOSFET gate drive voltage for the VI/O buck converter. Connect a capacitor from the switch node LXB1 to this pin.
41	Exposed Pad	The Exposed Pad should be soldered to a large PCB and connected to PGND for maximum thermal dissipation.

Function Block Diagram: CS902-A-R



Function Block Diagram: Sync-Boost



Operation

Power Sequence Timing Diagram

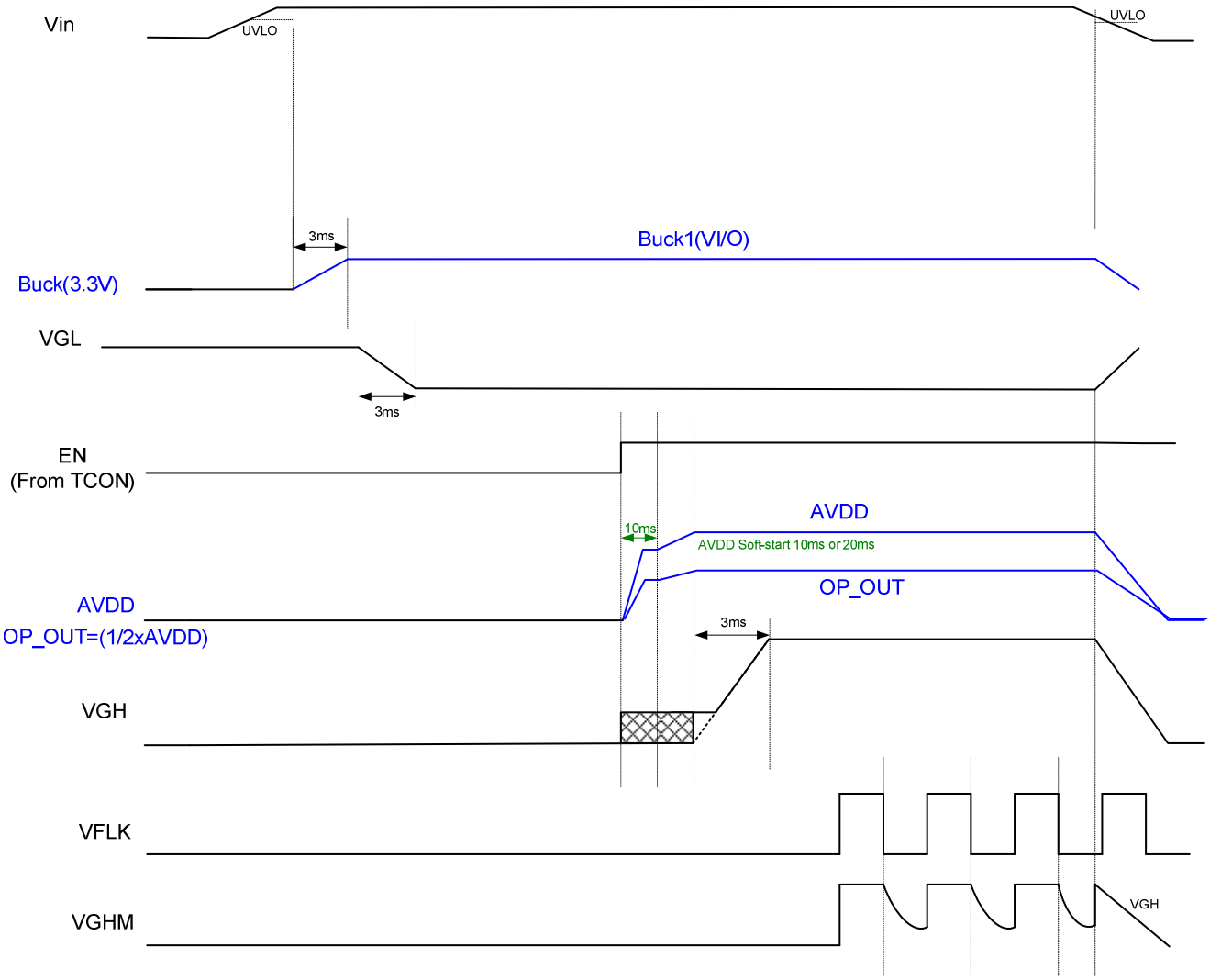


Figure 1. Power sequence

Absolute Maximum Ratings (Note 1)

EN, AVIN, VINB1, LXI, LXO, POS, NEG, OP_OUT to PGND ---------- –0.3 to 24V

POS to NEG ---------- –0.3 to 10V

LX to PGND ---------- –0.3 to 24V

VL, NTC, COMP, SDA, SCL, A1, A0, HVS, OUTB1, to PGND ---------- –0.3 to 6V

LXB1 to PGND ---------- 0.3 to (VINBx+0.3V)

BOOT1 to LXB1 ---------- –0.3 to 6V

DRVN to PGND ---------- –0.3 to 6V

VGHM, RE, DRVP to PGND ---------- –0.3 to +40V

VGL to VL ---------- –24V to +0.3V

PGND to AGND ---------- ±0.3V

PGND to AGND ---------- ±0.3V

- Power Dissipation, P_D @ T_A = 25°C

VQFN-40L 6x6 ---------- 3.2W

- Package Thermal Resistance (Note 2)

VQFN-40L 6x6, θ_{JA} ---------- 32.5°C/W

VQFN-40L 6x6, θ_{JC} ---------- 6.5°C/W

- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

HBM (Human Body Model) ---------- 2kV

MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 3)

- Junction Temperature Range---------- –40°C to 125°C
- Ambient Temperature Range---------- –40°C to 85°

Electrical Characteristics

(Typical values V_{IN}=12V, EN=high, V_{AVDD}=16V, Buck1($V_{I/O}$)=3.3V, V_{GH}=26V, V_{GL}=-5V with typical values T_A = 25 C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Input Voltage Range	V_{IN}		8		14	V
Quiescent Current into AVIN	I_{QIN}	LX, LXB1 switching		7		mA
Quiescent Current into VINB1		LX, LXB1 not switching		0.2		
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling, hysteresis 400mV		6.8		V

VL Output Voltage	V_L			5		V
Out Voltage Tolerance	ΔV_L	Out Voltage Tolerance	-1		+1	%
FAULT DETECTION						
Fault Trigger Duration				50		ms
Thermal Shutdown Threshold		Temperature rising	--	150	--	°C
LOGIC INPUTS(SDA, SCL, HVS, EN, VFLK)						
Input High Voltage	V_{IH}		1.7			V
Input Low Voltage	V_{IL}				0.6	V
Input Leakage Current	I_{IH}, I_{IL}	V_{IN}=0 or 3.3V	-1	+0.01	+1	µA
Input Capacitance				5		pF
SDA Output Low Voltage	V_{OL}	I_{SINK}=6mA		0.3		V
I^2C TIMING CHARACTERISTICS						
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		800	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R		20+0.1 C_B		300	ns
SDA and SCL Receiving Fall Time	t_F		20+0.1 C_B		300	ns
SDA Transmitting Fall Time	t_F		20+0.1 C_B		250	ns
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}				50	ns
INTERNAL OSCILLATOR						
Oscillator Frequency	F_{osc}		600	750	900	kHz
Maximum Duty Cycle				90		%

SYNC-BOOST CONVERTER (AVDD)						
LXO Regulation Voltage Range	V_{LXO}	HVS=0, programmable step 0.1V	13.5		19.8	V
LXO Regulation Voltage Tolerance			-1%		+1%	
HVS Voltage	V_{HVS}	Programmable step 0.2V	0		3	V
Low Side LX On-Resistance	$R_{DS(ON)}$	I_{LX} = 500 mA.		100		mΩ
Low Side LX Current Limit	I_{LIM}		4.25	5	5.75	A
Low Side LX Current Limit negative offset		current limit value= Ityp - offset register value x 0.4(A)	0		2.8	A
Switch Leakage Current	I_{leak}	V_{LX} = 16.5 V		1	10	uA
Soft-start time			--	10	20	ms
LXI Over-Voltage Protection	V_{OVP}	V_{LXI} rising, hysteresis = 1.5V	20.5	21.5	22.5	V
LXO Line Regulation		8V ≤ V_{IN} ≤ 14V, I_{out} = 1mA		±0.08		%/V
LXO Load Regulation		1mA ≤ I_{out} ≤ 2A		±1		%/A
Trans-Conductance of Error Amplifier	Gm			240		uA/V
Gain of Error Amplifier	Av			1000		V/V
LXO Fault Trip Level		V_{LXO} falling		80		%
High Side LX On-Resistance	$R_{DS(ON)}$	I_{SW} = 0.2A.		400		mΩ
Short-Circuit Trigger Duration		I_{SW} ≥ 2.5A.		1.5		ms
		I_{SW} ≥ 4.5A.		100		us
BUCK1 CONVERTER ($V_{I/O}$)						
OUTB1 Regulation Voltage Range	V_{OUTB1}	Programmable step 0.1V	2.2		3.7	V
OUTB1 Regulation Voltage Tolerance		Iload = 10mA	-2%		+2%	V
LXB1 to VINB1 N-MOSFET On-Resistance	$R_{DS(ON)}$	I_{LXB1} = 500 mA		150		mΩ
LXB1 Positive Current Limit	I_{LIM}		3.0	3.5	4.0	A
LXB1 to PGND N-MOSFET On-Resistance				6		Ω
OUTB1 Line Regulation		8V ≤ V_{IN} ≤ 14V, I_{out} = 1mA		0.005		%/V
OUTB1 Load Regulation		1mA ≤ I_{out} ≤ 2.5A		0.25		%/A
Soft Start Period	T_{SS}			3		ms
OUTB1 Fault Trip Level		V_{OUTB1} falling		80		%
POSITIVE CHARGE PUMP CONTROLLER (VGH)						

VGH_L Regulation Voltage Range	V_{VGH_L}	Programmable step 1V	20		35	V
VGH_H Offset Voltage	V_{VGH_OS}	$V_{VGH\_H}=V_{VGH\_L}+V_{VGH\_OS}$, programmable step 1V	0		15	V
VGH_H Regulation Voltage Range	V_{VGH_H}		20		40	V
DRVP Sink Current	I_{DRVP}	$V_{GH} = V_{VGHnominal}$ - 5%	--	3.5	--	mA
		V_{GH} < 20%		80		uA
Out Voltage Tolerance	V_{GH}		-2%		+2%	
VGH Load Regulation Error		V_{DRVP}=16V, 50uA<I_{DRVP}<1mA		120		mV/mA
Soft Start Period	T_{SS}			3		ms
VGH Fault Trip Level		V_{GH} falling		80		%
NEGATIVE CHARGE PUMP CONTROLLER (VGL)						
VGL Output Voltage VGL Programmable	VGL	Programmable Step 0.6V	−13.5	--	−4.5	V
DRVN Source Current	IDRVN	VDRVN = 0.6V, VGL= VGL(nominal) + 0.05V	--	3.5	--	mA
Regulation Voltage Tolerance		VDRVN = 0.6V, IDRVN = −100 μ A	-1	--	1	%
VGL Load Regulation Error		VDRVN = 0.6V, −50 μ A < IDRVN < −1mA	--	11	25	mV/mA
Soft-Start Period	tSS			3		ms
VGL Fault Trip Level		VGL Rising	VGL + 1.5		VGL + 2.5	V
Gate Pulse Modulation(GPM)						
Gate shaping lower limit voltage		Programmable step 5V	0		15	V
VGH-to-VGHM Switch On-resistance		VFLK=high		3	5	Ω
VGHM-to-RE Switch On-Resistance		VFLK=low		3	5	Ω
OPAMP						
Supply Current	IOP			4		mA
Input Offset Voltage	VOS	VCOM = AVDD/2		2	20	mV
Output Voltage Swing High	VOH	ILOAD = 50mA	Vs+ -1.5	Vs+ -0.6	--	V
Output Voltage Swing Low	VOL	ILOAD = −50mA		0.6	1.5	V
Short Circuit Current		To AVDD/2 Source or Sink for 1ms	300	350	400	mA

−3dB Bandwidth	F3dB	RL = 10kΩ, CL = 10pF		16		MHz
Gain Bandwidth Product	GBW	RL = 10kΩ, CL = 10pF		12		MHz
Slew Rate				35		V/us

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. $_{JA}$ is measured in the natural convection at T_A = 25 C on the high effective thermal conductivity four layers thermal test board of JEDEC 51-7 thermal measurement standard. The case point of $_{JC}$ is on the expose pad.

I2C Command

Slave Address

7	6	5	4	3	2	1	0=R/W
0	1	0	0	0	A1	A0	0=W;1=R

Write Command

(a) Write single byte to DAC Register

Example: Writing 29h to DAC address 07h (BK1_OUT)

START	0	1	0	0	0	A1	A0	0	SLAVE ACK	0	0	0	0	0	1	1	1	SLAVE ACK	0	0	1	0	1	0	0	1	STOP

(b) Write all data to Memory from DAC Register

Example: Writing data to Memory from DAC register

START	0	1	0	0	0	A1	A0	0	SLAVE ACK	1	1	1	1	1	1	1	1	SLAVE ACK	0	1	0	1	0	0	0	1	STOP

Read Command

(a) Read data from DAC Register

Example: Reading data from DAC register address 08h, 09h, 0Ah, 0Bh

START	0	1	0	0	0	A1	A0	0	SLAVE ACK	1	1	1	1	1	1	1	1	SLAVE ACK	0	0	0	0	0	0	0	0	SLAVE ACK	STOP
START	0	1	0	0	0	A1	A0	0	SLAVE ACK	0	0	0	0	1	0	0	0	SLAVE ACK										
START	0	1	0	0	0	A1	A0	1	SLAVE ACK	D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master ACK	
	D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master N-ACK	STOP									

(b) Read data from EEPROM

Example: Reading data from EEPROM address 03h, 04h, 05h, 06h

START	0	1	0	0	0	A1	A0	0	SLAVE ACK	1	1	1	1	1	1	1	1	SLAVE ACK	0	0	0	0	0	0	0	1	SLAVE ACK	STOP
START	0	1	0	0	0	A1	A0	0	SLAVE ACK	0	0	0	0	0	0	1	1	SLAVE ACK										
START	0	1	0	0	0	A1	A0	1	SLAVE ACK	D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master ACK	
	D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master N-ACK	STOP									

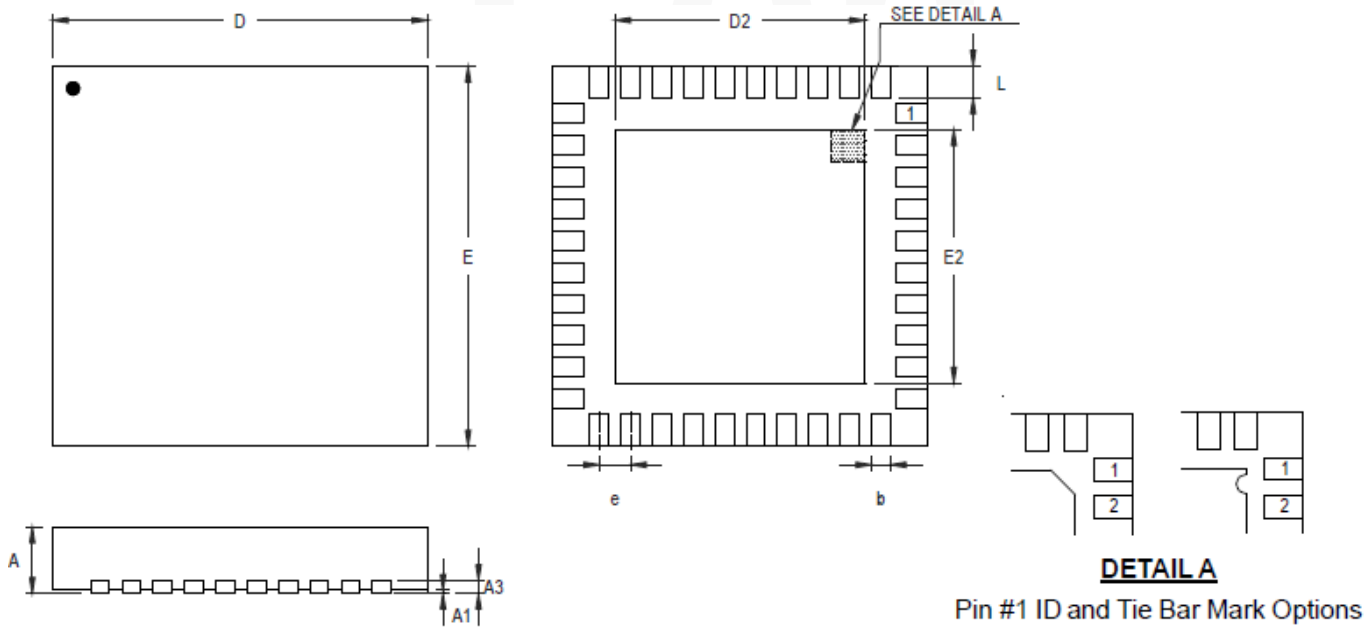
Register Map

Channel	Address	Range	Resolution	MTP Factory Initialization Value	Bit (Step)
Channel Disable Register	00h	0h ~ 3Fh	--	00h	8bits
AVDD	01h	13.5V(00h) ~ 19.8V(3Fh)	0.1V	15V(15h)	6bits (64 steps)
HVS	02h	0V(0h) ~ 3V(Fh)	0.2V	1.6V(08h)	4bits (16 steps)
AVDD OCP (Negative offset)	03h	0A(0h) ~ 2.8A(7h)	0.4A	1.6A(04h)	3bits (8 steps)
AVDD Soft-Start Time	04h	10ms(0h) ~ 20ms(1h)	10ms	10ms(0h)	1bits (2 steps)
Buck1 (VI/O)	05h	2.2V(0h) ~ 3.7V(Fh)	0.1V	3.3V(11h)	4bits (16 steps)
VGH_L	06h	20V(0h) ~ 35V(Fh)	1V	33V(13h)	4bits (16 steps)
VGH_H Offset	07h	0V(0h) ~ 15V(Fh)	1V	8V(08h)	4bits (16 steps)
GPM stop level	08h	5V(1h) ~ 15V(3h)	5V	5V(01h)	2bits (4 steps)
VGL	09h	-13.5V(Fh) ~ -4.5V(0h)	0.6V	-6.3V(03h)	4bits
Control Register1	FFh	00h: Read data form DAC register 01h : Read data form EEPROM register 51h : Write all DAC into EEPROM A1h: All EEPROM to DAC register	--	01h	8bits

Channel Disable Register (Address 00h)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Reserved	Reserved	Reserved	OPAMP 0 : Enable 1 : Disable	VGH 0 : Enable 1 : Disable	VGL 0 : Enable 1 : Disable	GPM 0 : Enable 1 : Disable	NTC 0 : Enable 1 : Disable

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	5.950	6.050	0.234	0.238
D2	4.000	4.750	0.157	0.187
E	5.950	6.050	0.234	0.238
E2	4.000	4.750	0.157	0.187
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 6x6 Package

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