



CS9N90 AKRD-G

General Description:

CS9N90 AKRD-G, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-247, which accords with the RoHS standard.

Features:

- I **Fast Switching**
- I **Low ON Resistance**($R_{dson} \leq 1.1\Omega$)
- I **Low Gate Charge** (Typical Data: 57.9nC)
- I **Low Reverse transfer capacitances**(Typical: 11.3pF)
- I **100% Single Pulse avalanche energy Test**
- I **Halogen Free**

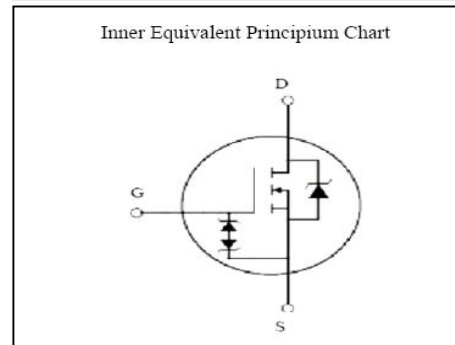
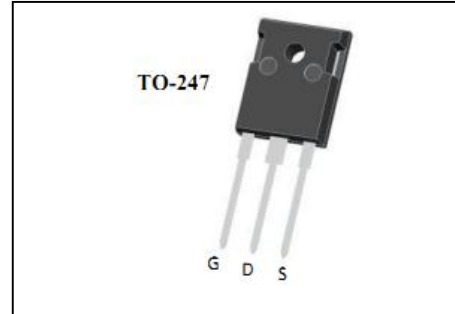
Applications:

PC power and Inverter.

Absolute ($T_J = 25^\circ\text{C}$ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	900	V
I_D	Continuous Drain Current $T_C = 25^\circ\text{C}$	9	A
	Continuous Drain Current $T_C = 100^\circ\text{C}$	5.4	A
I_{DM}^{a1}	Pulsed Drain Current $T_C = 25^\circ\text{C}$	36	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}^{a2}	Single Pulse Avalanche Energy	1035	mJ
dv/dt^{a3}	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	250	W
	Derating Factor above 25°C	2	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5k Ω)	3000	V
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ\text{C}$
T_L	Maximum Temperature for Soldering	300	$^\circ\text{C}$

V_{DSS}	900	V
I_D	9	A
$P_D(T_C=25^\circ\text{C})$	250	W
$R_{DS(ON)Typ}$	0.9	Ω



Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	900	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	$I_D=250\mu A, \text{Reference } 25^\circ\text{C}$	--	0.9	--	V/°C
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=900V, V_{GS}=0V, T_J=25^\circ\text{C}$	--	--	25	μA
		$V_{DS}=720V, V_{GS}=0V, T_J=125^\circ\text{C}$	--	--	250	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20V$	--	--	10	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20V$	--	--	-10	μA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=4.5A$	--	0.9	1.1	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	--	4.0	V
Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	$V_{DS}=15V, I_D=4.5A$	--	11.3	--	S
R_g	Gate resistance	$f=1.0\text{MHz}$	--	3.2	--	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V, f=1.0\text{MHz}$	--	2716	--	pF
C_{oss}	Output Capacitance		--	211	--	
C_{rss}	Reverse Transfer Capacitance		--	11.3	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=9A, V_{DD}=450V, R_G=10\Omega$	--	30.4	--	ns
t_r	Rise Time		--	41.6	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	82	--	
t_f	Fall Time		--	52	--	
Q_g	Total Gate Charge	$I_D=9A, V_{DD}=720V, V_{GS}=10V$	--	57.9	--	nC
Q_{gs}	Gate to Source Charge		--	10.6	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	23.4	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	9	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	36	A
V_{SD}	Diode Forward Voltage	$I_S=9A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=9A, T_j = 25^\circ C$ $dI_F/dt=100A/us,$ $V_{GS}=0V$	--	845	--	ns
Q_{rr}	Reverse Recovery Charge		--	8030	--	nC
I_{RRM}	Reverse Recovery Current		--	19.1	--	A
Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	0.49	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	40	$^\circ C/W$

Gate-source Zener diode						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{GSO}	Gate-source breakdown voltage	$I_{GS} = \pm 1mA$ (Open Drain)	30			V
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.						

^{a1}: Repetitive rating; pulse width limited by maximum junction temperature

^{a2}: $L=10mH, I_D=14A, Start T_j=25^\circ C$

^{a3}: $I_{SD}=9A, di/dt \leq 100A/us, V_{DD} \leq BV_{DS}, Start T_j=25^\circ C$

Characteristics Curve:

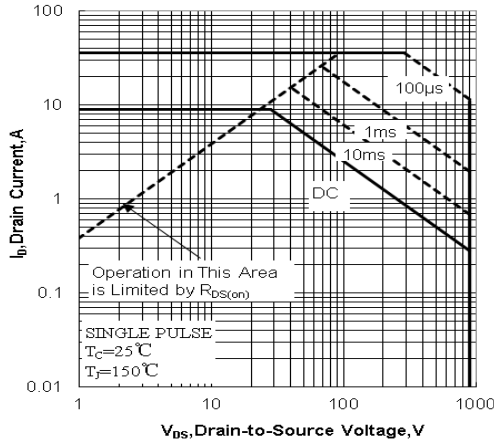


Figure 1 Maximum Forward Bias Safe Operating Area

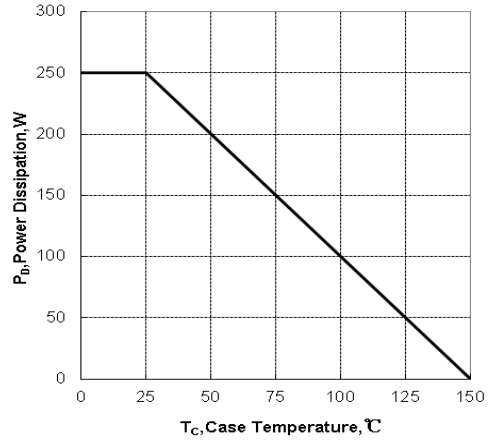


Figure 2 Maximum Power dissipation vs Case Temperature

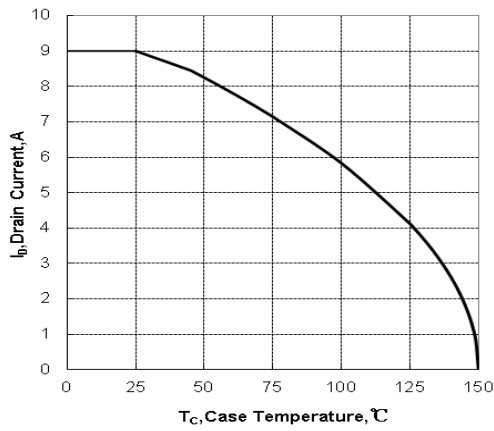


Figure 3 Maximum Continuous Drain Current vs Case Temperature

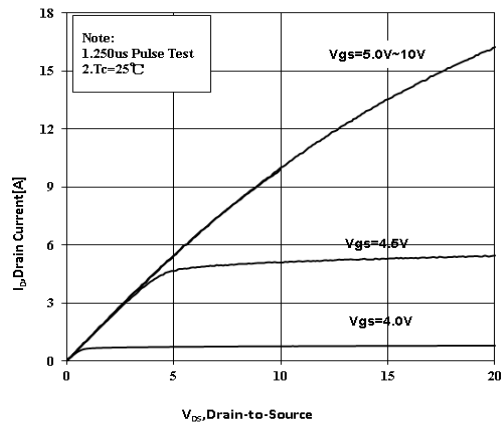


Figure 4 Typical Output Characteristics

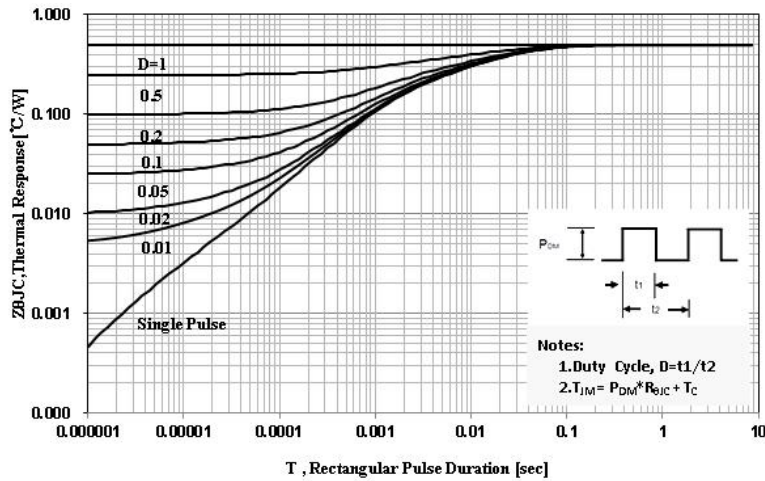


Figure 5 Maximum Effective Thermal Impedance, Junction to Case

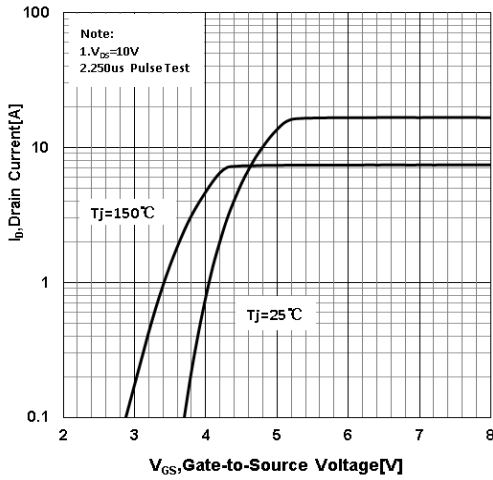


Figure 6 Typical Transfer Characteristics

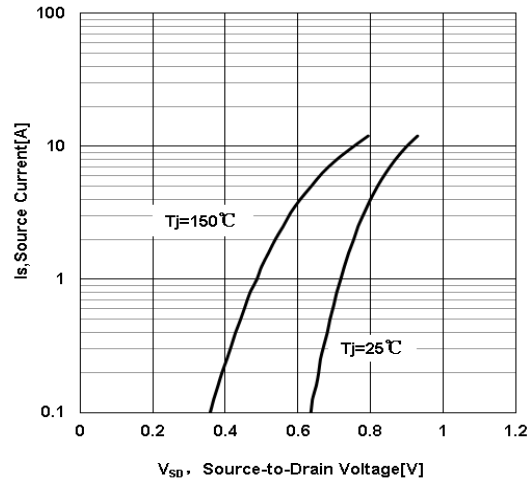


Figure 7 Typical Body Diode Transfer Characteristics

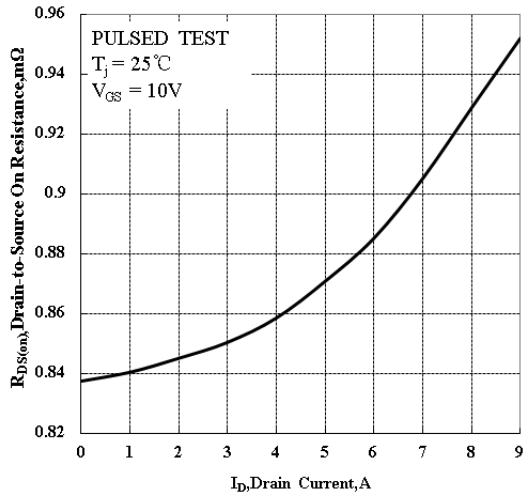


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

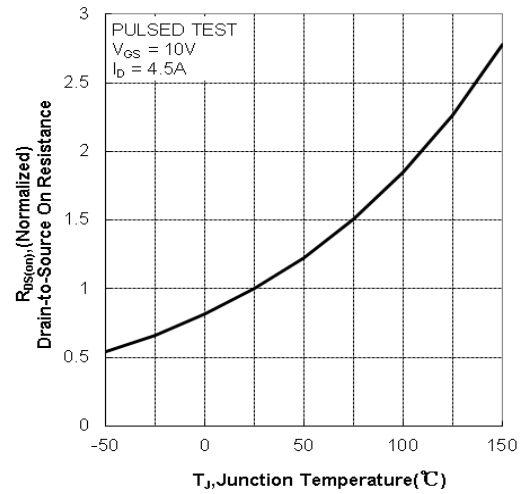


Figure 9 Typical Drain to Source on Resistance vs Junction Temperature

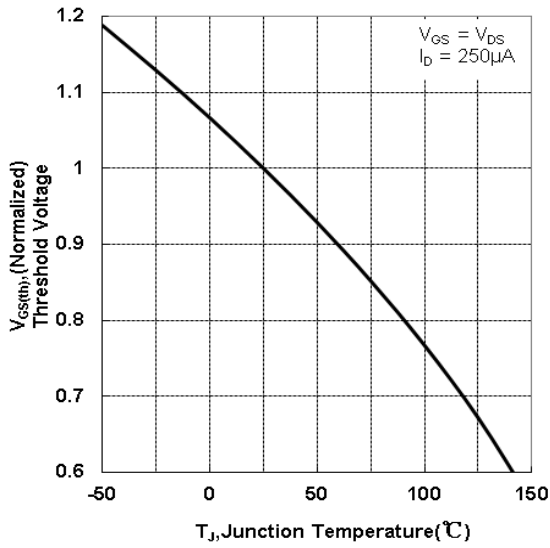


Figure 10 Typical Theshold Voltage vs Junction Temperature

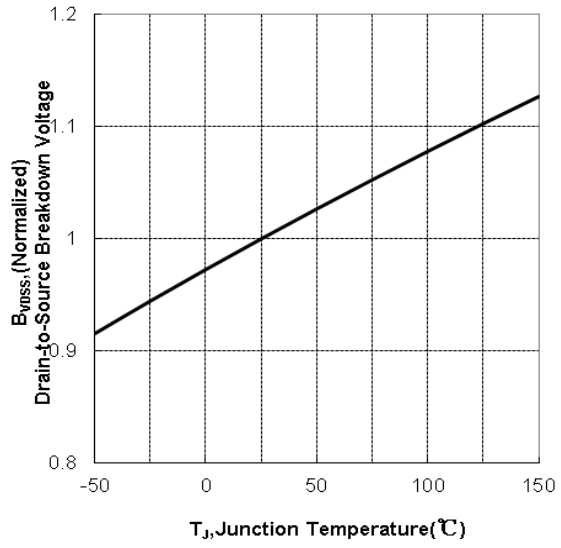


Figure 11 Typical Breakdown Voltage vs Junction Temperature

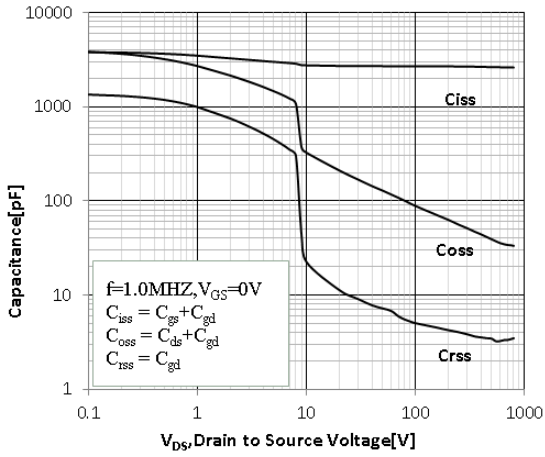


Figure 12 Typical Capacitance vs Drain to Source Voltage

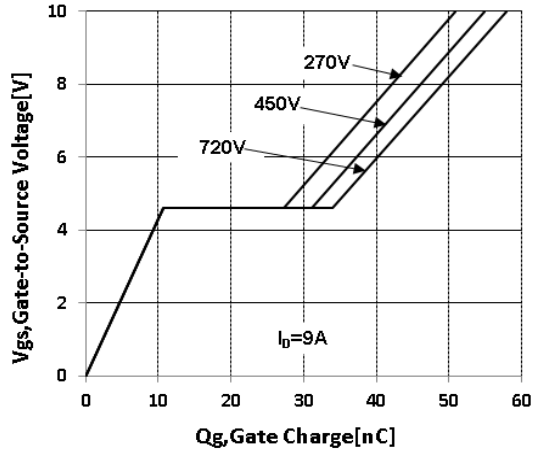


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform



Figure 14. Gate Charge Test Circuit



Figure 15. Gate Charge Waveforms



Figure 16. Resistive Switching Test Circuit



Figure 17. Resistive Switching Waveforms



Figure 18. Diode Reverse Recovery Test Circuit



Figure 19. Diode Reverse Recovery Waveform



Figure 20. Unclamped Inductive Switching Test Circuit

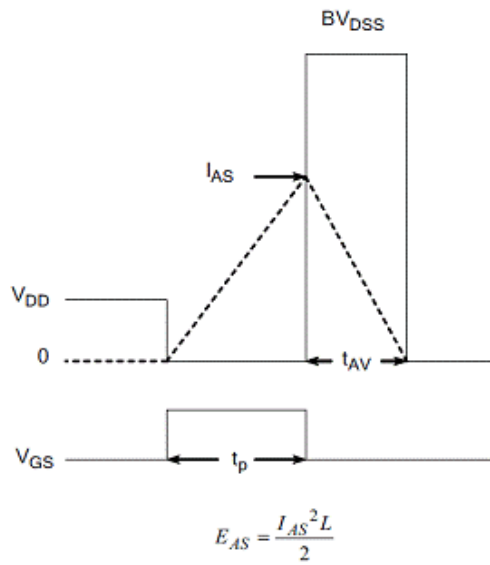
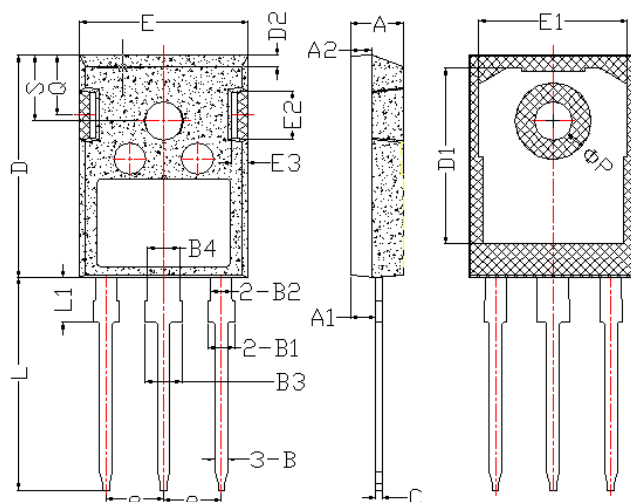


Figure 21. Unclamped Inductive Switching Waveform

Package Information


项 目	规范(mm)	
	MIN	MAX
A	4.6	5.2
A1	2.2	2.6
B	0.9	1.4
B1	1.75	2.35
B2	1.75	2.15
B3	2.8	3.35
B4	2.8	3.15
C	0.5	0.7
D	20.60	21.30
D1	16	18
E	15.5	16.10
E1	13	14.7
E2	3.80	5.3
E3	0.8	2.60
e	5.2	5.7
L	19	20.5
L1	3.9	4.6
ΦP	3.3	3.70
Q	5.2	6.00
S	5.8	6.6

TO-247 Package



The name and content of poisonous and harmful material in products

Part's Name	Hazardous Substance									
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE	DBP	DEHP	DBP	BBP
Limit	≤0.1%	≤0.1%	≤ 0.01%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%
Lead Frame	○	○	○	○	○	○	○	○	○	○
Molding	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
Wire Bonding	○	○	○	○	○	○	○	○	○	○
Solder	×	○	○	○	○	○	○	○	○	○
Note	○: Means the hazardous material is under the criterion of 2011/65/EU. ×: Means the hazardous material exceeds the criterion of 2011/65/EU. The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup's RoHS.									

Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heatsink, please pay attention to the torsional moment and the smoothness of the heatsink.
3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. This publication is made by Huajing Microelectronics and subject to regular change without notice.

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