

N-Channel Trench Power MOSFET

General Description

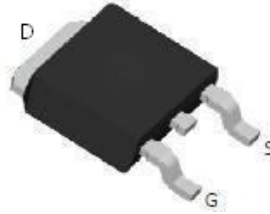
The CSD01N650 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for power switching application and LED backlighting.

Features

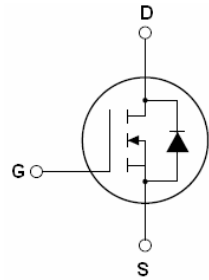
- $V_{DS}=100V$; $I_D=11A$
 $R_{DS(ON)} < 140m\Omega$ @ $V_{GS}=10V$ (Typ:90m Ω)
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Power switching application
- LED backlighting



To-252 Top View



Schematic Diagram

$$V_{DS} = 100V$$

$$I_D = 11A$$

$$R_{DS(ON)} = 90m\Omega$$

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
CSD01N650	CSD01N650	TO-252	-	-	-

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	100	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 20	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	11	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	7.7	A
$I_{DM(Pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	44	A
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	45	W
E_{AS}	Single Pulse Avalanche Energy (Note 2)	16	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, V_{DD}=50V, V_G=10V, R_G=25\Omega$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	---	3.3	$^{\circ}C/W$

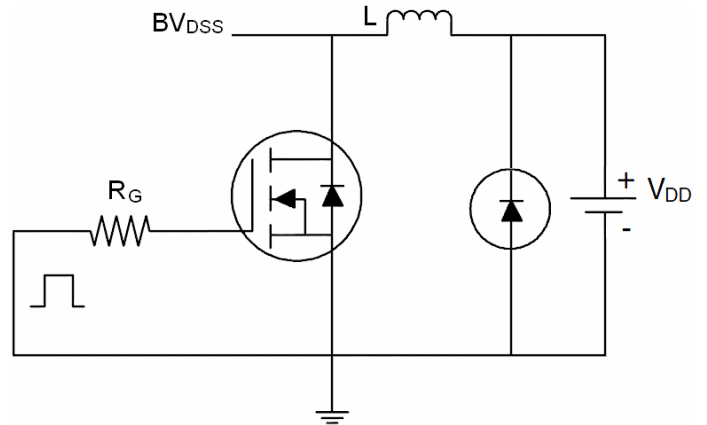
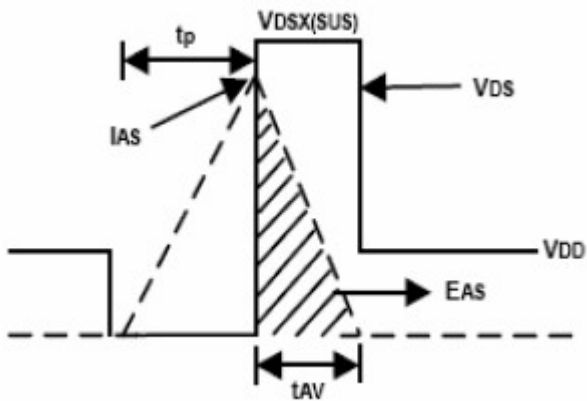
Table 3. Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100			V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25 $^{\circ}C$)	$V_{DS}=100V, V_{GS}=0V$			1	μA
I_{DSS}	Zero Gate Voltage Drain Current(Tc=100 $^{\circ}C$)	$V_{DS}=100V, V_{GS}=0V$			5	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	2.0	3.0	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=4.5A$		90	140	m Ω
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=4.5V, I_D=3A$		95	152	m Ω
Dynamic Characteristics						
g_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=4.5A$	5			S
C_{iss}	Input Capacitance	$V_{DS}=50V, V_{GS}=0V$ $f=1.0MHz$		690		PF
C_{oss}	Output Capacitance			44		PF
C_{riss}	Reverse Transfer Capacitance			30		PF
Q_g	Total Gate Charge	$V_{DS}=50V, I_D=4.5A$ $V_{GS}=10V$		13.4		nC
Q_{gs}	Gate-Source Charge			3.2		nC
Q_{gd}	Gate-Drain Charge			6.2		nC
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=50V, R_L=8.6\Omega$ $V_{GS}=10V, R_G=3\Omega$		7		nS
t_r	Turn-on Rise Time			12		nS
$t_{d(off)}$	Turn-Off Delay Time			24		nS
t_f	Turn-Off Fall Time			11		nS
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current(Body Diode)			11		A
I_{SDM}	Pulsed Source-Drain Current(Body Diode)			44		A
V_{SD}	Forward On Voltage ^(Note 1)	$T_J=25^{\circ}C, I_{SD}=1A, V_{GS}=0V$		0.75	1	V
t_{rr}	Reverse Recovery Time ^(Note 1)	$T_J=25^{\circ}C, I_F=4.5A$ $di/dt=500A/\mu s$		11		nS
Q_{rr}	Reverse Recovery Charge ^(Note 1)			14		nC
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

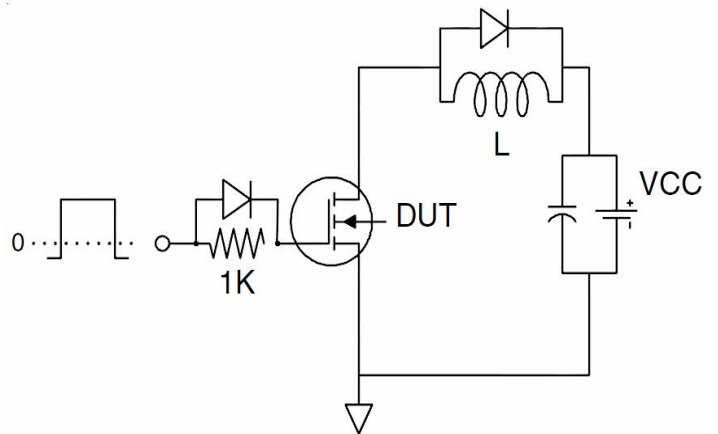
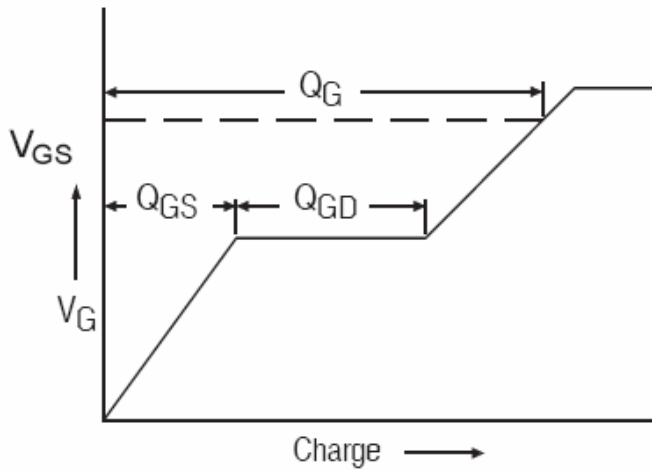
Notes 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1.5\%$, Starting $T_J=25^{\circ}C$

Test Circuit

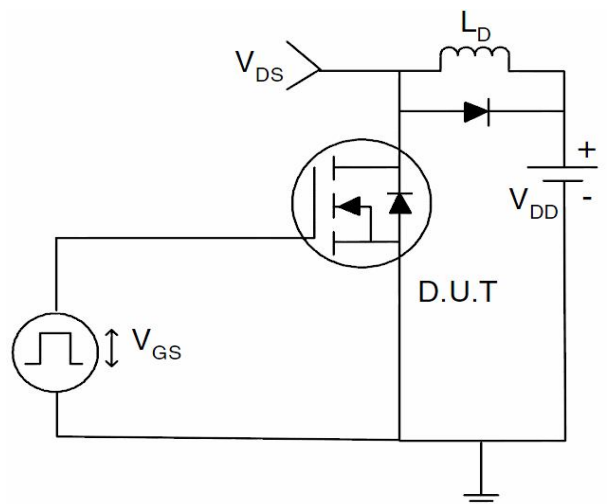
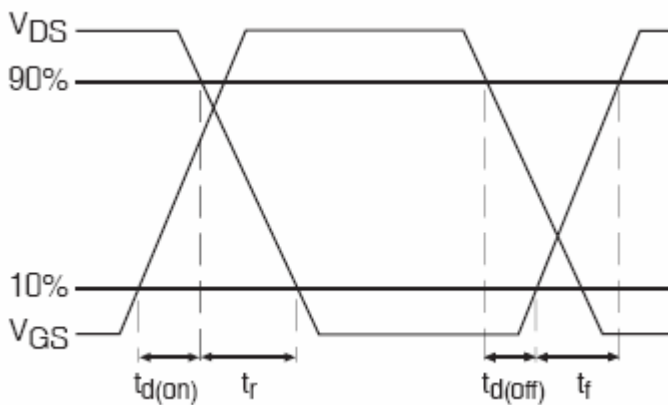
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. On-Region Characteristics

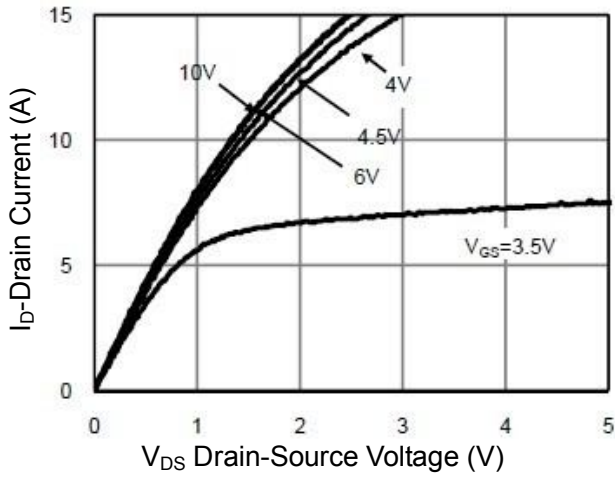


Figure 2: Transfer Characteristics

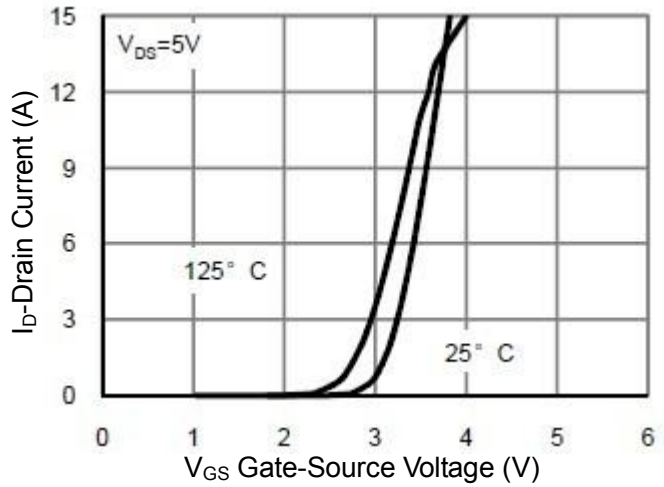


Figure3. I_D vs Junction Temperature

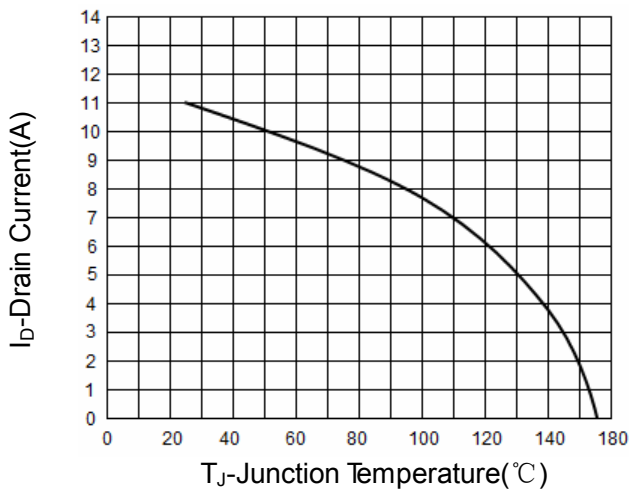


Figure4. On-Resistance vs. Junction Temperature

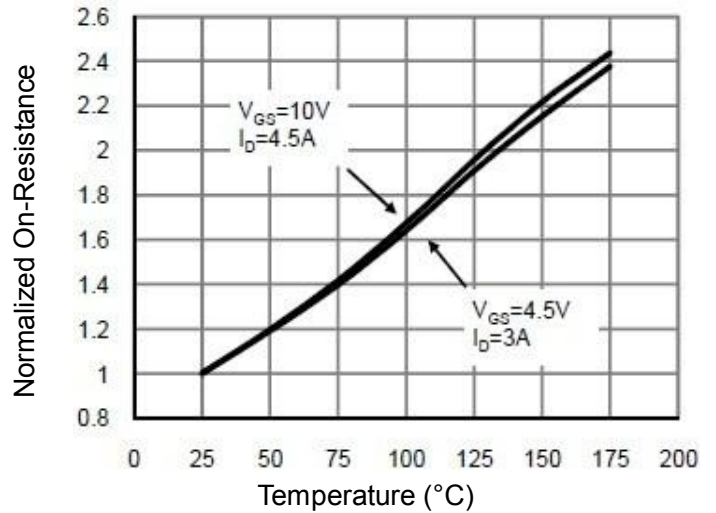


Figure5. On-Resistance vs. Gate-Source Voltage

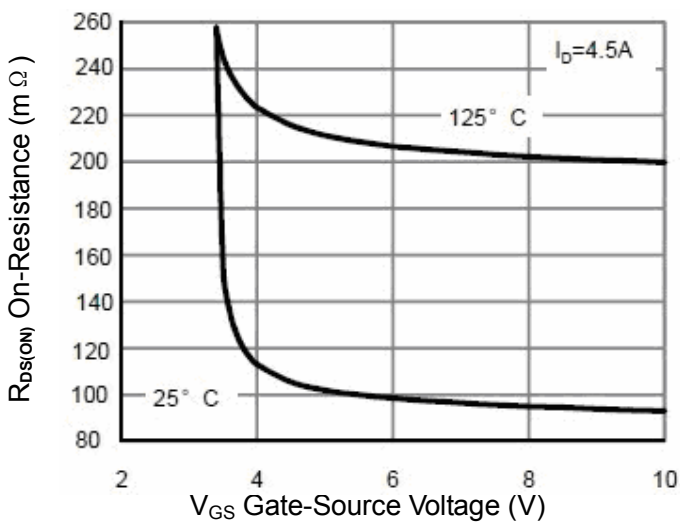


Figure6. Body-Diode Characteristics

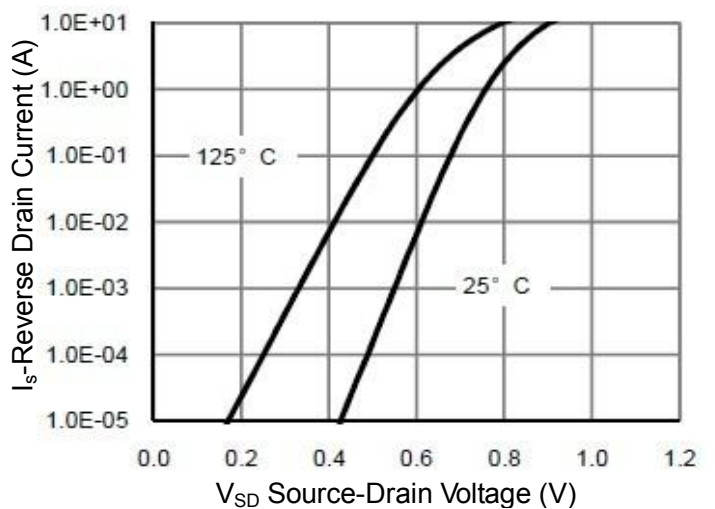


Figure 7. Gate-Charge Characteristics

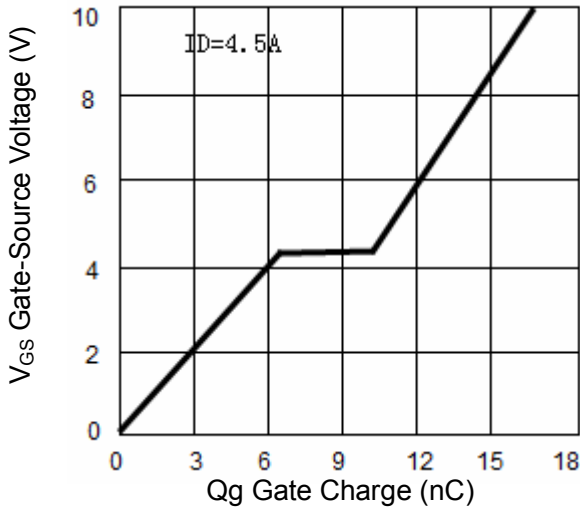


Figure 8. Capacitance Characteristics

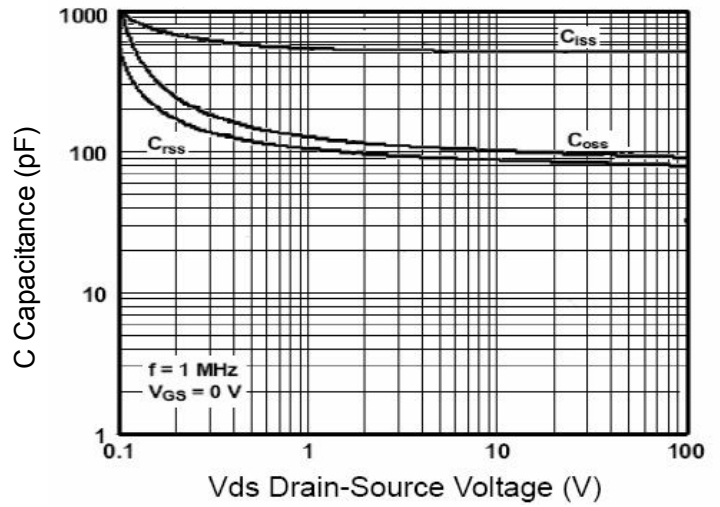


Figure 9. Maximum Forward Biased Safe Operating Area

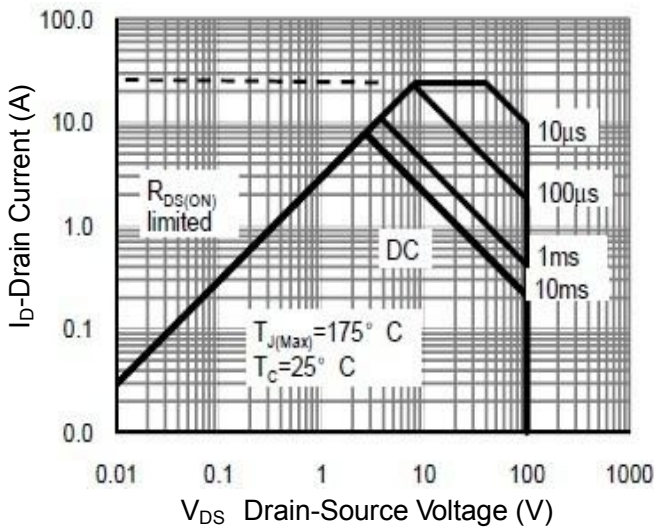


Figure 10. Single Pulse Power Rating Junction-to-Case

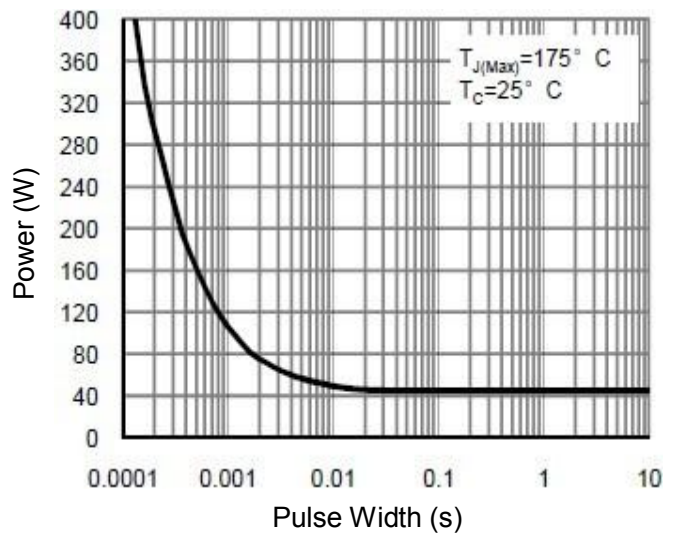
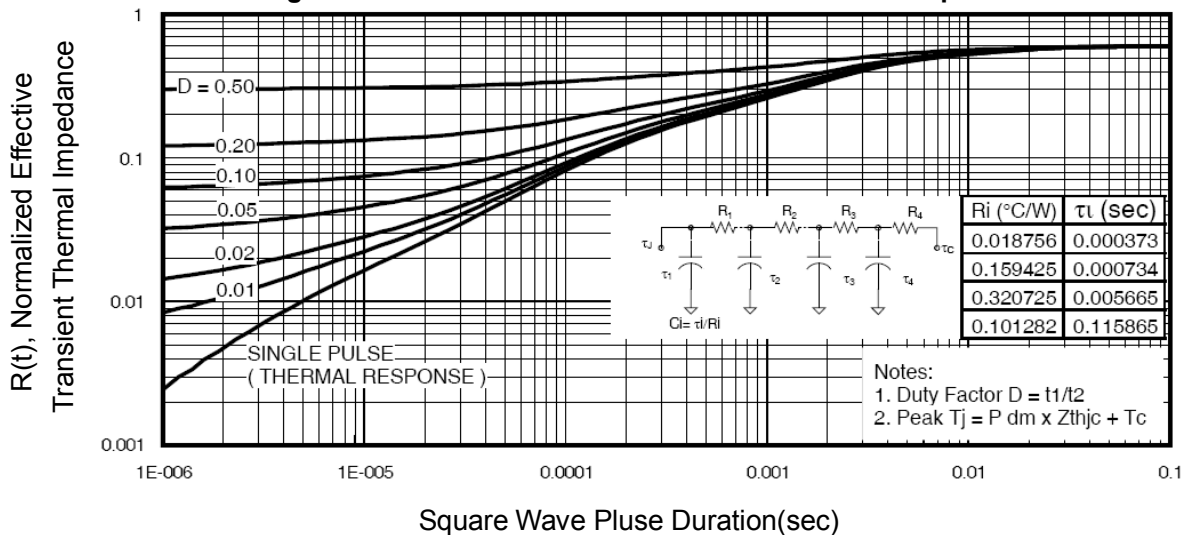
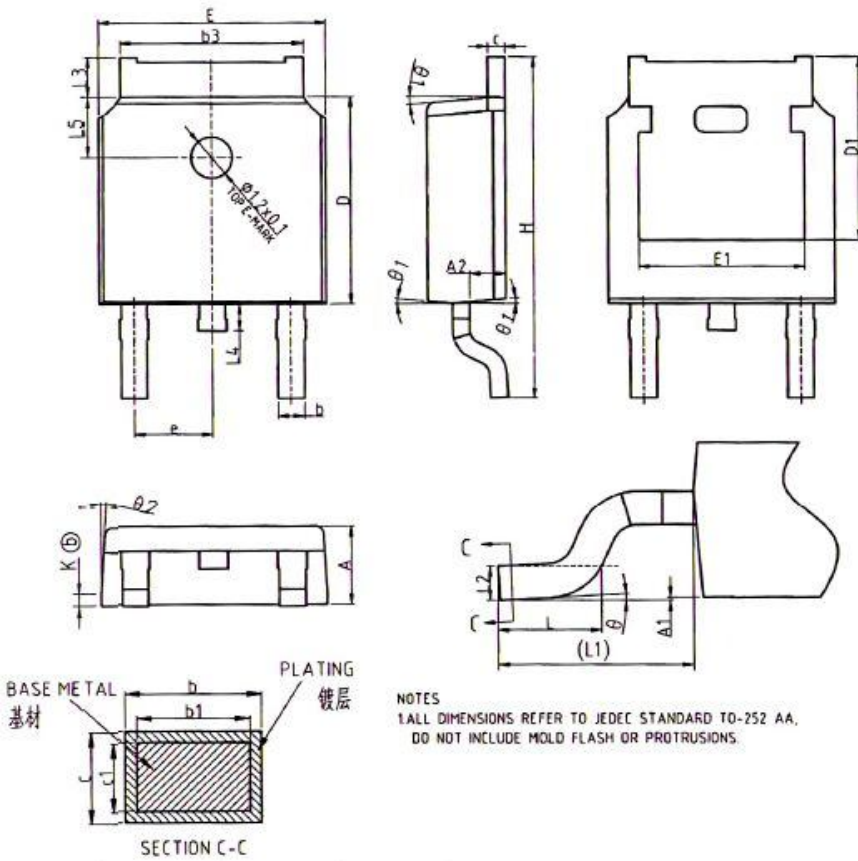


Figure 11. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



COMMON DIMENSIONS			
SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
$\theta 1$	0°	-	8°
$\theta 2$	5°	7°	9°
K	0.10REF		

NOTES
 1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AA.
 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.