

## CSD17308Q3 30-V N-Channel NexFET™ Power MOSFETs

### 1 Features

- Optimized for 5-V gate drive
- Ultra-low  $Q_g$  and  $Q_{gd}$
- Low thermal resistance
- Avalanche rated
- Lead-free terminal plating
- RoHS compliant
- Halogen free
- VSON 3.3 mm × 3.3 mm plastic package

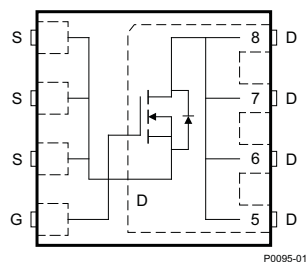
### 2 Applications

- Notebook point of load
- Point-of-load synchronous buck in networking, telecom, and computing systems

### 3 Description

This 30-V, 8.2-m $\Omega$ , 3.3 mm × 3.3 mm VSON NexFET™ power MOSFET is designed to minimize losses in power conversion applications and optimized for 5-V gate drive applications.

Top View



### Product Summary

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-source voltage	30	V
$Q_g$	Gate charge total (4.5 V)	3.9	nC
$Q_{gd}$	Gate charge gate-to-drain	0.8	nC
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 3\text{ V}$	12.5
		$V_{GS} = 4.5\text{ V}$	9.4
		$V_{GS} = 8\text{ V}$	8.2
$V_{GS(th)}$	Threshold voltage	1.3	V

### Device Information<sup>(1)</sup>

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD17308Q3	2500	13-Inch Reel	SON 3.30 mm × 3.30 mm Plastic Package	Tape and Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

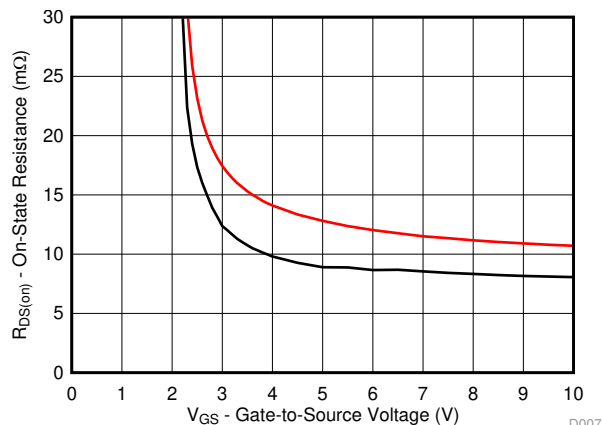
### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain-to-source voltage	30	V
$V_{GS}$	Gate-to-source voltage	+10 / -8	V
$I_D$	Continuous drain current (package limited)	50	A
	Continuous drain current, $T_C = 25^\circ\text{C}$	44	
	Continuous drain current <sup>(1)</sup>	14	
$I_{DM}$	Pulsed drain current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	167	A
$P_D$	Power dissipation <sup>(1)</sup>	2.7	W
	Power dissipation, $T_C = 25^\circ\text{C}$	28	
$T_J$ , $T_{stg}$	Operating junction and storage temperature	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche energy, single pulse $I_D = 36\text{ A}$ , $L = 0.1\text{ mH}$ , $R_G = 25\ \Omega$	65	mJ

(1) Typical  $R_{\theta JA} = 46^\circ\text{C/W}$  when mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.

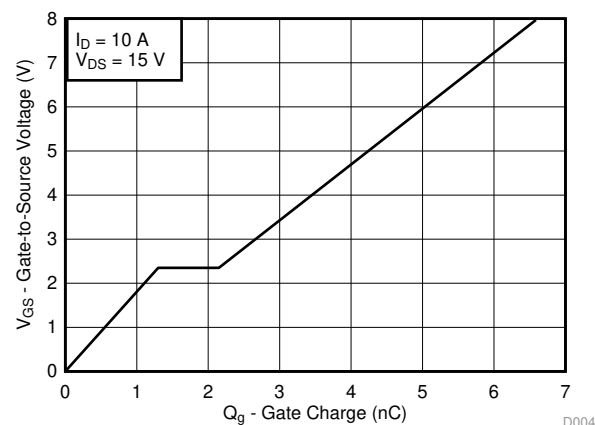
(2) Max  $R_{\theta JC} = 4.5^\circ\text{C/W}$ , pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .

$R_{DS(on)}$  vs  $V_{GS}$



D007

Gate Charge



D004



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision B (October 2015) to Revision C Page

- Changed  $V_{GS(th)}$  MAX specification in the *Electrical Characteristics* table, From 1.8 V : To 1.6 V ..... 3

### Changes from Revision A (February 2010) to Revision B Page

- Added part number to title ..... 1
- Added Package Limited Continuous Drain Current ..... 1
- Added line for Power Dissipation,  $T_C = 25^\circ\text{C}$  in *Absolute Maximum Ratings* table ..... 1
- Updated pulsed current conditions ..... 1
- Updated [Figure 1](#) to show  $R_{\theta JC}$  curves ..... 5
- Added 4.5 V curve in [Figure 8](#) ..... 6
- Updated [Figure 10](#) ..... 7
- Added the *Device and Documentation Support* section ..... 8
- Updated the [Mechanical, Packaging, and Orderable Information](#) section ..... 9

### Changes from Original (February 2010) to Revision A Page

- Deleted the Package Marking Information section ..... 11

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = +10 / -8\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.9	1.3	1.6	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 3\text{ V}, I_D = 10\text{ A}$		12.5	16.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		9.4	11.8	
		$V_{GS} = 8\text{ V}, I_D = 10\text{ A}$		8.2	10.3	
$g_{fs}$	Transconductance	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		37		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{ISS}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		540	700	pF
$C_{OSS}$	Output capacitance			280	365	pF
$C_{RSS}$	Reverse transfer capacitance			27	35	pF
$R_g$	Series gate resistance			0.9	1.8	$\Omega$
$Q_g$	Gate charge total (4.5 V)	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		3.9	5.1	nC
$Q_{gd}$	Gate charge gate-to-drain			0.8		nC
$Q_{gs}$	Gate charge gate-to-source			1.3		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			0.7		nC
$Q_{OSS}$	Output charge		$V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}$		7.4	
$t_{d(on)}$	Turnon delay time	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}, R_G = 2\ \Omega$		4.5		ns
$t_r$	Rise time			5.7		ns
$t_{d(off)}$	Turnoff delay time			9.9		ns
$t_f$	Fall time			2.3		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{DS} = 10\text{ A}, V_{GS} = 0\text{ V}$		0.85	1	V
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 13\text{ V}, I_F = 10\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		9.3		nC
$t_{rr}$	Reverse recovery time			14.3		ns

### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  unless otherwise stated

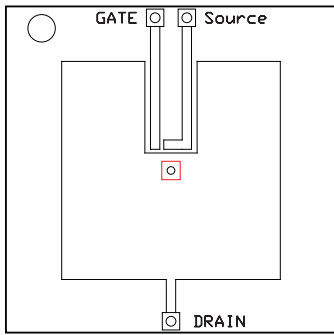
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance <sup>(1)</sup>			4.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>			58	$^\circ\text{C}/\text{W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

### CSD17308Q3

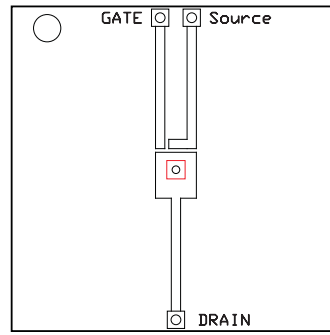
SLPS262C – FEBRUARY 2010 – REVISED DECEMBER 2019

[www.ti.com](http://www.ti.com)



M0161-01

Max  $R_{\theta JA} = 58^{\circ}\text{C/W}$   
 when mounted on 1 in<sup>2</sup>  
 (6.45 cm<sup>2</sup>) of  
 2-oz (0.071-mm) thick  
 Cu.



M0161-02

Max  $R_{\theta JA} = 165^{\circ}\text{C/W}$   
 when mounted on a  
 minimum pad area of  
 2-oz (0.071-mm) thick  
 Cu.

### 5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise stated

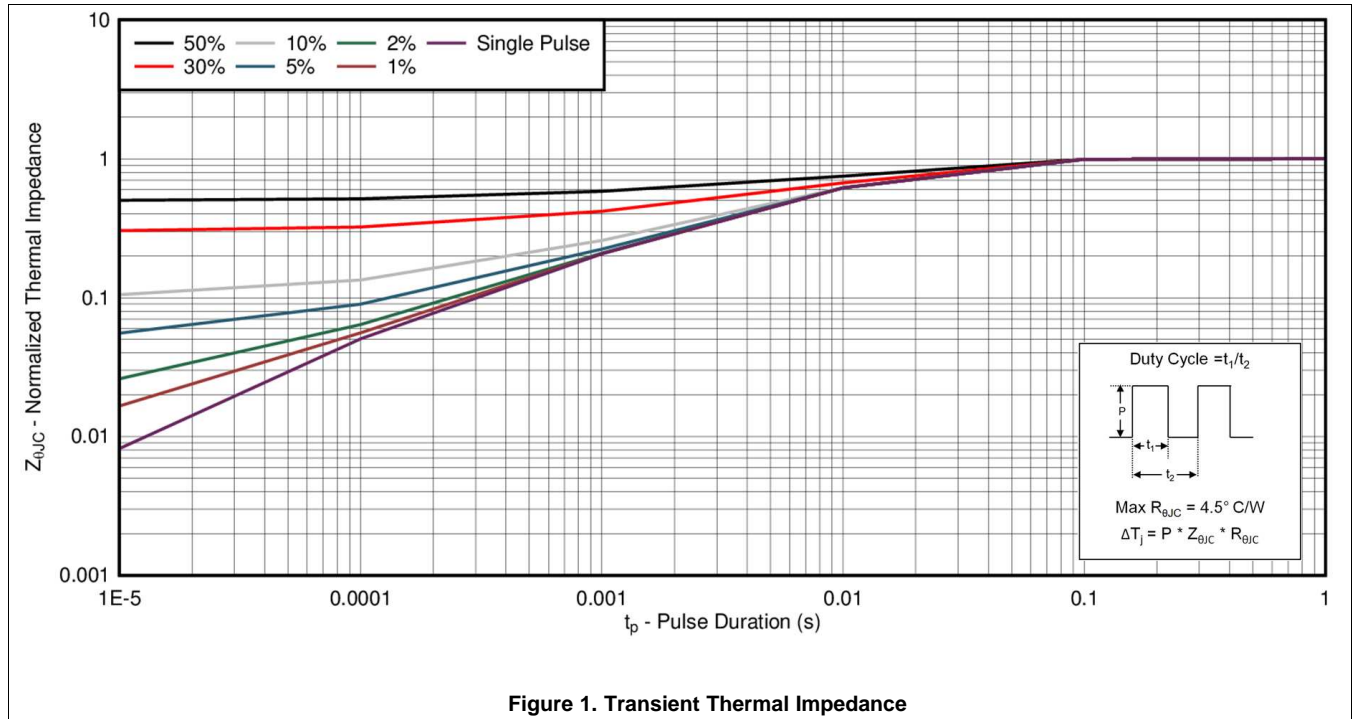


Figure 1. Transient Thermal Impedance

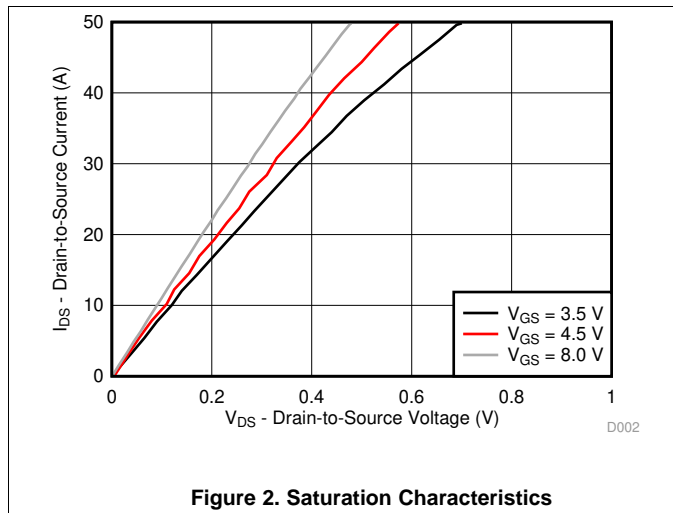


Figure 2. Saturation Characteristics

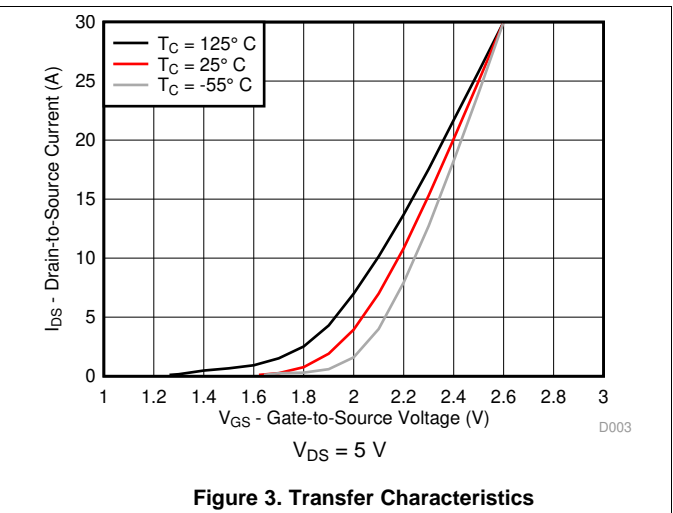
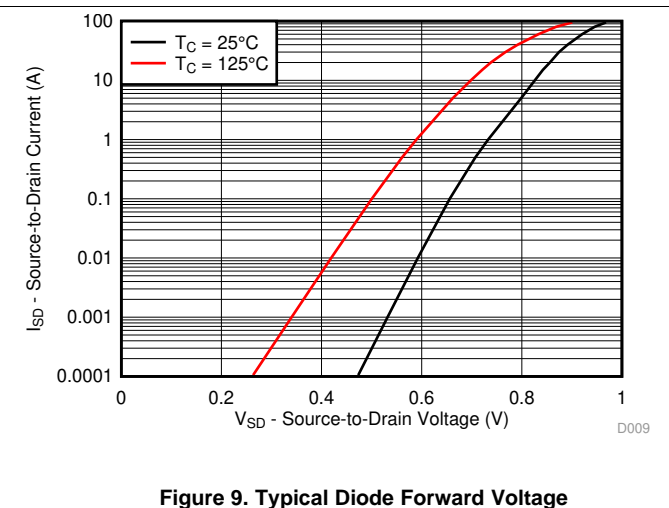
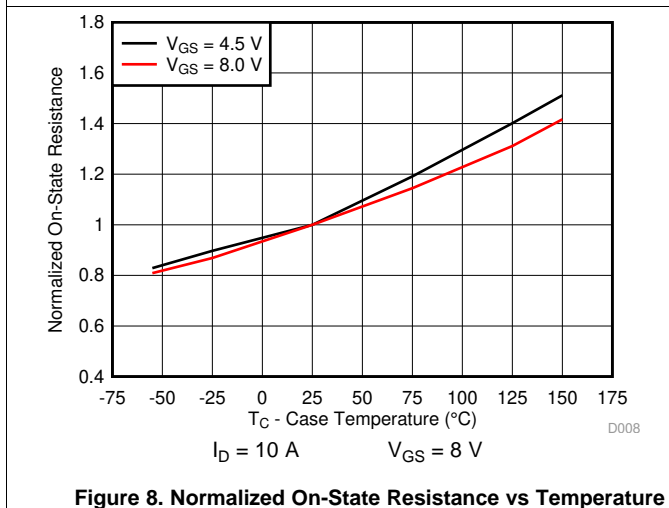
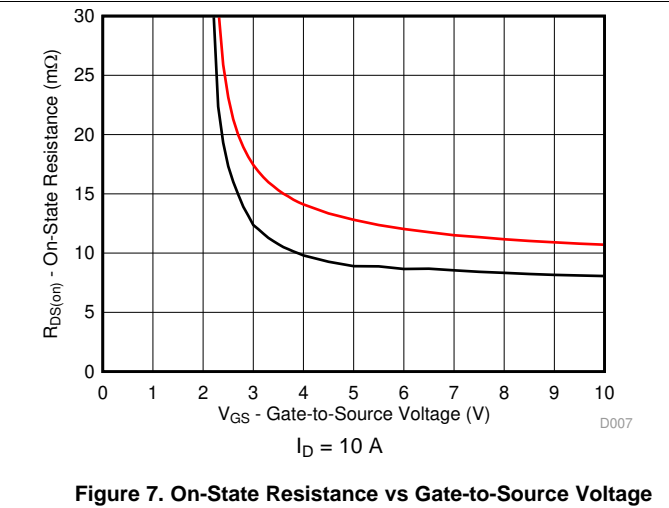
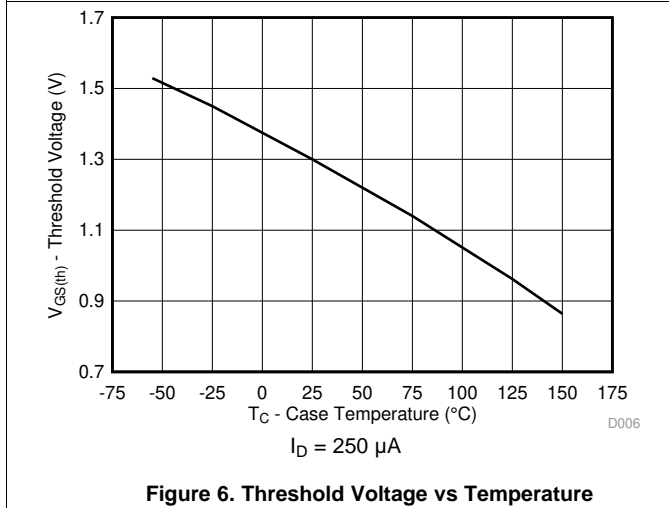
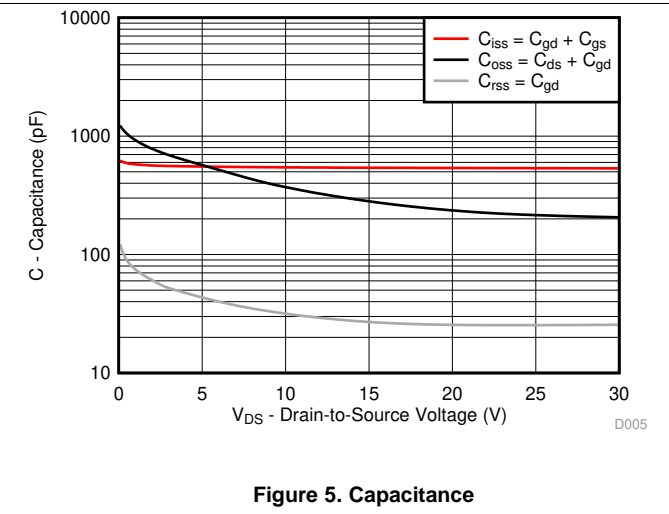
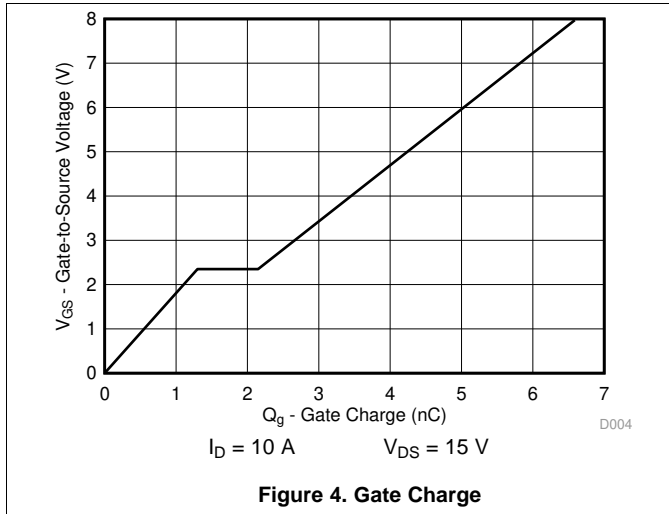


Figure 3. Transfer Characteristics

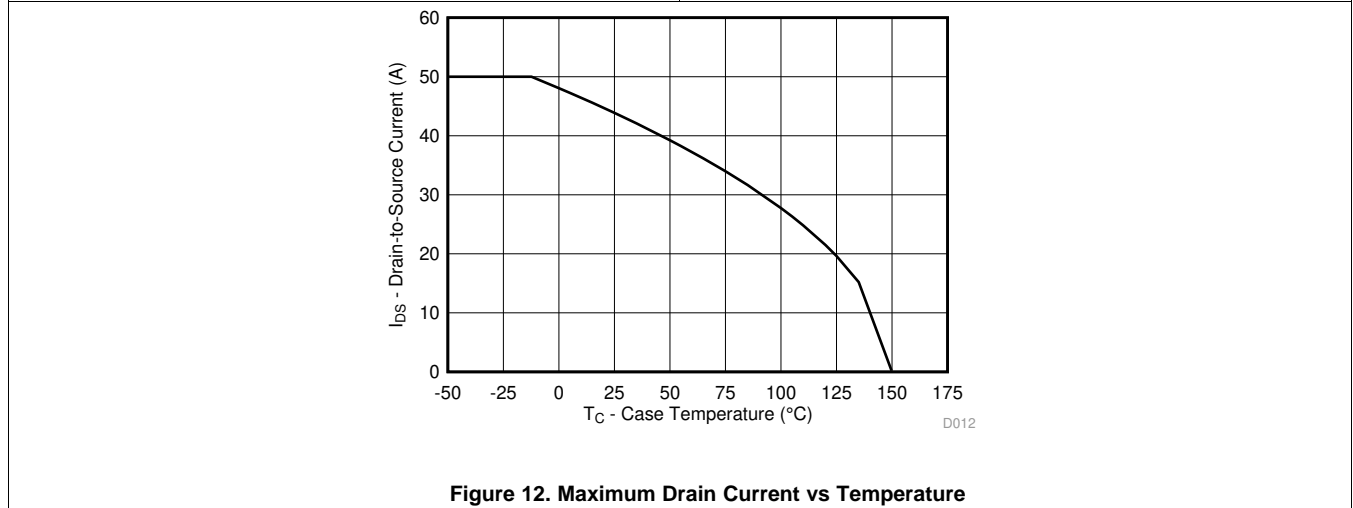
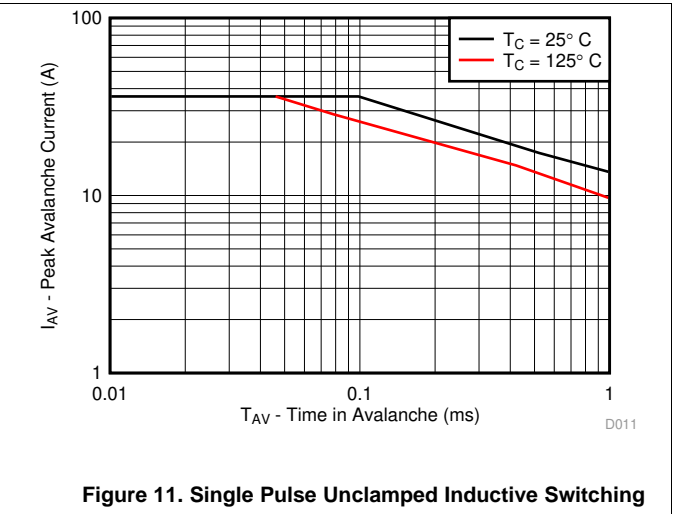
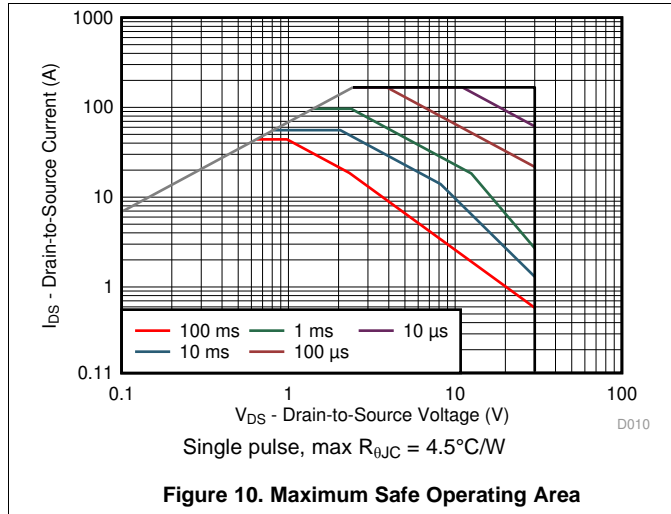
Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C unless otherwise stated



**Typical MOSFET Characteristics (continued)**

$T_A = 25^\circ\text{C}$  unless otherwise stated



## 6 Device and Documentation Support

### 6.1 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.4 Glossary

[SLYZ022](#) — *TI Glossary*.

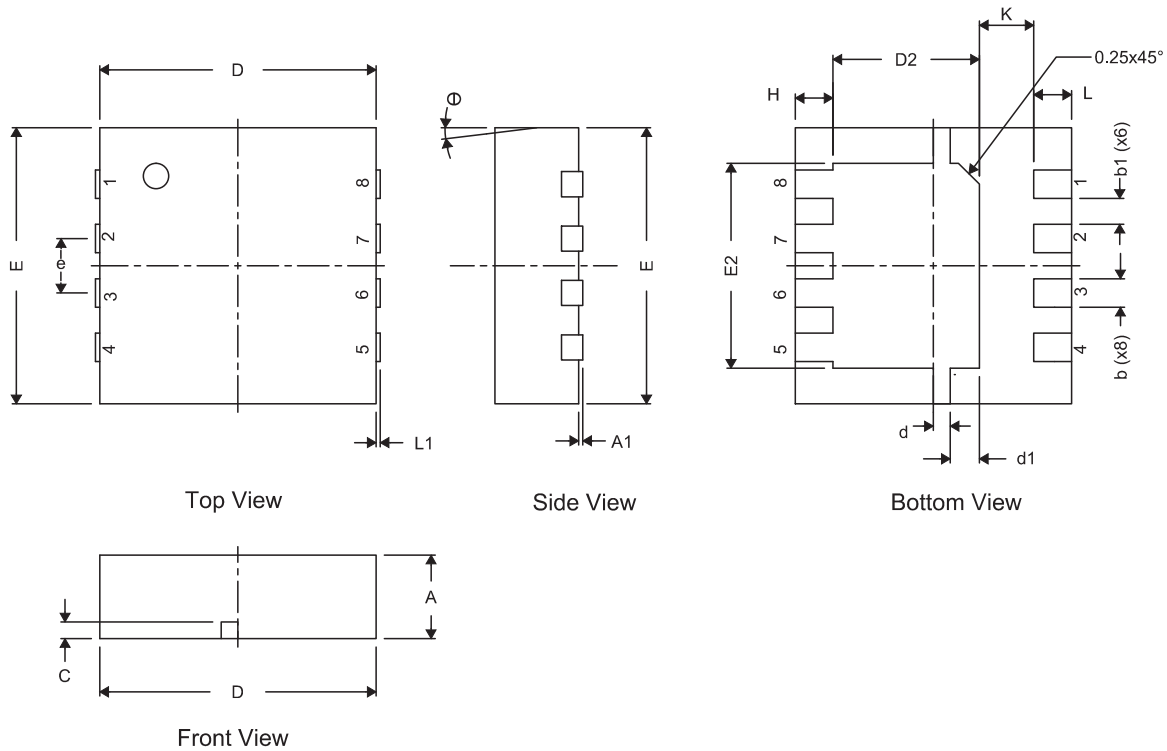
This glossary lists and explains terms, acronyms, and definitions.



## 7 Mechanical, Packaging, and Orderable Information

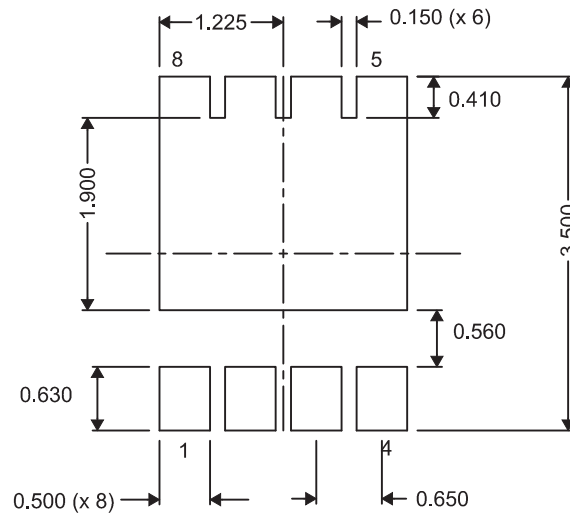
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Q3 Package Dimensions



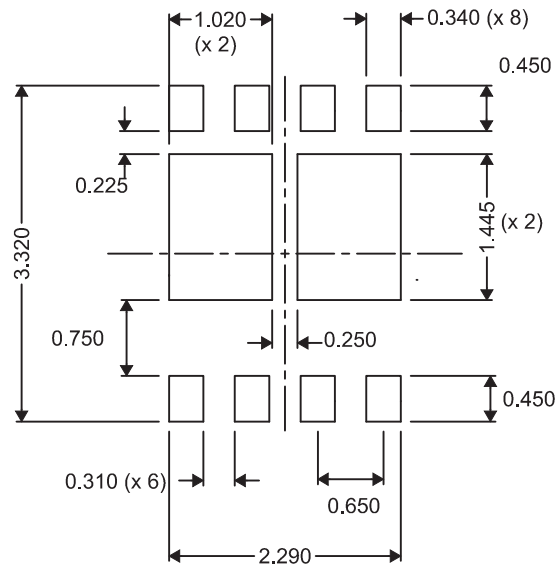
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026 TYP		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
$\theta$	0	—	0	0	—	0

## 7.2 Recommended PCB Pattern



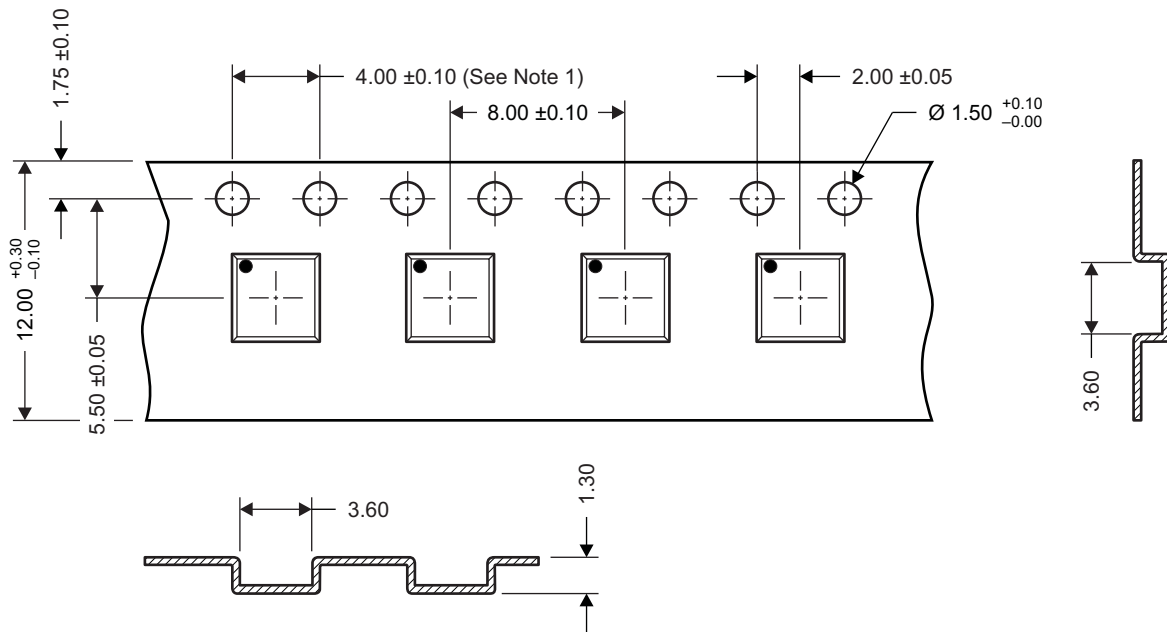
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

## 7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

## 7.4 Q3 Tape and Reel Information



M0144-01

### Notes:

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness:  $0.30 \pm 0.05$  mm
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17308Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Pb-Free (RoHS Exempt)	SN	Level-1-260C-UNLIM	-55 to 150	CSD17308	<a href="#">Samples</a>
CSD17308Q3T	ACTIVE	VSON-CLIP	DQG	8	250	Pb-Free (RoHS Exempt)	SN	Level-1-260C-UNLIM	-55 to 150	CSD17308	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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