CSD17382F4 30-V N-Channel FemtoFET™ MOSFET

1 Features

- Low On-Resistance
- Low Q_g and Q_{gd}
- Low Threshold Voltage
- Ultra-Small Footprint (0402 Case Size)
  - 1.0 mm × 0.6 mm
- Ultra-Low Profile
  - 0.35-mm Height
- Integrated ESD Protection Diode
  - Rated > 3-kV HBM
  - Rated > 2-kV CDM
- Lead and Halogen Free
- RoHS Compliant

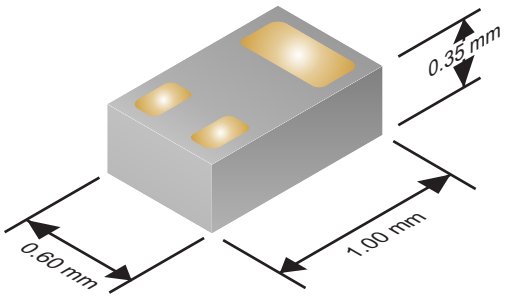
2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Single-Cell Battery Applications
- Handheld and Mobile Applications

3 Description

This 30-V, 54-mΩ, N-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

Typical Part Dimensions



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	2.1		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.63		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 1.8 V	110	mΩ
		V_{GS} = 2.5 V	67	mΩ
		V_{GS} = 4.5 V	56	mΩ
		V_{GS} = 8.0 V	54	mΩ
$V_{GS(th)}$	Threshold Voltage	0.9		V

Ordering Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD17382F4	3000	7-Inch Reel	Femto (0402) 1.0-mm × 0.6-mm SMD Lead Less	Tape and Reel
CSD17382F4T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

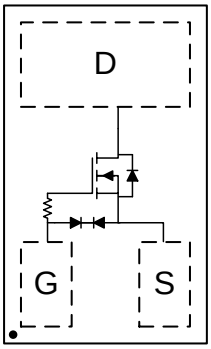
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	10	V
I_D	Continuous Drain Current(1)	2.3	A
I_{DM}	Pulsed Drain Current(2)	14.8	A
P_D	Power Dissipation(1)	500	mW
ESD Rating	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	2000	V
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 6.5 A, L = 0.1 mH, R_G = 25 Ω	2.1	mJ

(1) Typical $R_{\theta JA}$ = 245°C/W on 1-in^2 (6.45-cm^2), 2-oz. (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤100 µs, duty cycle ≤1%.

Top View



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4 Revision History

Changes from Original (April 2016) to Revision A **Page**

- Changed the TEST CONDITIONS for g_{fs} Transconductance From: V_{DS} = 15 V To: V_{DS} = 3 V in the Electrical Characteristics section. ... 3
- Added Receiving Notification of Documentation Updates in the Device and Documentation Support section. ... 7
- Updated all mechanical drawings. ... 8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 10 V			5	µA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	0.7	0.9	1.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 1.8 V, I_{DS} =0.5 A		110	180	mΩ
		V_{GS} = 2.5 V, I_{DS} =0.5 A		67	82	mΩ
		V_{GS} = 4.5 V, I_{DS} = 0.5 A		56	67	mΩ
		V_{GS} = 8.0 V, I_{DS} = 0.5 A		54	64	mΩ
g_{fs}	Transconductance	V_{DS} = 3 V, I_{DS} = 0.5 A		5.9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		267	347	pF
C_{oss}	Output capacitance			31.0	40.3	pF
C_{rss}	Reverse transfer capacitance			15.0	19.5	pF
R_G	Series gate resistance			220		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_{DS} = 0.5 A		2.1	2.7	nC
Q_{gd}	Gate charge gate-to-drain			0.63		nC
Q_{gs}	Gate charge gate-to-source			0.41		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.12		nC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		1.53		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 0.5 A, R_G = 0 Ω		59		ns
t_r	Rise time			111		ns
$t_{d(off)}$	Turn off delay time			279		ns
t_f	Fall time			270		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 0.5 A, V_{GS} = 0 V		0.7	1.0	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	85	°C/W
	Junction-to-ambient thermal resistance(2)	245	°C/W

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz. (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

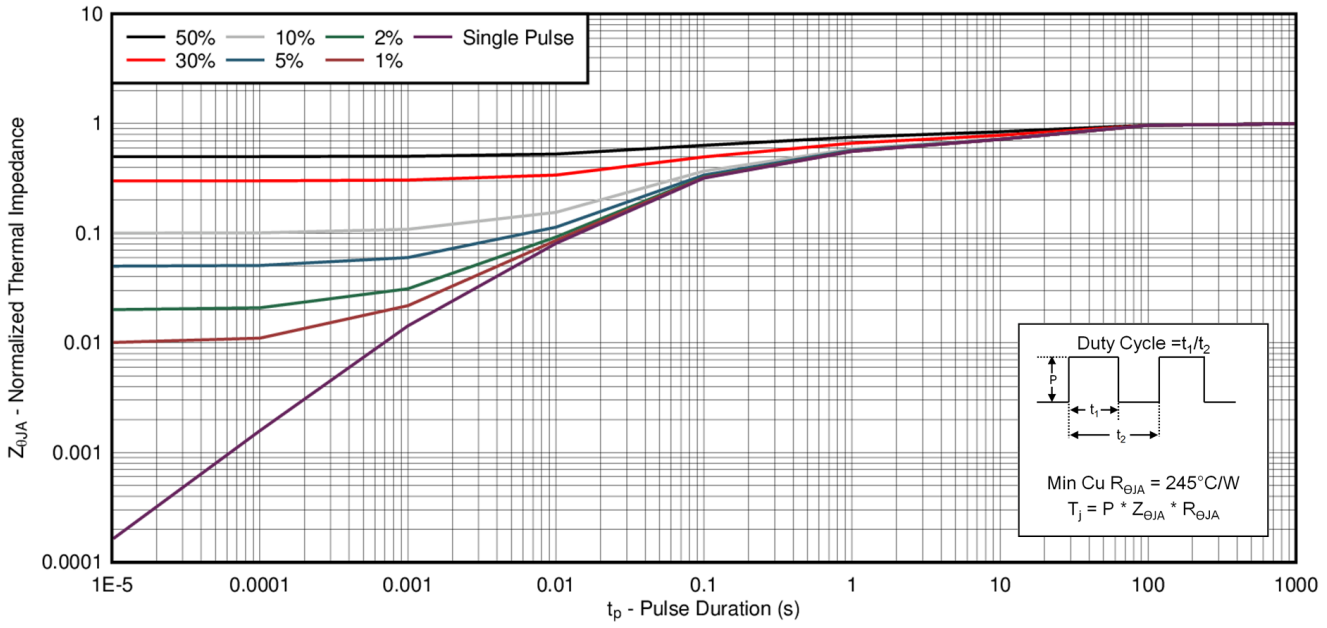

Figure 1. Transient Thermal Impedance

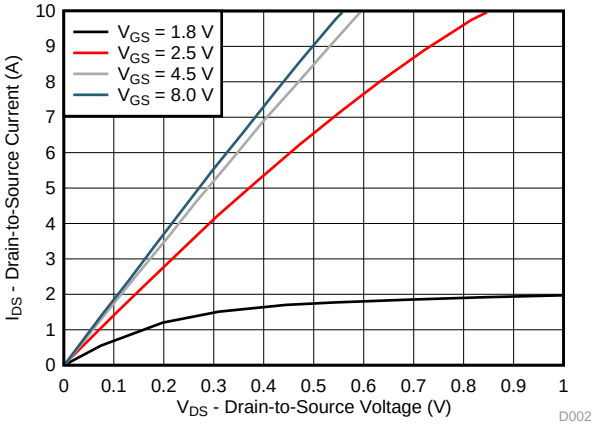

Figure 2. Saturation Characteristics

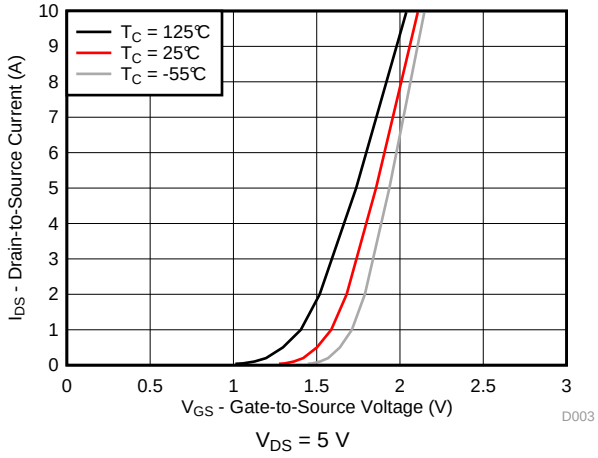

Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

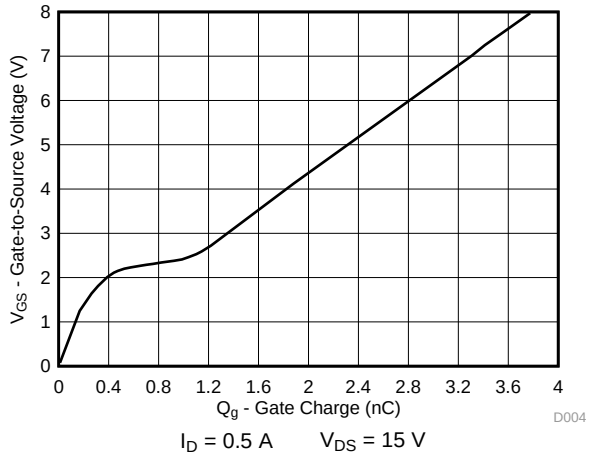

Figure 4. Gate Charge

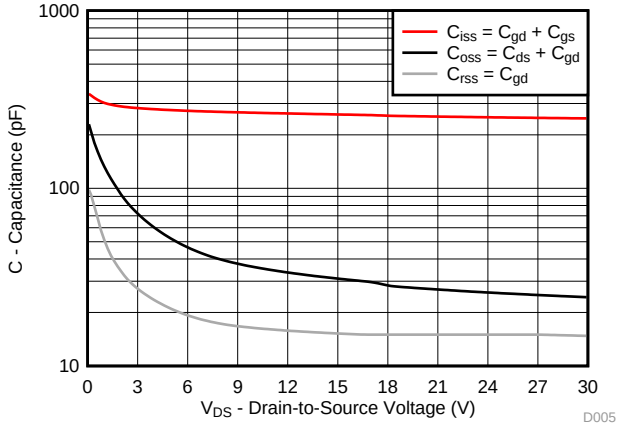

Figure 5. Capacitance

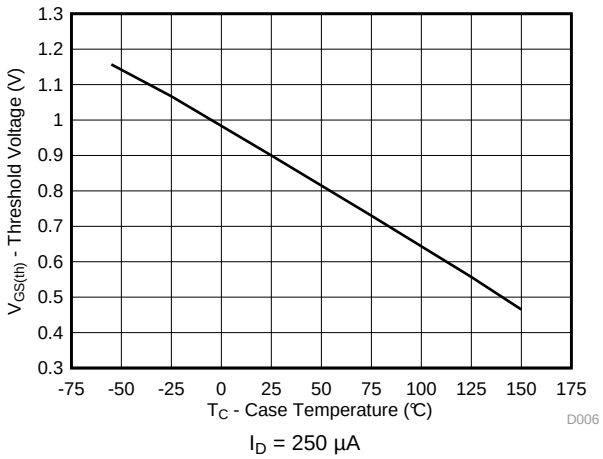

Figure 6. Threshold Voltage vs Temperature

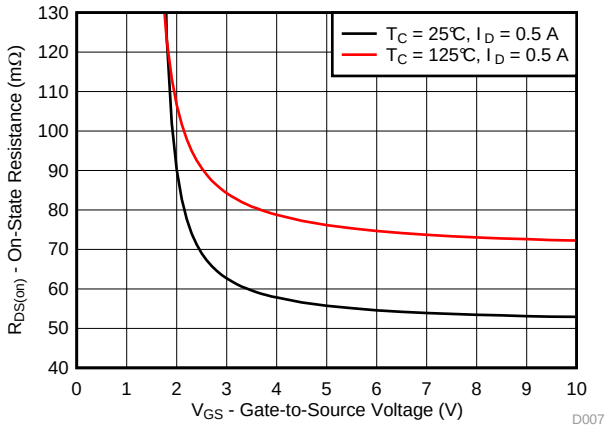

Figure 7. On-State Resistance vs Gate-to-Source Voltage

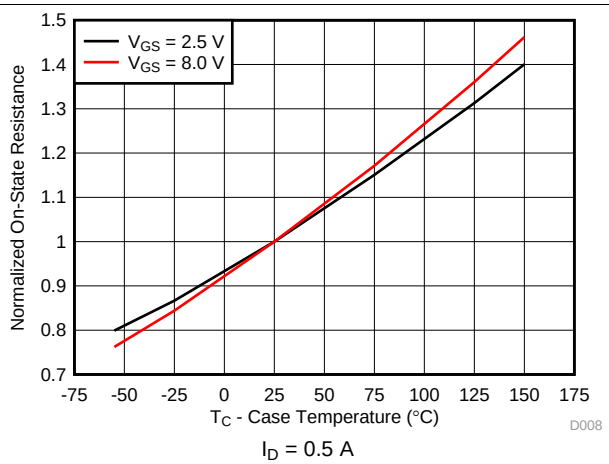

Figure 8. Normalized On-State Resistance vs Temperature

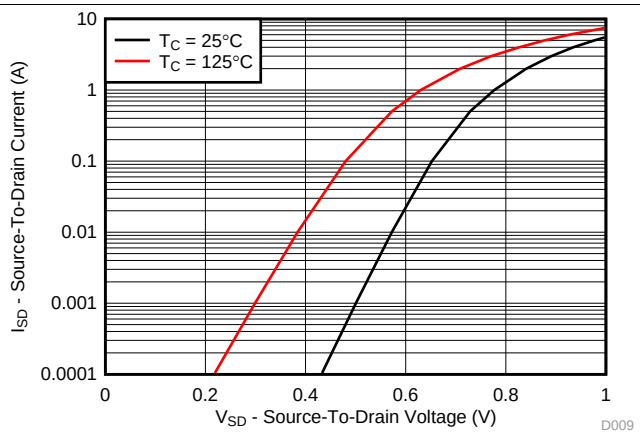

Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

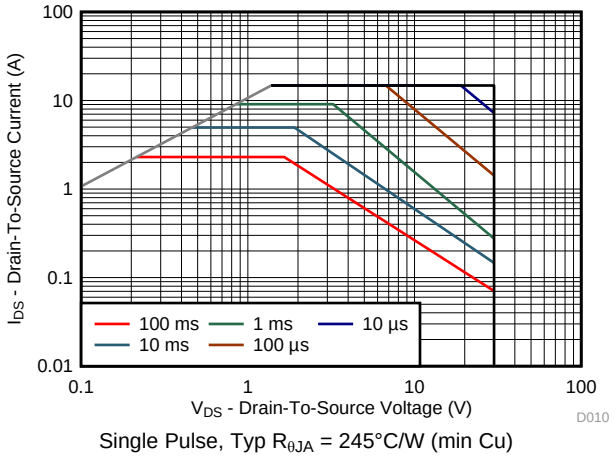

Figure 10. Maximum Safe Operating Area (SOA)

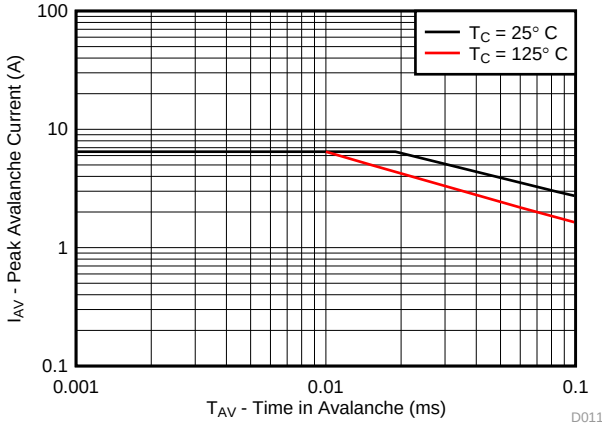

Figure 11. Single Pulse Unclamped Inductive Switching

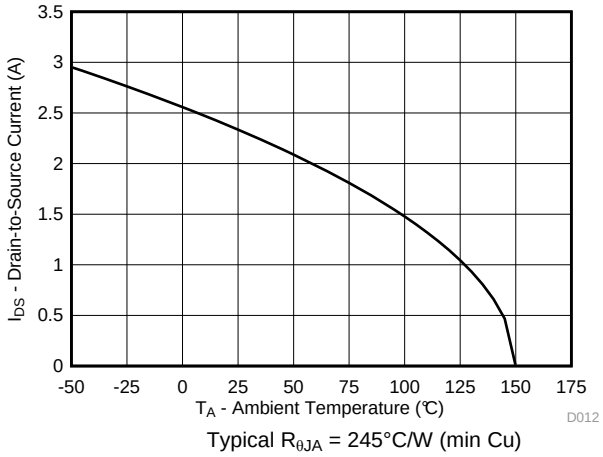

Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

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All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

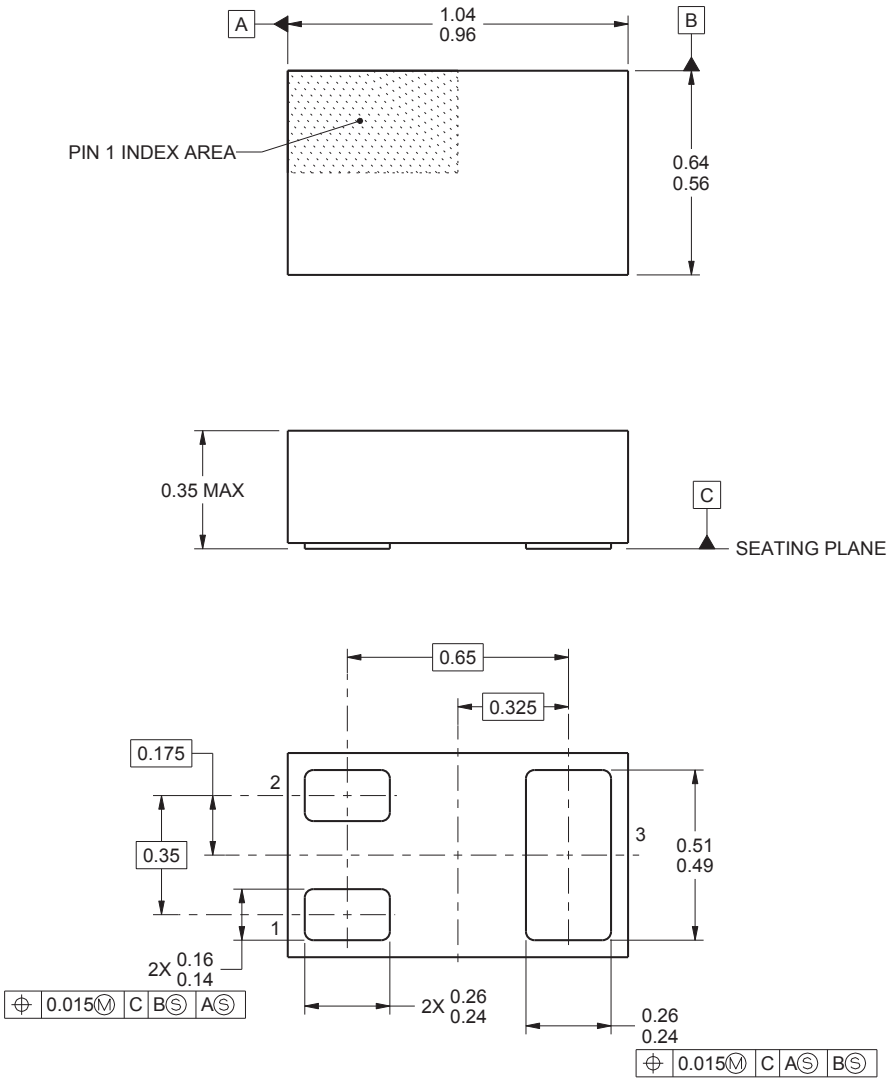
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

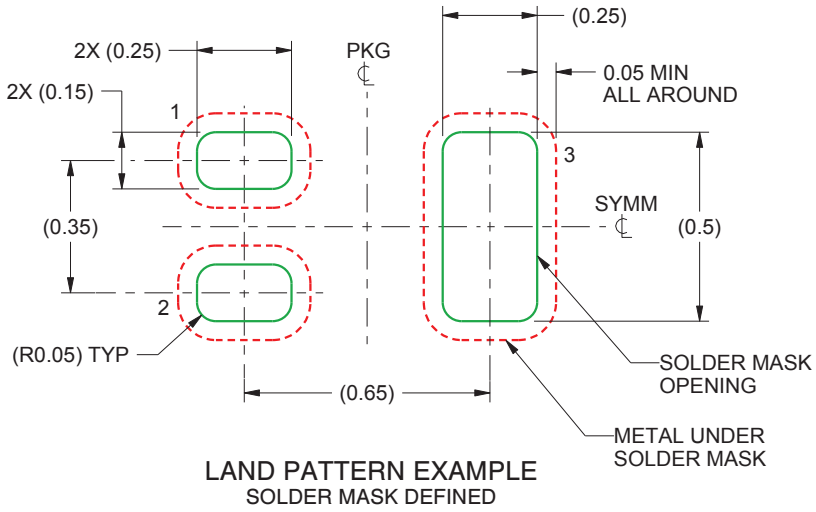


(1) All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

(2) This drawing is subject to change without notice.

(3) This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

7.2 Recommended Minimum PCB Layout

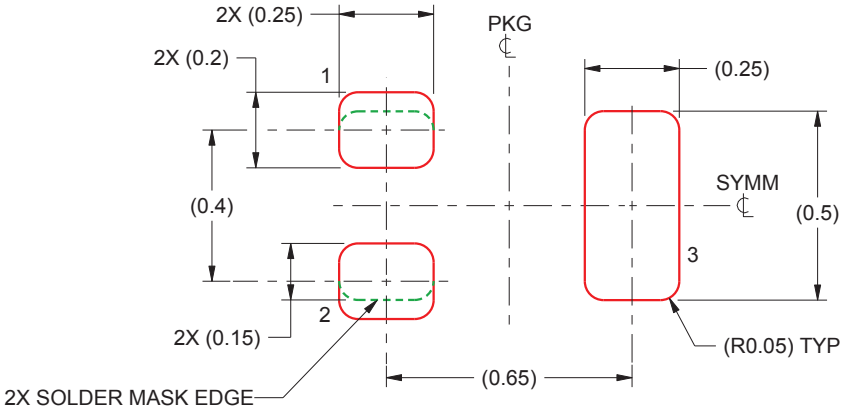


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED

(1) All dimensions are in millimeters.

(2) For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

7.3 Recommended Stencil Pattern

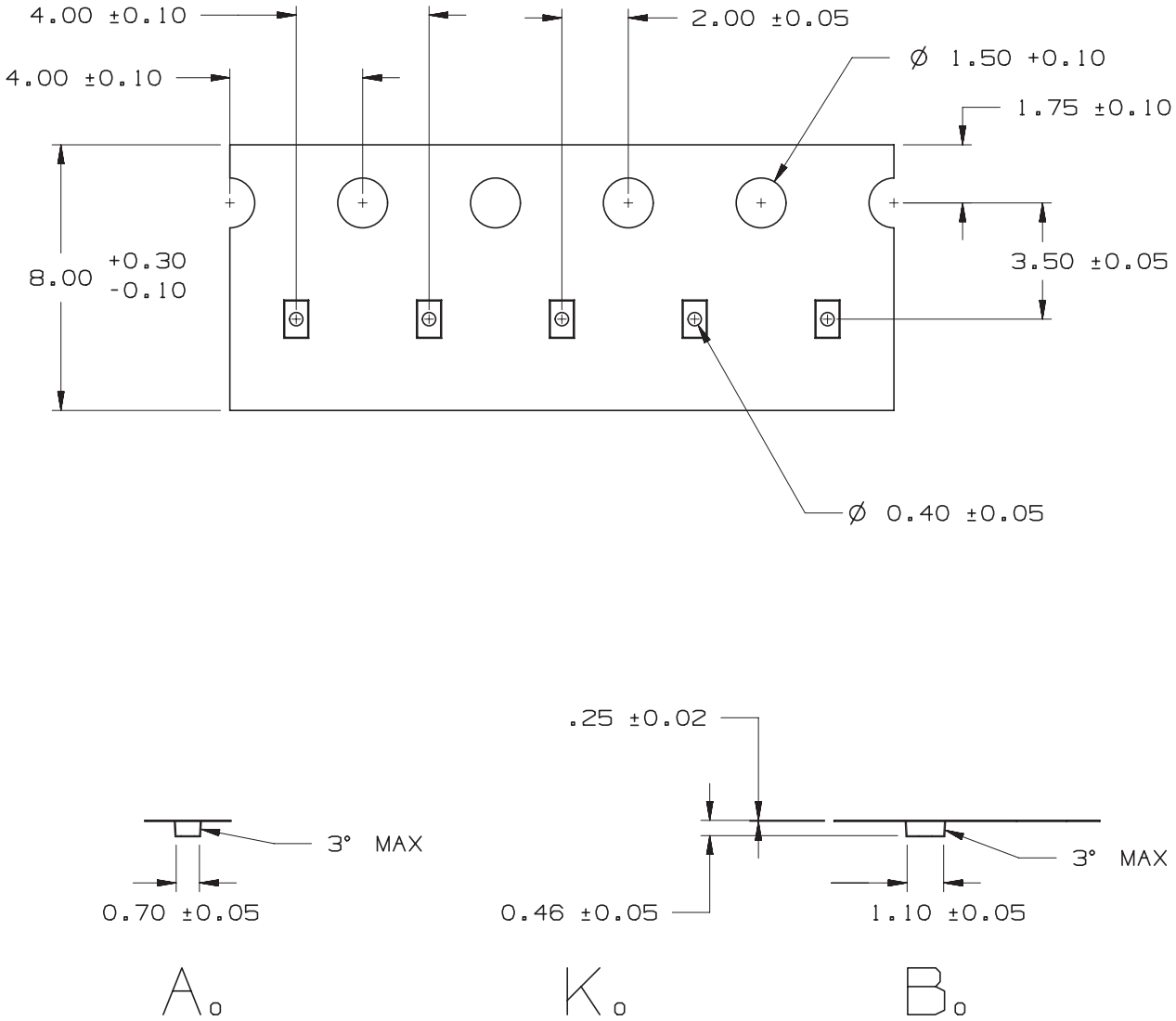


SOLDER PASTE EXAMPLE

(1) All dimensions are in millimeters.

(2) Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7.4 CSD17382F4 Embossed Carrier Tape Dimensions



(1) Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17382F4	ACTIVE	PICOSTAR	YJC	3	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-55 to 150	HM	Samples
CSD17382F4T	ACTIVE	PICOSTAR	YJC	3	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-55 to 150	HM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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