CSD19533KCS, 100 V N-Channel NexFET™ Power MOSFET

1 Features

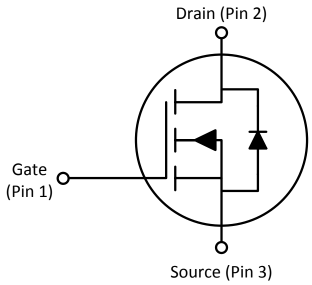
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 100 V, 8.7 mΩ, TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	100		V
Q_g	Gate Charge Total (10 V)	27		nC
Q_{gd}	Gate Charge Gate-to-Drain	5.4		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 6 V	9.7	mΩ
		V_{GS} = 10 V	8.7	mΩ
$V_{GS(th)}$	Threshold Voltage	2.8		V

Ordering Information[(1)]

Device	Package	Media	Qty	Ship
CSD19533KCS	TO-220 Plastic Package	Tube	50	Tube

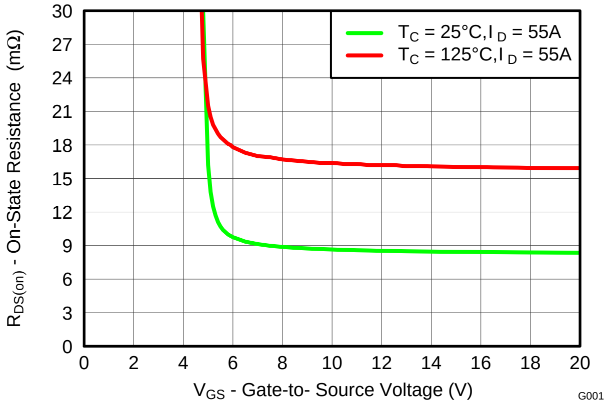
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

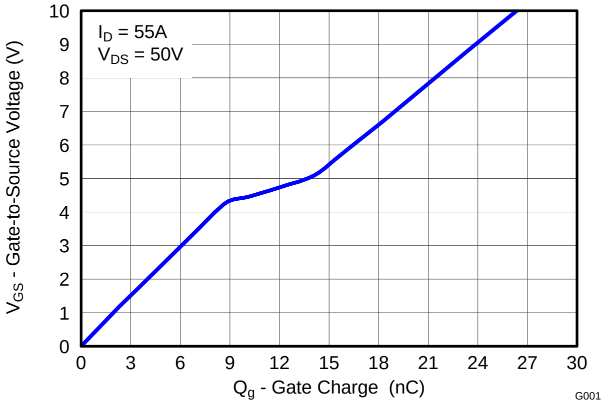
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	86	
	Continuous Drain Current (Silicon limited), T_C = 100°C	61	
I_{DM}	Pulsed Drain Current [(1)]	207	A
P_D	Power Dissipation	188	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 175	°C
E_{AS}	Avalanche Energy, single pulse I_D = 46 A, L = 0.1 mH, R_G = 25 Ω	106	mJ

(1) Max $R_{\theta JC}$ = 0.8°C/W, pulse duration ≤100 μs, Duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge



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4 Revision History

Changes from Revision A (July 2014) to Revision B	Page
• Changed Q_{rr} to 211 nC	3

Changes from Original (December 2013) to Revision A	Page
• Pulsed drain current increased from 104 to 207 A	1
• Updated pulsed current conditions	1
• Updated Figure 10 to reflect increased pulsed drain current	6

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 μA	100			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 80 V			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.2	2.8	3.4	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 6 V, I_D = 55 A		9.7	12.2	mΩ
		V_{GS} = 10 V, I_D = 55 A		8.7	10.5	mΩ
$g_{ƒs}$	Transconductance	V_{DS} = 10 V, I_D = 55 A		115		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 50 V, ƒ = 1 MHz		2050	2670	pF
C_{oss}	Output Capacitance			395	514	pF
C_{rss}	Reverse Transfer Capacitance			9.6	12.5	pF
R_G	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (10 V)	V_{DS} = 50 V, I_D = 55 A		27	35	nC
Q_{gd}	Gate Charge Gate-to-Drain			5.4		nC
Q_{gs}	Gate Charge Gate-to-Source			9		nC
$Q_{g(th)}$	Gate Charge at V_{th}			3.9		nC
Q_{oss}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		79		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 50 V, V_{GS} = 10 V, I_{DS} = 55 A, R_G = 0 Ω		7		ns
t_r	Rise Time			5		ns
$t_{d(off)}$	Turn Off Delay Time			12		ns
t_f	Fall Time			2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 55 A, V_{GS} = 0 V		0.9	1.1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 50 V, I_F = 55 A, di/dt = 300 A/μs		211		nC
t_{rr}	Reverse Recovery Time			77		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{θJC}$	Junction-to-Case Thermal Resistance			0.8	°C/W
$R_{θJA}$	Junction-to-Ambient Thermal Resistance			62	

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

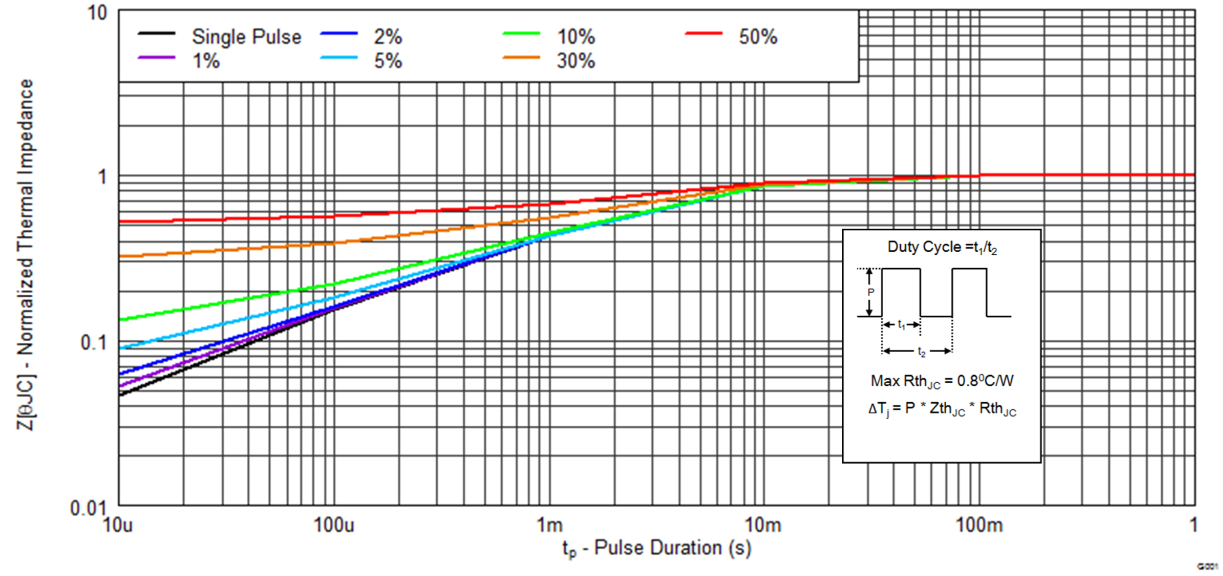


Figure 1. Transient Thermal Impedance

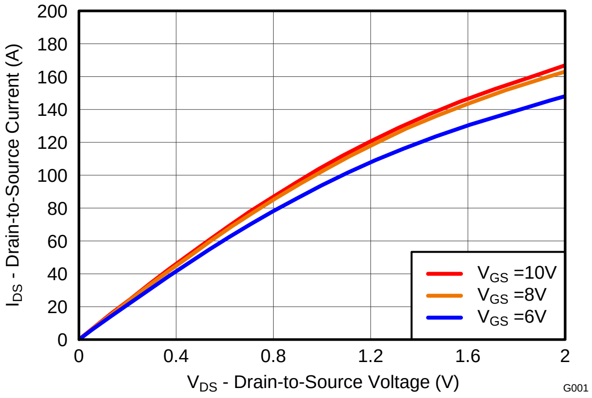


Figure 2. Saturation Characteristics

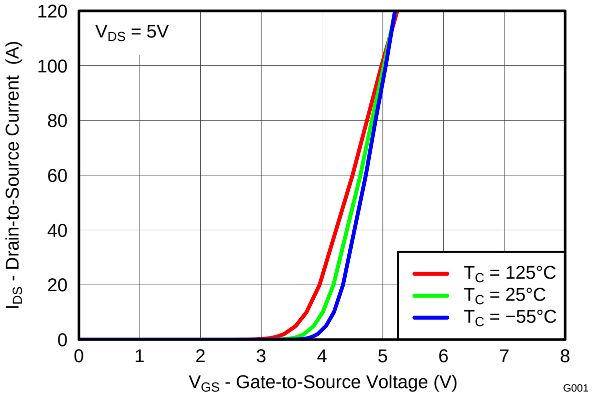


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

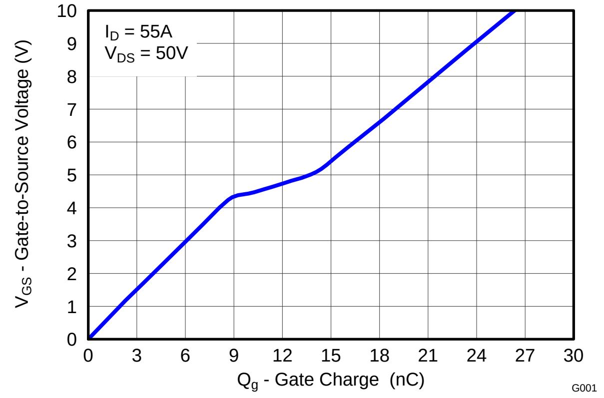


Figure 4. Gate Charge

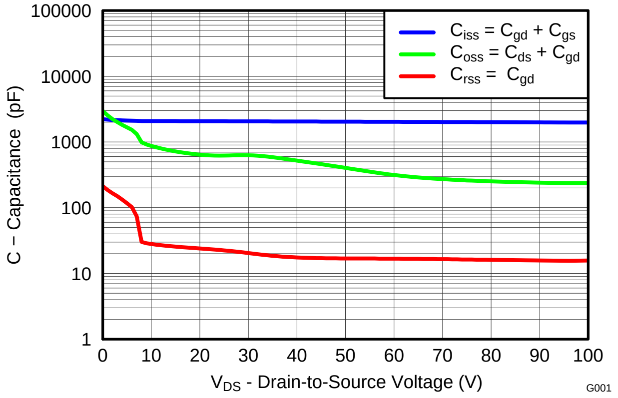


Figure 5. Capacitance

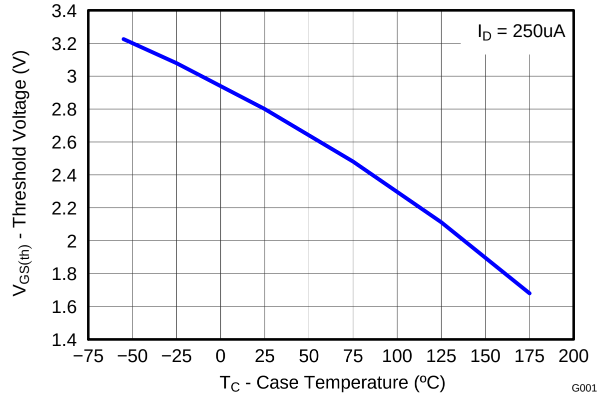


Figure 6. Threshold Voltage vs Temperature

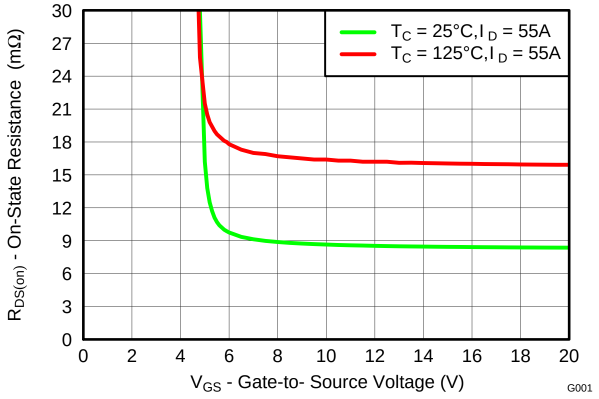


Figure 7. On-State Resistance vs Gate-to-Source Voltage

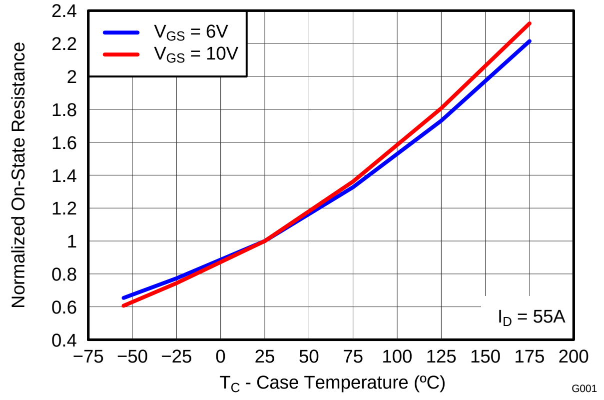


Figure 8. Normalized On-State Resistance vs Temperature

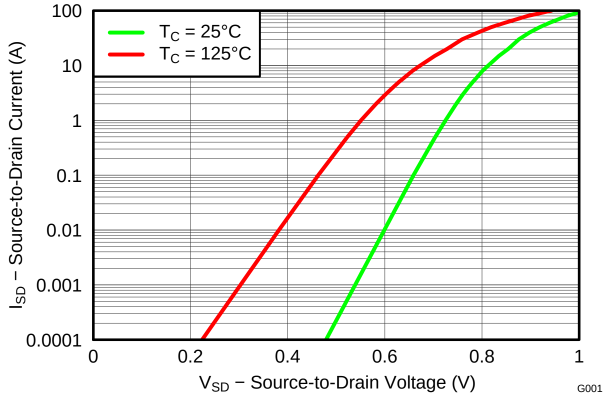


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

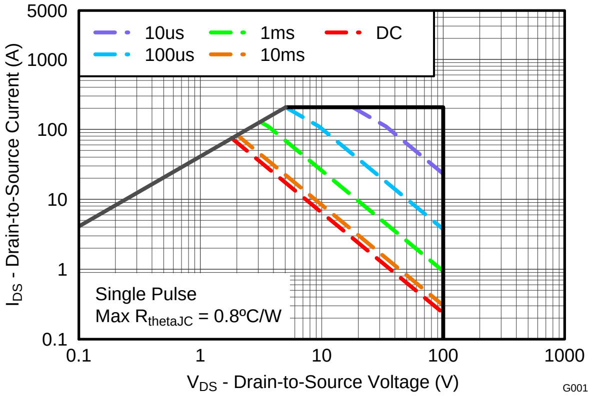


Figure 10. Maximum Safe Operating Area

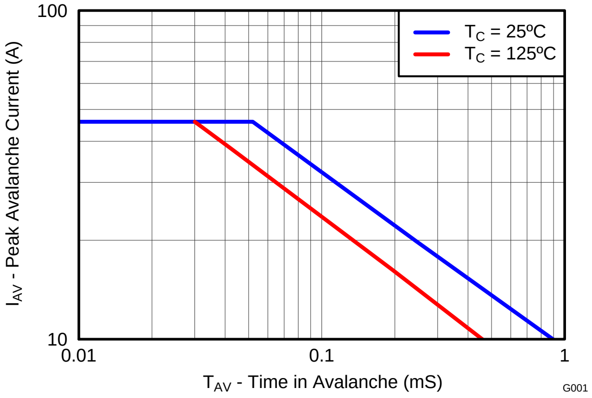


Figure 11. Single Pulse Unclamped Inductive Switching

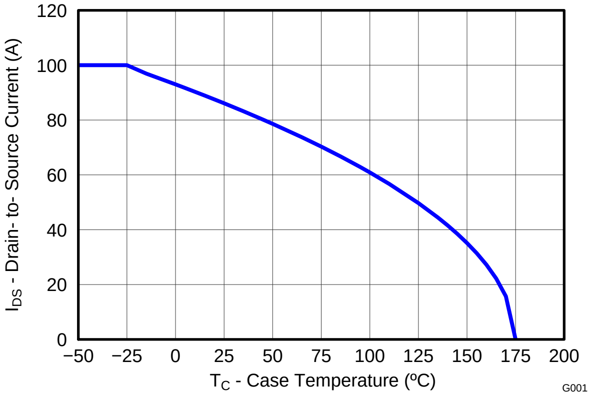


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

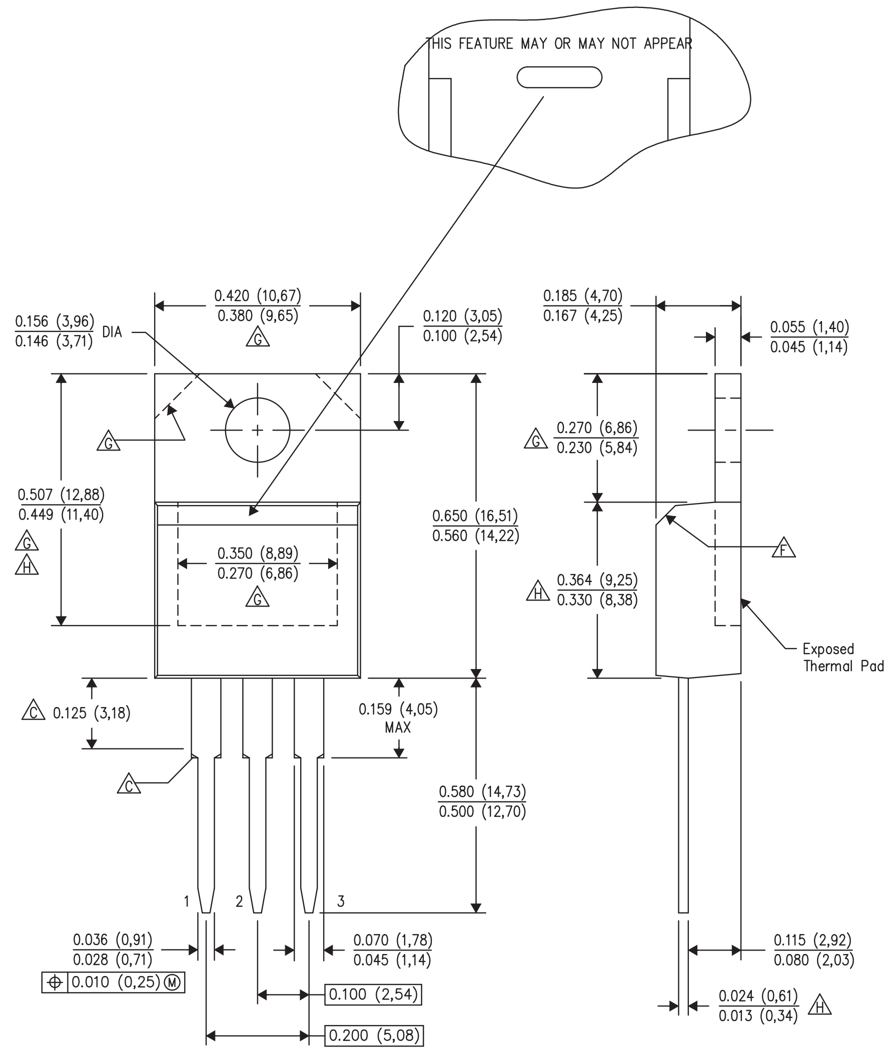
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KCS Package Dimensions



NOTES:

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area. Chamfer may or may not appear
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.
F. The chamfer is optional.
G. Thermal pad contour optional within these dimensions.
H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

Pin Configuration

Position	Designation
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19533KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS Exempt)	CU SN	N / A for Pkg Type	-55 to 175	CSD19533KCS	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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