# CSD19536KTT 100-V N-Channel NexFET™ Power MOSFET

## 1 Features

- Ultra-Low $Q_g$ and $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- $D^2PAK$ Plastic Package

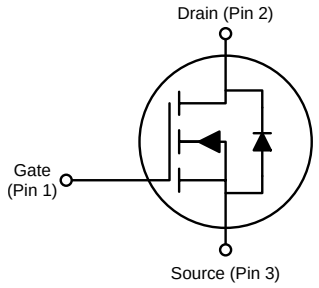
## 2 Applications

- Secondary Side Synchronous Rectifier
- Hot Swap
- Motor Control

## 3 Description

This 100-V, 2-mΩ, $D^2PAK$ (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

### Pin Out




### Product Summary

| $T_A$ = 25°C | | TYPICAL VALUE | | UNIT |
|---|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 100 | | V |
| $Q_g$ | Gate Charge Total (10 V) | 118 | | nC |
| $Q_{gd}$ | Gate Charge Gate-to-Drain | 17 | | nC |
| $R_{DS(on)}$ | Drain-to-Source On-Resistance | $V_{GS}$ = 6 V | 2.2 | mΩ |
| | | $V_{GS}$ = 10 V | 2 | |
| $V_{GS(th)}$ | Threshold Voltage | 2.5 | | V |

### Device Information(1)

| DEVICE | QTY | MEDIA | PACKAGE | SHIP |
|---|---|---|---|---|
| CSD19536KTT | 500 | 13-Inch Reel | $D^2PAK$ Plastic Package | Tape and Reel |
| CSD19536KTTT | 50 | | | |

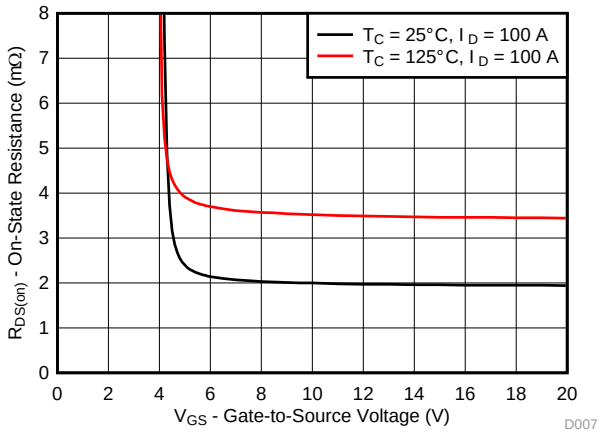
(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

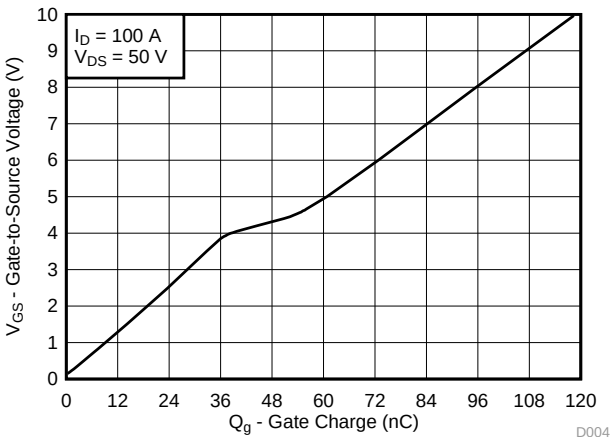
| $T_A$ = 25°C | | VALUE | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 100 | V |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $I_D$ | Continuous Drain Current (Package Limited) | 200 | A |
| | Continuous Drain Current (Silicon Limited), $T_C$ = 25°C | 272 | |
| | Continuous Drain Current (Silicon Limited), $T_C$ = 100°C | 192 | |
| $I_{DM}$ | Pulsed Drain Current(1) | 400 | A |
| $P_D$ | Power Dissipation | 375 | W |
| $T_J$, $T_{stg}$ | Operating Junction, Storage Temperature | –55 to 175 | °C |
| $E_{AS}$ | Avalanche Energy, Single Pulse $I_D$ = 127 A, L = 0.1 mH, $R_G$ = 25 Ω | 806 | mJ |

(1) Max $R_{\theta JC}$ = 0.4°C/W, Pulse duration ≤ 100 µs, Duty cycle ≤ 1%.

### $R_{DS(on)}$ vs $V_{GS}$




### Gate Charge



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## 4 Revision History

**Changes from Revision A (May 2015) to Revision B** **Page**

- Added *Receiving Notification of Documentation Updates* section ..... 7
- Updated package drawing ..... 8
- Updated PCB drawing ..... 9
- Updated stencil drawing ..... 10

**Changes from Original (March 2015) to Revision A** **Page**

- Added *Community Resources* section ..... 7
- Added PCB and stencil drawings in *Mechanical, Packaging, and Orderable Information* ..... 8

# 5 Specifications

## 5.1 Electrical Characteristics

$T_A$ = 25°C (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-source voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 100 | | | V |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{GS}$ = 0 V, $V_{DS}$ = 80 V | | | 1 | μA |
| $I_{GSS}$ | Gate-to-source leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 2.1 | 2.5 | 3.2 | V |
| $R_{DS(on)}$ | Drain-to-source on-resistance | $V_{GS}$ = 6 V, $I_D$ = 100 A | | 2.2 | 2.8 | mΩ |
| | | $V_{GS}$ = 10 V, $I_D$ = 100 A | | 2 | 2.4 | |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 10 V, $I_D$ = 100 A | | 329 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 50 V, $f$ = 1 MHz | | 9250 | 12000 | pF |
| $C_{oss}$ | Output capacitance | | | 1820 | 2370 | pF |
| $C_{rss}$ | Reverse transfer capacitance | | | 47 | 61 | pF |
| $R_G$ | Series gate resistance | | | 1.4 | 2.8 | Ω |
| $Q_g$ | Gate charge total (10 V) | $V_{DS}$ = 50 V, $I_D$ = 100 A | | 118 | 153 | nC |
| $Q_{gd}$ | Gate charge gate-to-drain | | | 17 | | nC |
| $Q_{gs}$ | Gate charge gate-to-source | | | 37 | | nC |
| $Q_{g(th)}$ | Gate charge at $V_{th}$ | | | 24 | | nC |
| $Q_{oss}$ | Output charge | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V | | 335 | | nC |
| $t_{d(on)}$ | Turnon delay time | $V_{DS}$ = 50 V, $V_{GS}$ = 10 V, $I_{DS}$ = 100 A, $R_G$ = 0 Ω | | 13 | | ns |
| $t_r$ | Rise time | | | 8 | | ns |
| $t_{d(off)}$ | Turnoff delay time | | | 32 | | ns |
| $t_f$ | Fall time | | | 6 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode forward voltage | $I_{SD}$ = 100 A, $V_{GS}$ = 0 V | | 0.9 | 1.1 | V |
| $Q_{rr}$ | Reverse recovery charge | $V_{DS}$= 50 V, $I_F$ = 100 A, di/dt = 300 A/μs | | 548 | | nC |
| $t_{rr}$ | Reverse recovery time | | | 103 | | ns |

## 5.2 Thermal Information

$T_A$ = 25°C (unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-case thermal resistance | | | 0.4 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | | | 62 | °C/W |

## 5.3 Typical MOSFET Characteristics

$T_A$ = 25°C (unless otherwise stated)

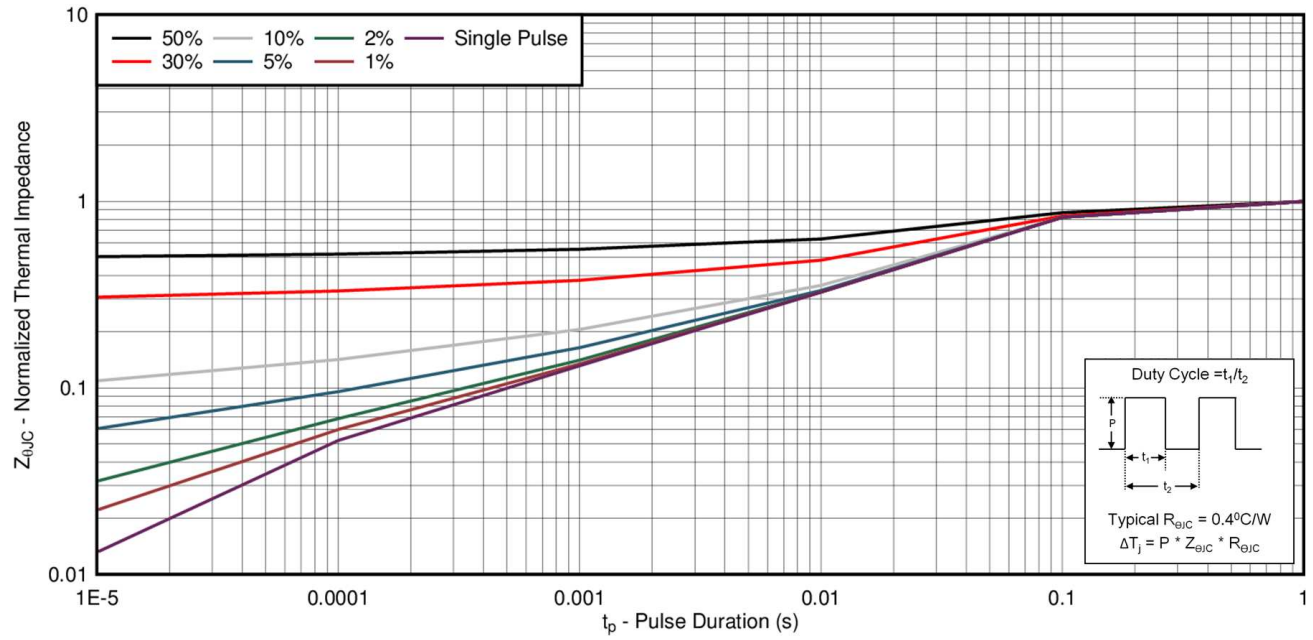


**Figure 1. Transient Thermal Impedance**

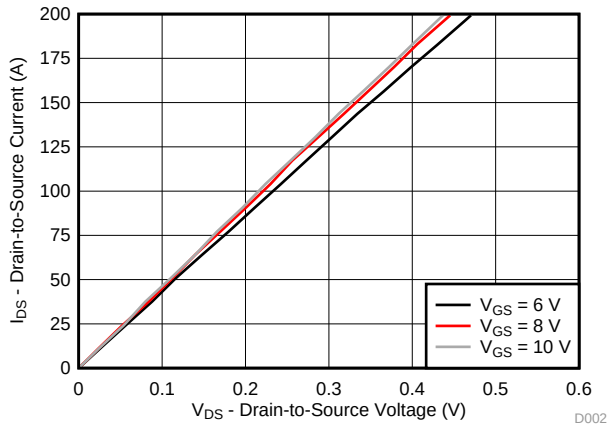


**Figure 2. Saturation Characteristics**

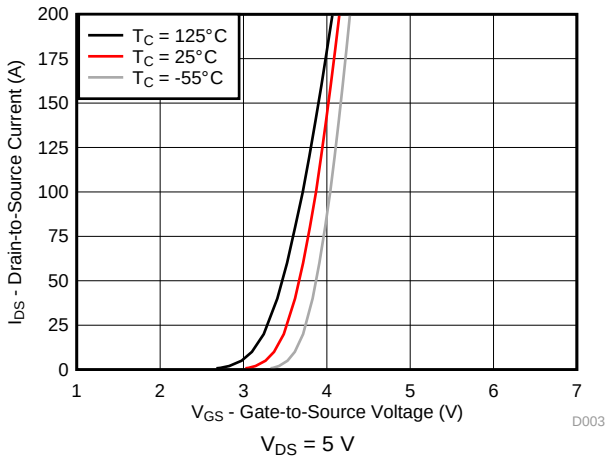


**Figure 3. Transfer Characteristics**

## Typical MOSFET Characteristics (continued)

$T_A$ = 25°C (unless otherwise stated)

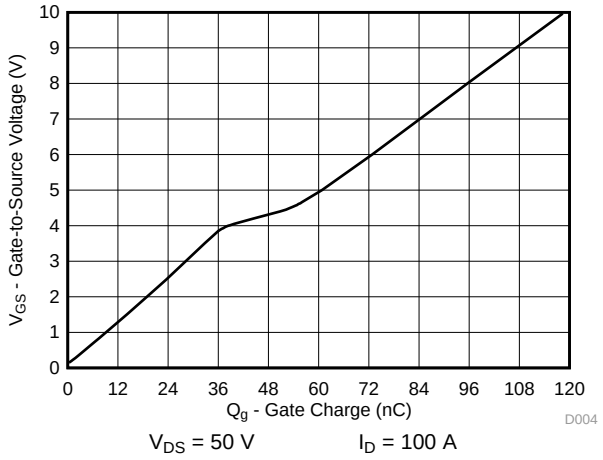


**Figure 4. Gate Charge**

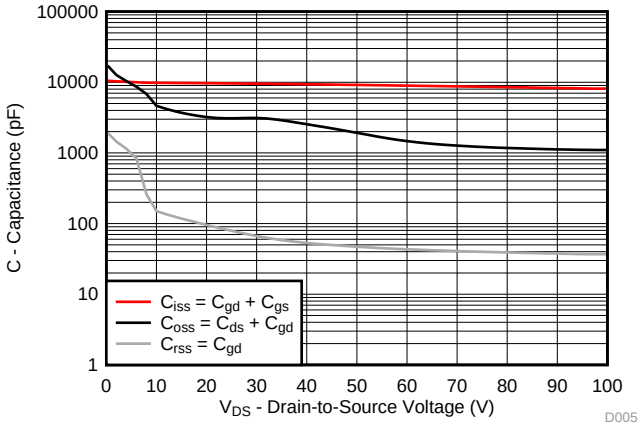


**Figure 5. Capacitance**

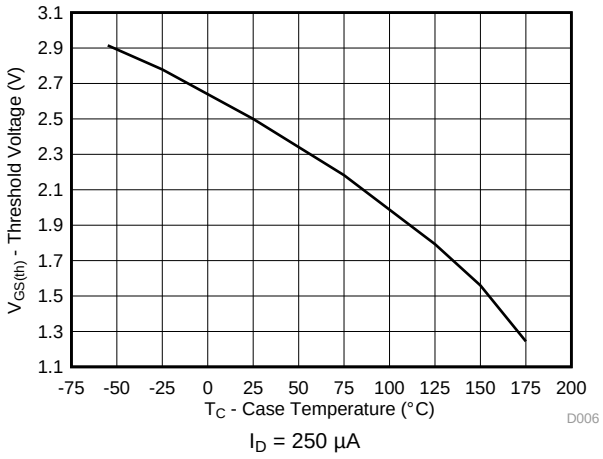


**Figure 6. Threshold Voltage vs Temperature**

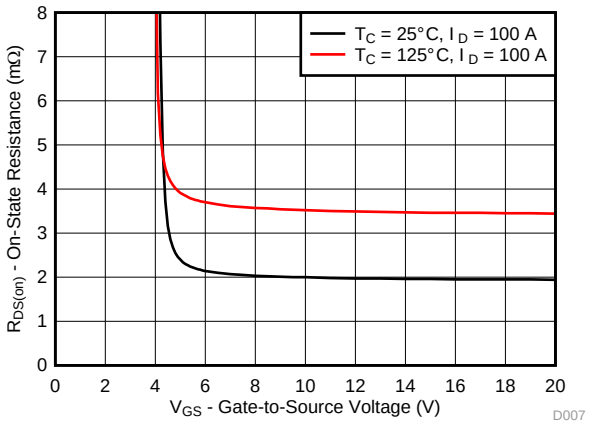


**Figure 7. On-State Resistance vs Gate-to-Source Voltage**

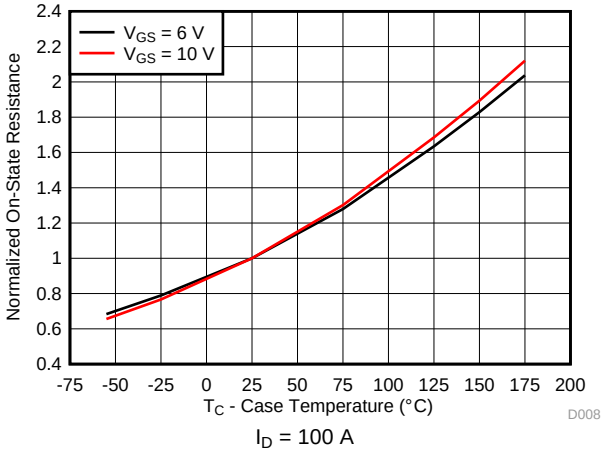


**Figure 8. Normalized On-State Resistance vs Temperature**

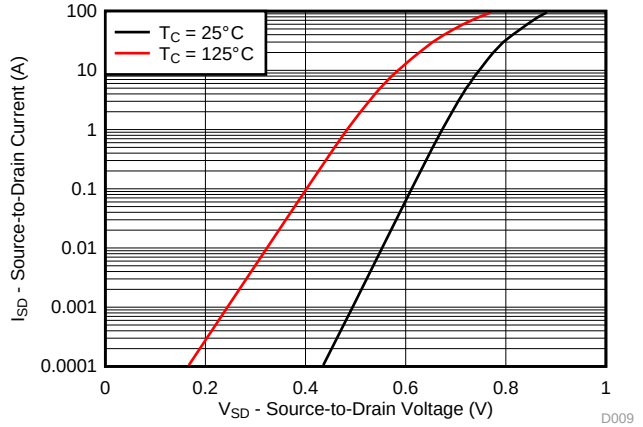


**Figure 9. Typical Diode Forward Voltage**

## Typical MOSFET Characteristics (continued)

$T_A$ = 25°C (unless otherwise stated)

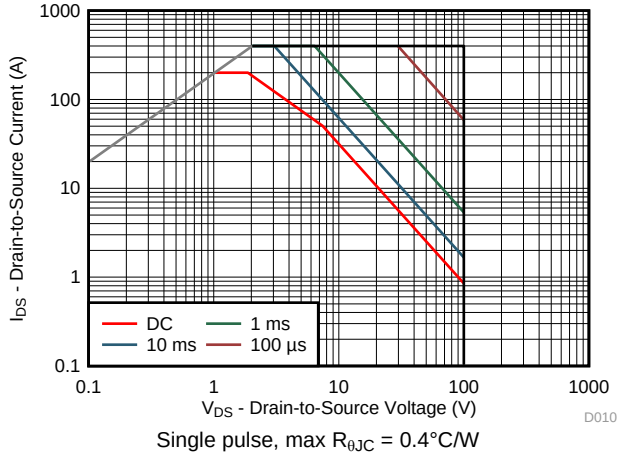


**Figure 10. Maximum Safe Operating Area**

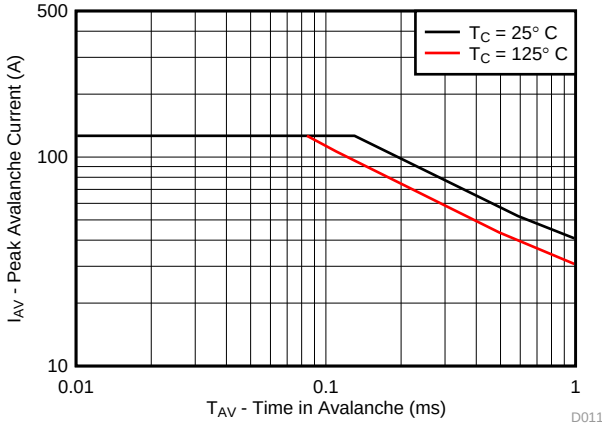


**Figure 11. Single Pulse Unclamped Inductive Switching**

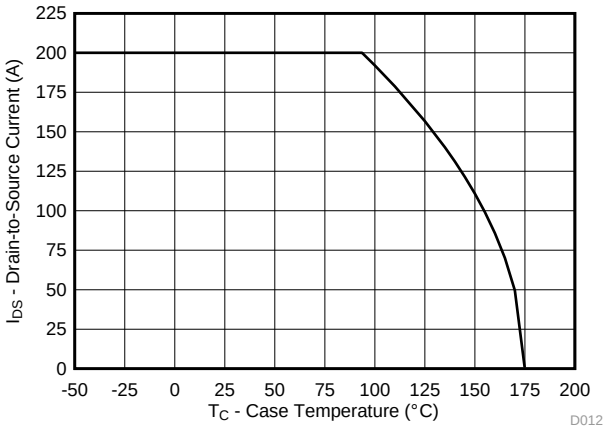


**Figure 12. Maximum Drain Current vs Temperature**

# 6 Device and Documentation Support

## 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 6.3 Trademarks

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All other trademarks are the property of their respective owners.

## 6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 6.5 Glossary

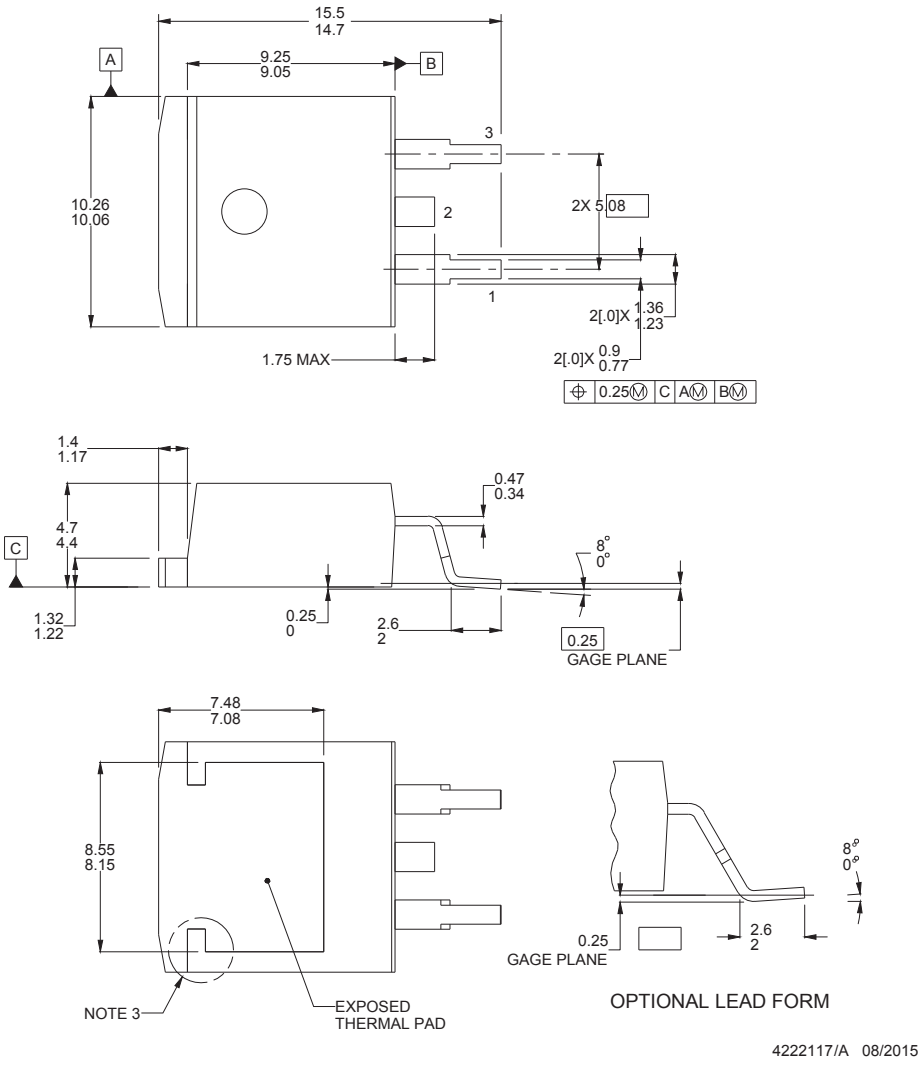
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 7.1 KTT Package Dimensions



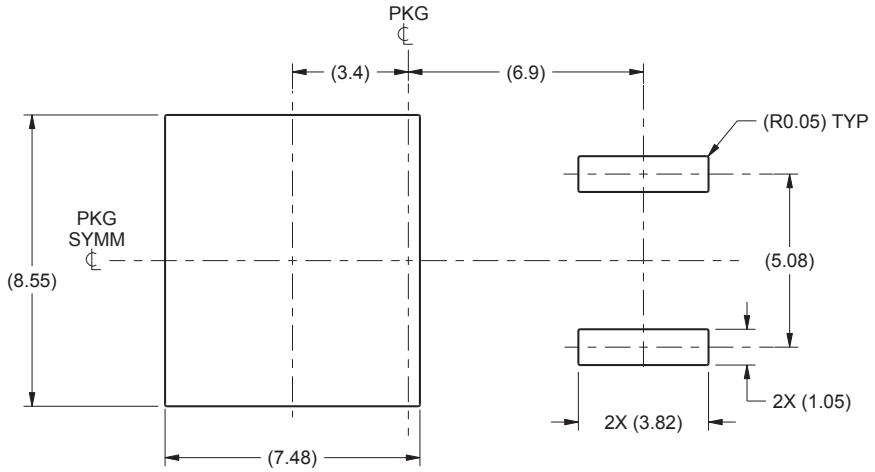

**Notes:**

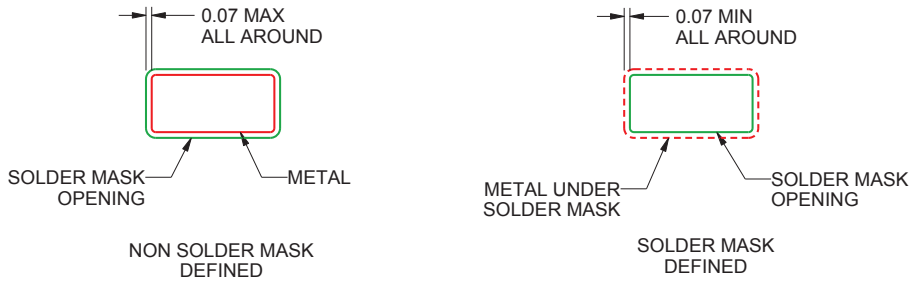
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.

**Table 1. Pin Configuration**

| POSITION | DESIGNATION |
|---|---|
| Pin 1 | Gate |
| Pin 2 / Tab | Drain |
| Pin 3 | Source |

## 7.2 Recommended PCB Pattern



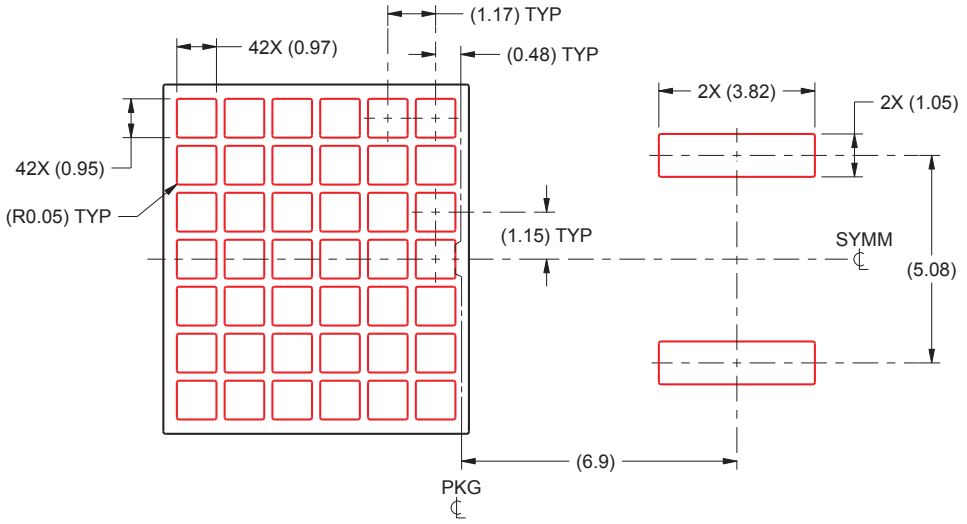




4222117/A 08/2015

**Note:**

1. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

## 7.3 Recommended Stencil Opening




**Notes:**

1. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
2. Board assembly site may have different recommendations for stencil design.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD19536KTT | ACTIVE | DDPAK/ TO-263 | KTT | 3 | 500 | Pb-Free (RoHS Exempt) | CU SN | Level-2-260C-1 YEAR | -55 to 175 | CSD19536KTT | Samples |
| CSD19536KTTT | ACTIVE | DDPAK/ TO-263 | KTT | 3 | 50 | Pb-Free (RoHS Exempt) | CU SN | Level-2-260C-1 YEAR | -55 to 175 | CSD19536KTT | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

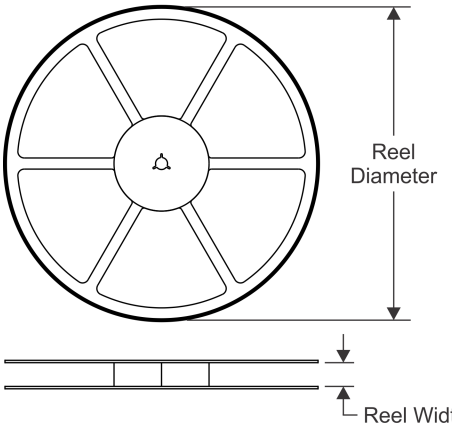
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

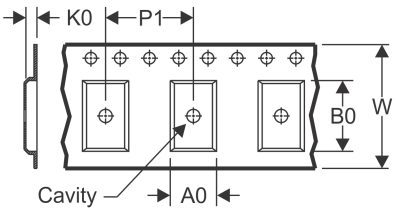
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

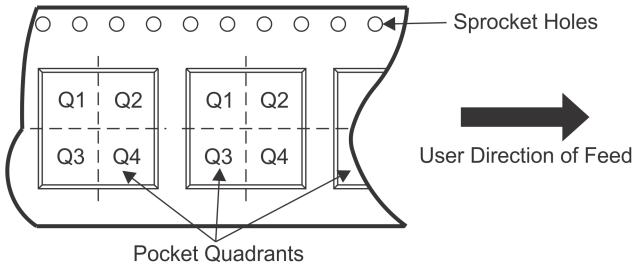



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

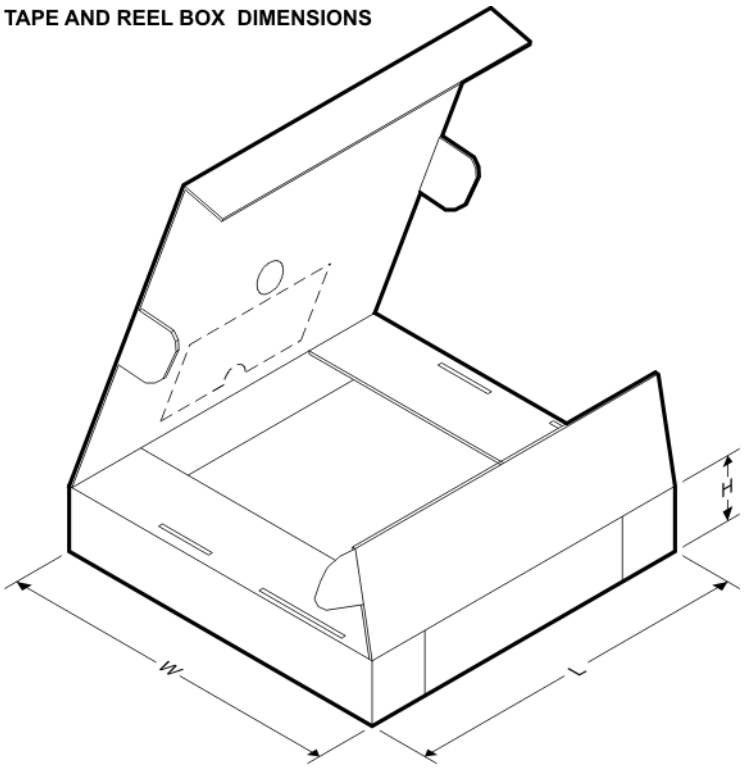
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD19536KTT | DDPAK/ TO-263 | KTT | 3 | 500 | 330.0 | 24.4 | 10.8 | 16.3 | 5.11 | 16.0 | 24.0 | Q2 |
| CSD19536KTTT | DDPAK/ TO-263 | KTT | 3 | 50 | 330.0 | 24.4 | 10.8 | 16.3 | 5.11 | 16.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CSD19536KTT | DDPAK/TO-263 | KTT | 3 | 500 | 340.0 | 340.0 | 38.0 |
| CSD19536KTTT | DDPAK/TO-263 | KTT | 3 | 50 | 340.0 | 340.0 | 38.0 |

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