CSD19538Q3A 100V N-Channel NexFET™ Power MOSFET

1 Features

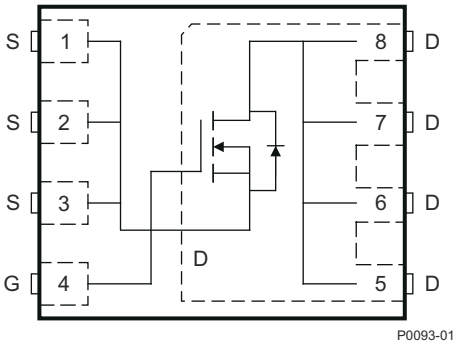
- Ultra-low Q_g and Q_{gd}
- Low-thermal resistance
- Avalanche rated
- Lead free
- RoHS compliant
- Halogen free
- SON 3.3mm × 3.3mm plastic package

2 Applications

- Power over Ethernet (PoE)
- Power sourcing equipment (PSE)
- Motor control

3 Description

This 100V, 49mΩ, SON 3.3mm × 3.3mm NexFET™ power MOSFET is designed to minimize conduction losses and reduce board footprint in PoE applications.



Top View

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	100		V
Q_g	Gate Charge Total (10V)	4.3		nC
Q_{gd}	Gate Charge Gate to Drain	0.8		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6V	58	mΩ
		V_{GS} = 10V	49	
$V_{GS(th)}$	Threshold Voltage	3.2		V

Package Information

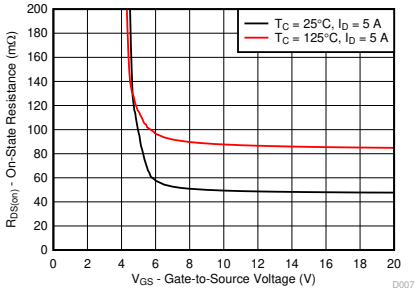
PART NUMBER	MEDIA	QTY	PACKAGE(1)	SHIP
CSD19538Q3A	13-in reel	3000	SON 3.30mm × 3.30mm(2) Plastic package	Tape and reel
CSD19538Q3AT	7-in reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

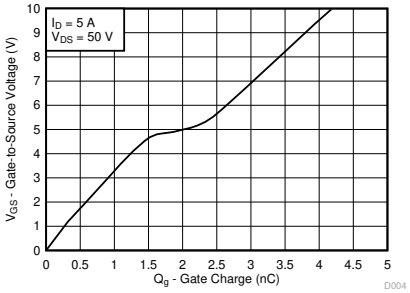
Absolute Maximum Ratings

TA = 25°C		VALUE	UNIT
V_{DS}	Drain-to-source voltage	100	V
V_{GS}	Gate-to-source voltage	±20	
I_D	Continuous drain current (package limited)	15	A
	Continuous drain current (silicon limited), T_C = 25°C	14	
	Continuous drain current(1)	4.9	
I_{DM}	Pulsed drain current(2)	37	
P_D	Power dissipation(1)	2.8	W
	Power dissipation, T_C = 25°C	23	
T_J	Operating junction temperature	–55 to 150	°C
T_{stg}	Storage temperature		
E_{AS}	Avalanche energy, single pulse I_D = 12.7A, L = 0.1mH, R_G = 25Ω	8.1	mJ

(1) Typical $R_{\theta JA}$ = 45°C/W on a 1-in², 2oz Cu pad on a 0.06 in thick FR4 PCB.
(2) Maximum $R_{\theta JC}$ = 5.5°C/W, pulse duration ≤ 100µs, duty cycle ≤ 1%.



$R_{DS(on)}$ versus V_{GS}



Gate Charge

Table of Contents

4 Specifications

4.1 Electrical Characteristics

T_A = 25°C

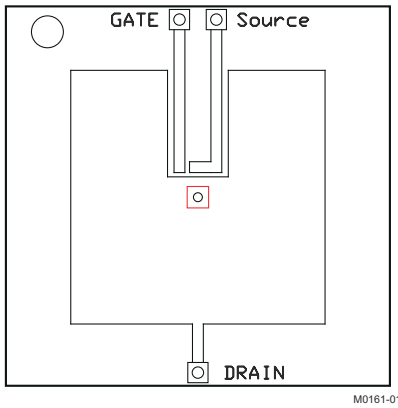
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 250µA	100			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 80V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2.8	3.2	3.8	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 6V, I_D = 5A		58	72	mΩ
		V_{GS} = 10V, I_D = 5A		49	59	
g_{fs}	Transconductance	V_{DS} = 10V, I_D = 5A		6.1		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz		349	454	pF
C_{oss}	Output capacitance			69	90	pF
C_{rss}	Reverse transfer capacitance			12.6	16.4	pF
R_G	Series gate resistance			4.6	9.2	Ω
Q_g	Gate charge total (10V)	V_{DS} = 50V, I_D = 5A		4.3		nC
Q_{gd}	Gate charge gate-to-drain			0.8		nC
Q_{gs}	Gate charge gate-to-source			1.6		nC
$Q_{g(th)}$	Gate charge at V_{th}			1		nC
Q_{oss}	Output charge	V_{DS} = 50V, V_{GS} = 0V		12.3		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 50V, V_{GS} = 10V, I_{DS} = 5A, R_G = 0 Ω		5		ns
t_r	Rise time			3		ns
$t_{d(off)}$	Turnoff delay time			7		ns
t_f	Fall time			2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 5A, V_{GS} = 0V		0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 50V, I_F = 5A, di/dt = 300A/µs		94		nC
t_{rr}	Reverse recovery time			32		ns

4.2 Thermal Information

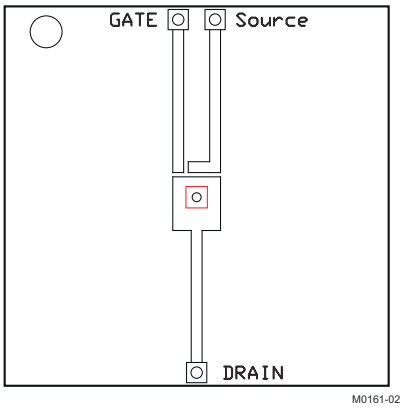
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			5.5	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1) (2)			55	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45cm^2), 2oz (0.071mm) thick Cu pad on a 1.5-in × 1.5-in (3.81cm × 3.81cm), 0.06-in (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by board design of the user.
(2) Device mounted on FR4 material with 1-in^2 (6.45cm^2), 2oz (0.071mm) thick Cu.



Maximum $R_{\theta JA}$ = 55°C/W When Mounted on 1-in^2 (6.45cm^2) of 2oz (0.071mm) Thick Cu.



Maximum $R_{\theta JA}$ = 195°C/W When Mounted on a Minimum Pad Area of 2oz (0.071mm) Thick Cu.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

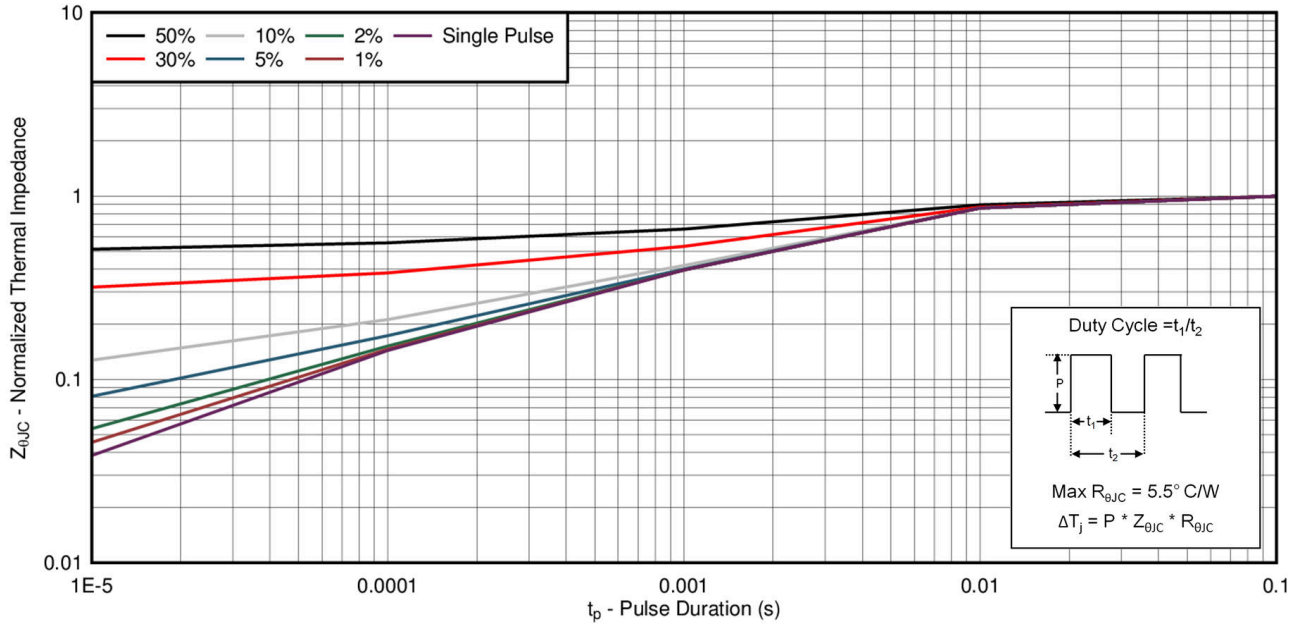


Figure 4-1. Transient Thermal Impedance

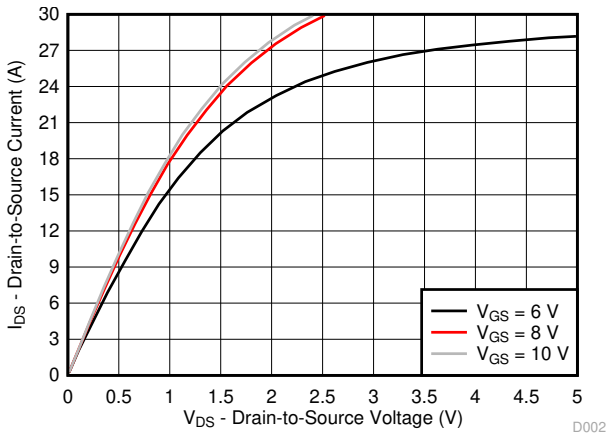
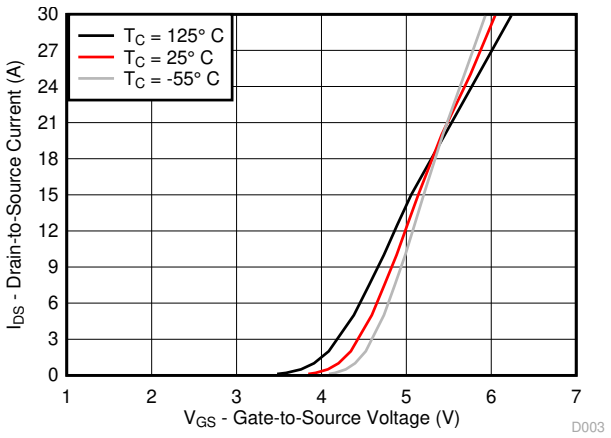
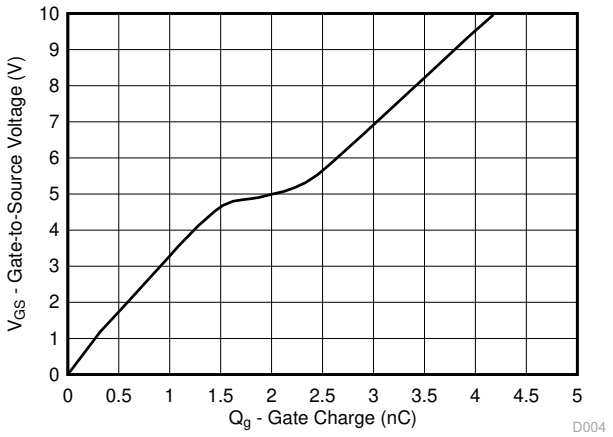


Figure 4-2. Saturation Characteristics



V_{DS} = 5V

Figure 4-3. Transfer Characteristics



I_D = 5A V_{DS} = 50V

Figure 4-4. Gate Charge

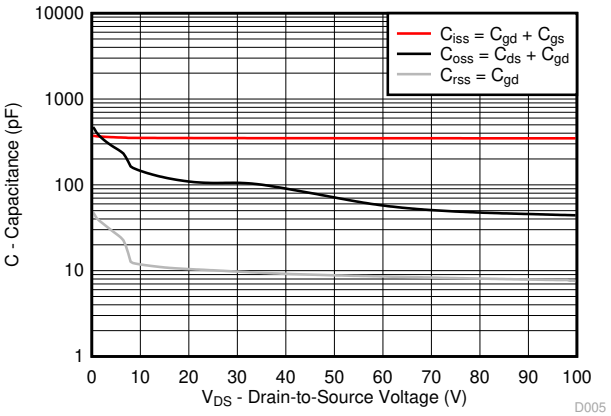
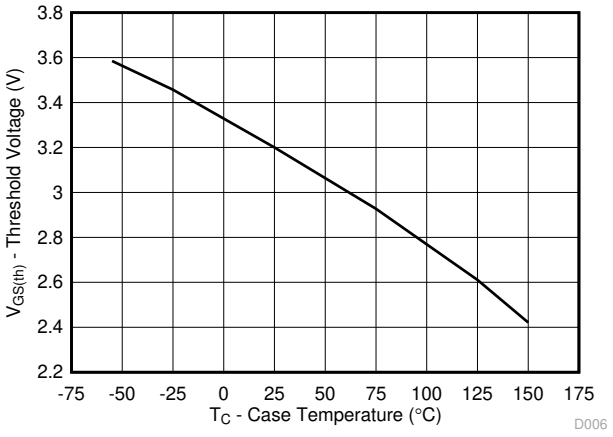


Figure 4-5. Capacitance



I_D = 250 µA

Figure 4-6. Threshold Voltage vs Temperature

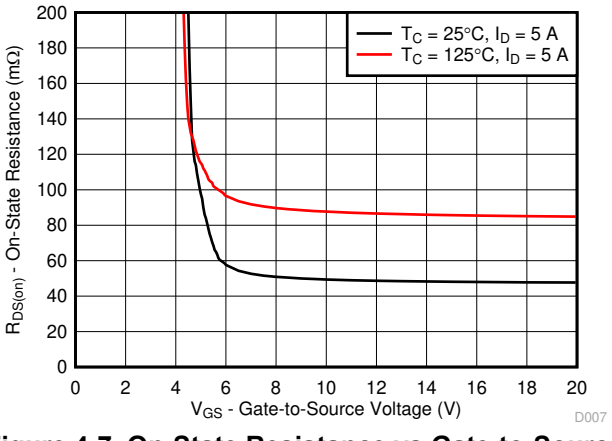
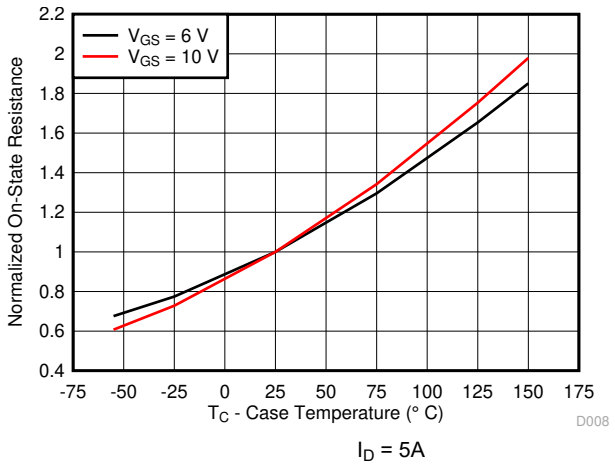


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 5A

Figure 4-8. Normalized On-State Resistance vs Temperature

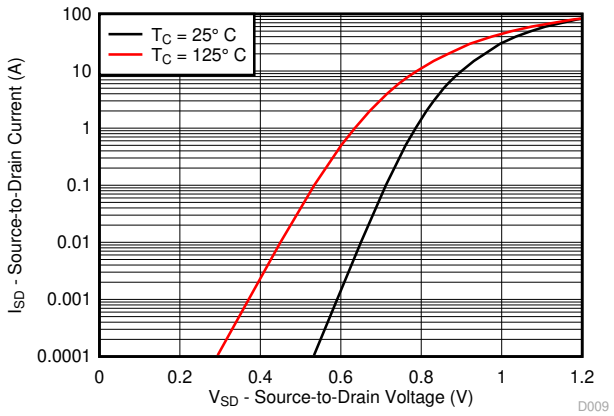
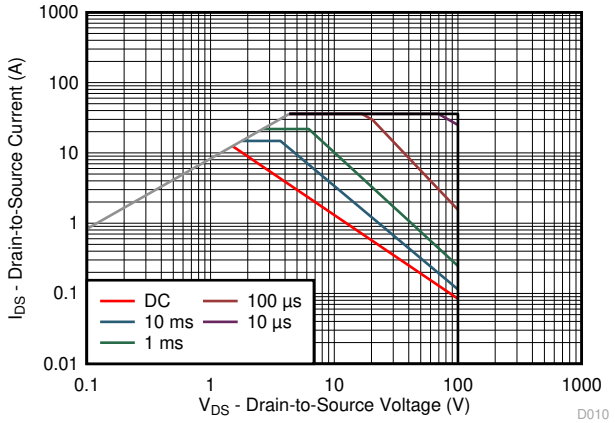


Figure 4-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 5.5°C/W

Figure 4-10. Maximum Safe Operating Area

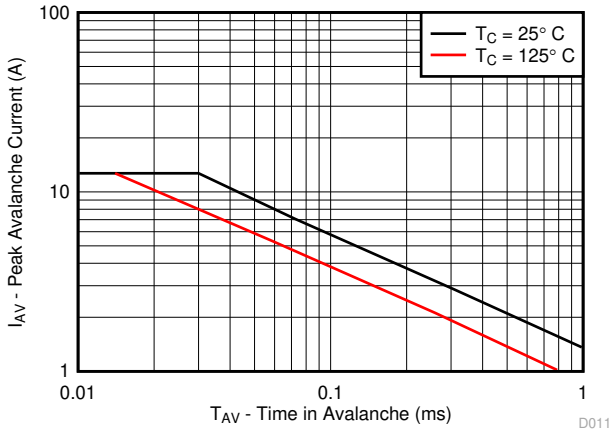


Figure 4-11. Single Pulse Unclamped Inductive Switching

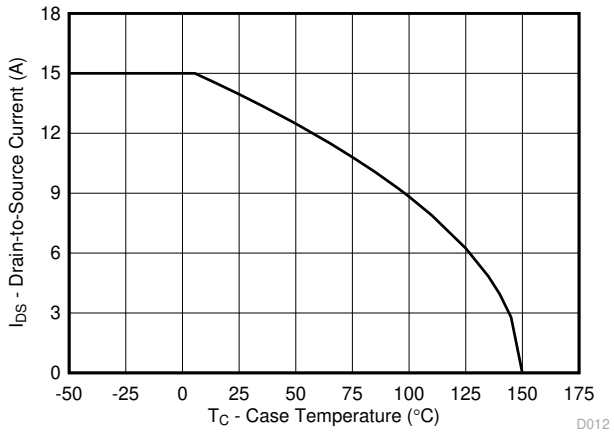


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

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5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2017) to Revision B (October 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (May 2016) to Revision A (March 2017)	Page
• Changed the test voltage V_{DS} in Gate Charge curve from 100V : to 50V	1
• Changed the test voltage V_{DS} in Figure 4-4 from 100V : to 50V	4

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD19538Q3A	Active	Production	VSONP (DNH) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	19538
CSD19538Q3A.B	Active	Production	VSONP (DNH) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	19538
CSD19538Q3AT	Active	Production	VSONP (DNH) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	19538
CSD19538Q3AT.B	Active	Production	VSONP (DNH) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	19538

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

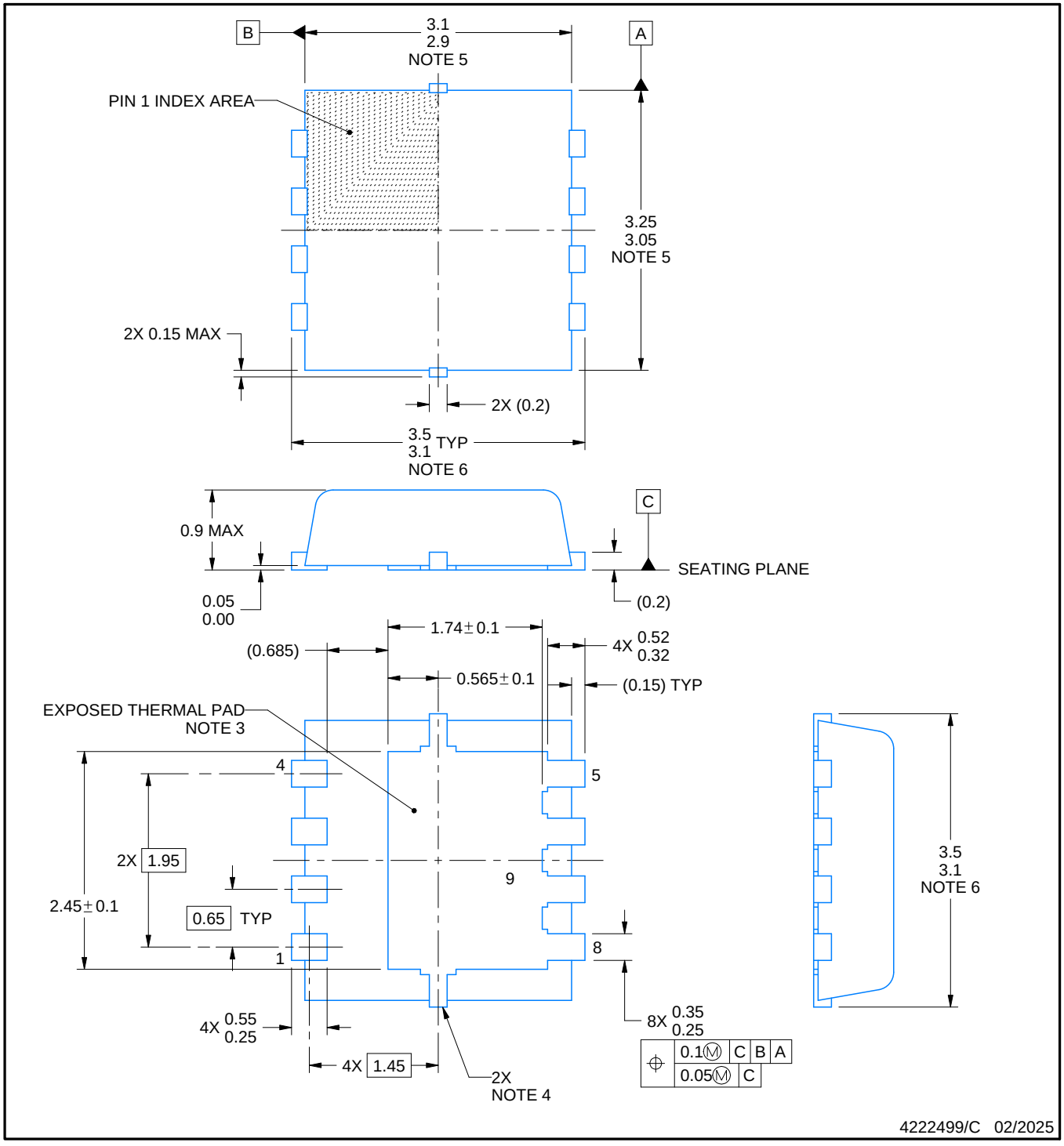
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DNH0008A

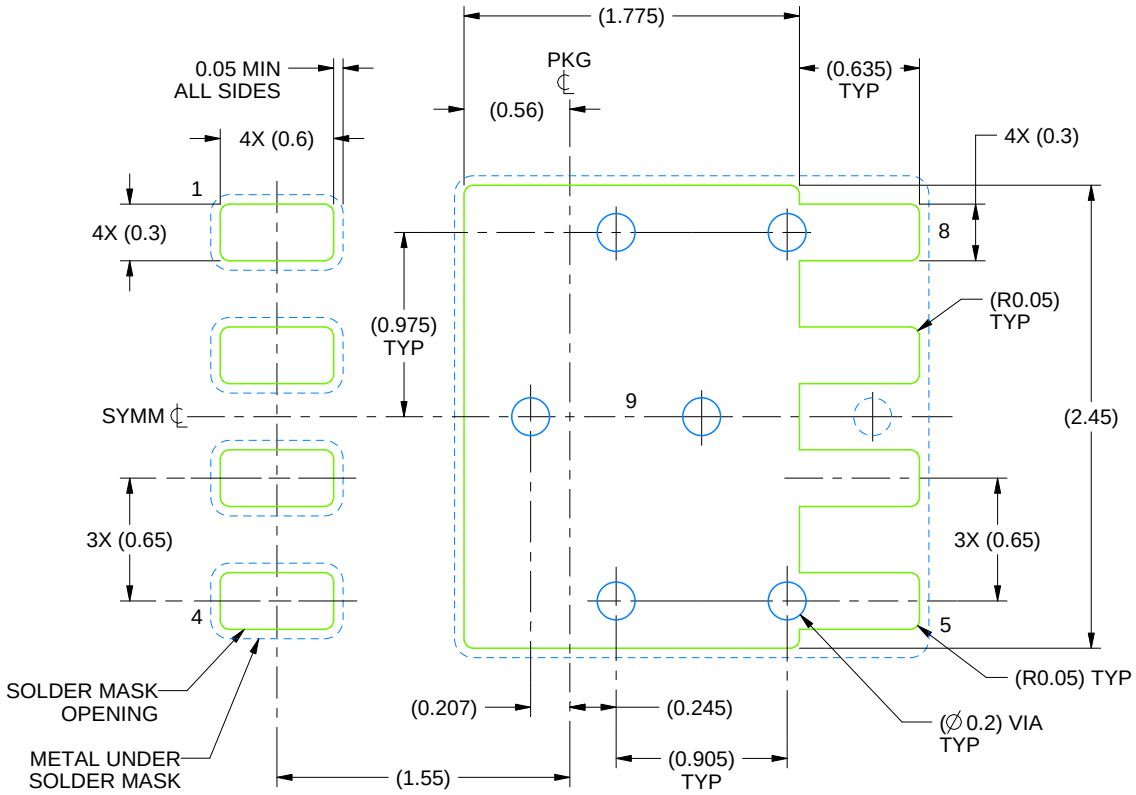
VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 25X

4222499/C 02/2025

NOTES: (continued)

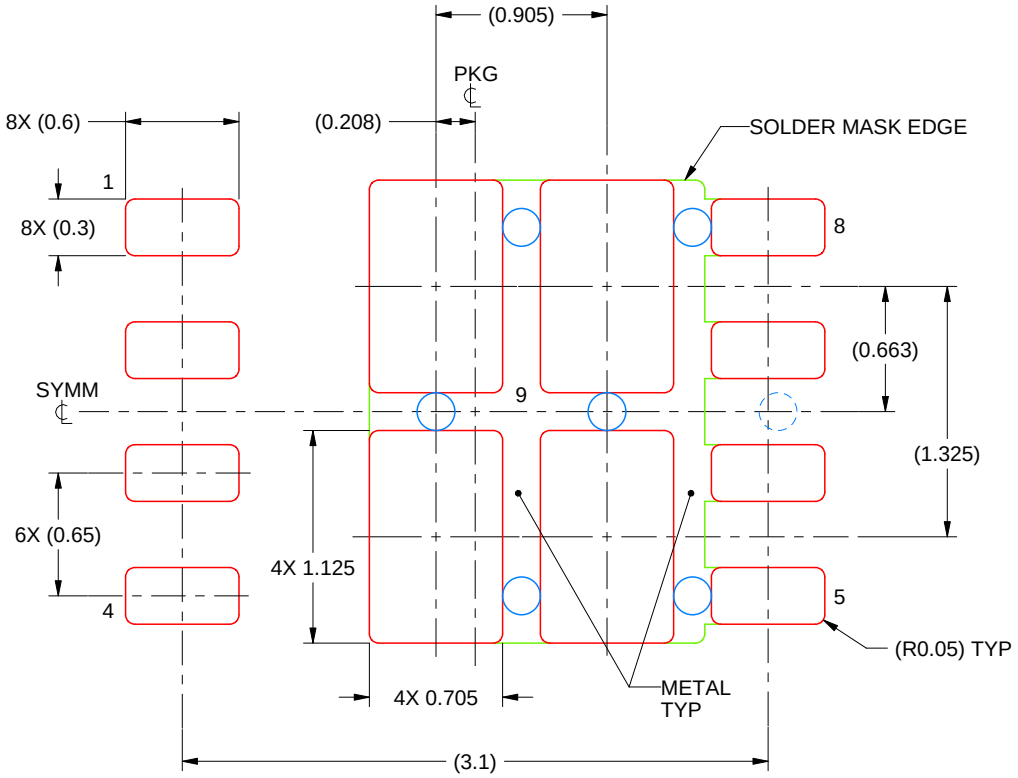
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DNH0008A

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025