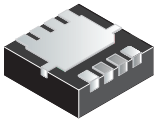


P-Channel NexFET™ Power MOSFETs

Check for Samples: CSD25401Q3

FEATURES

- **Ultra Low Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Low $R_{DS(on)}$**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 3.3mm x 3.3mm Plastic Package**

APPLICATIONS

- **DC-DC Converters**
- **Battery Management**
- **Load Switch**
- **Battery Protection**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion load management applications. The SON 3×3 package offers excellent thermal performance for the size of the package.

Figure 1. Top View

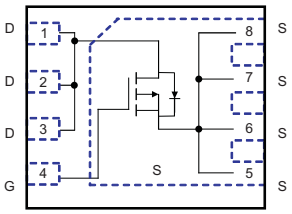


Table 1. PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	–20		V
Q_g	Gate Charge Total (4.5V)	8.8		nC
Q_{gd}	Gate Charge Gate to Drain	2.1		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = –2.5V	13.5	mΩ
		V_{GS} = –4.5V	8.8	mΩ
V_{th}	Threshold Voltage	–0.85		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD25401Q3	SON 3 × 3 Plastic Package	13-inch reel	2500	Tape and Reel

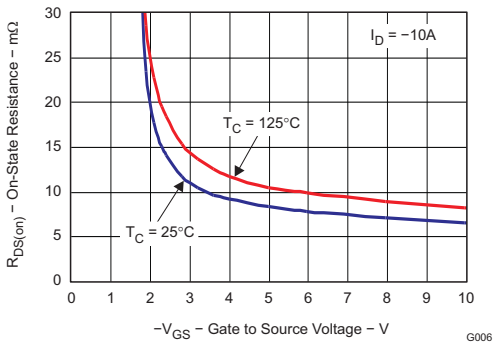
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	–20	V
V_{GS}	Gate to Source Voltage	+12 / -12	V
I_D	Continuous Drain Current, T_C = 25°C	–60	A
	Continuous Drain Current(1)	–14	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	–82	A
P_D	Power Dissipation(1)	2.8	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C

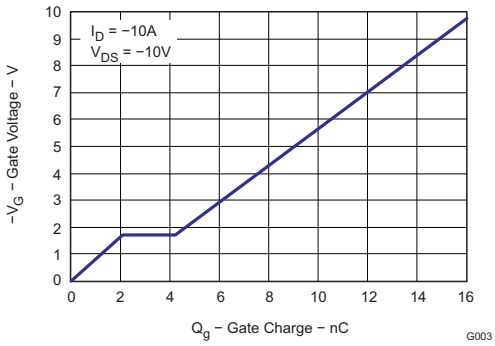
(1) $R_{\theta JA}$ = 45°C/W on 1inch^2 Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300µs , duty cycle ≤2%

$R_{DS(ON)}$ vs V_{GS}



Gate Charge



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NexFET is a trademark of Texas Instruments.

ELECTRICAL CHARACTERISTICS

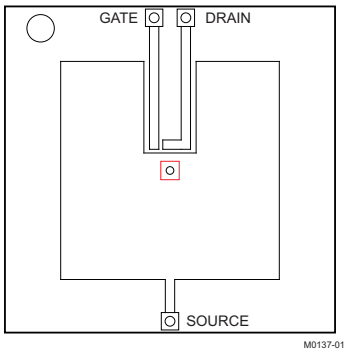
(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = –250µA	–20			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = –20V to –16V			–1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = ±12V			–100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = –250µA	–0.6	–0.85	–1.2	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = –2.5V, I_D = –10A		13.5	18.2	mΩ
		V_{GS} = –4.5V, I_D = –10A		8.8	11.7	mΩ
g_{fs}	Transconductance	V_{DS} = –15V, I_D = –10A		43		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = –10V, f = 1MHz		1070	1400	pF
C_{OSS}	Output Capacitance			560	730	pF
C_{RSS}	Reverse Transfer Capacitance			180	230	pF
Q_g	Gate Charge Total (4.5V)	V_{DS} = –10V, I_D = –10A		8.8	12.3	nC
Q_{gd}	Gate Charge Gate to Drain			2.1		nC
Q_{gs}	Gate Charge Gate to Source			2.1		nC
$Q_{g(th)}$	Gate Charge at Vth			0.9		nC
Q_{OSS}	Output Charge	V_{DS} = –10V, V_{GS} = 0V		8.2		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10V, V_{GS} = –4.5V, I_D = –10A , R_G = 5.1Ω		8.1		ns
t_r	Rise Time			3.9		ns
$t_{d(off)}$	Turn Off Delay Time			13.5		ns
t_f	Fall Time			12.6		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = –10A, V_{GS} = 0V		–0.7	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = –12.5V, I_F = –10A, di/dt = 300A/µs		17.4		nC
t_{rr}	Reverse Recovery Time			21		ns

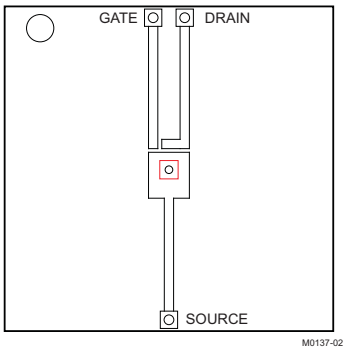
THERMAL INFORMATION

THERMAL METRIC(1)(2)		CSD25401Q3 8 PIN	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	42.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	20.6	
θ_{JB}	Junction-to-board thermal resistance	8.8	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	8.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.



Max $R_{\theta JA}$ = 57°C/W when mounted on 1inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 158°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

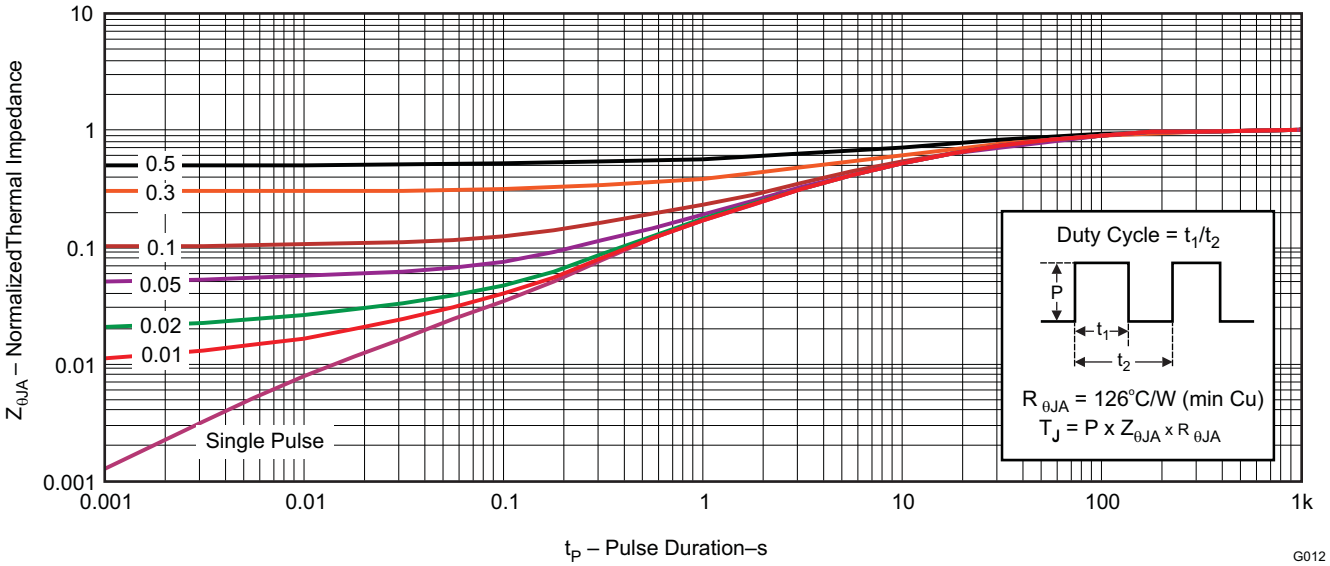


Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

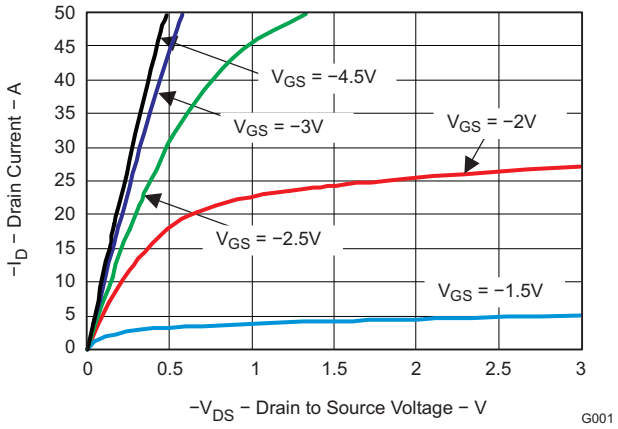


Figure 3. Saturation Characteristics

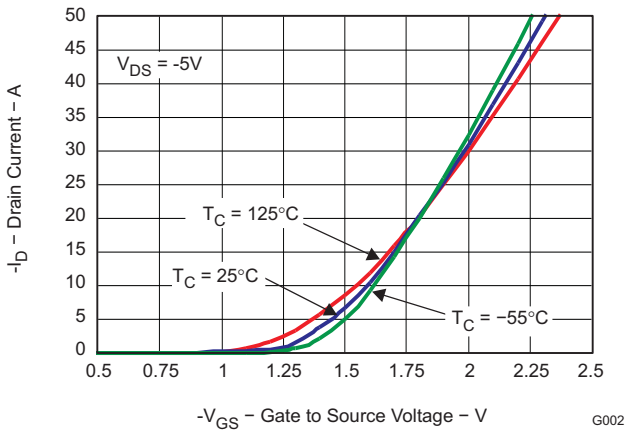


Figure 4. Transfer Characteristics

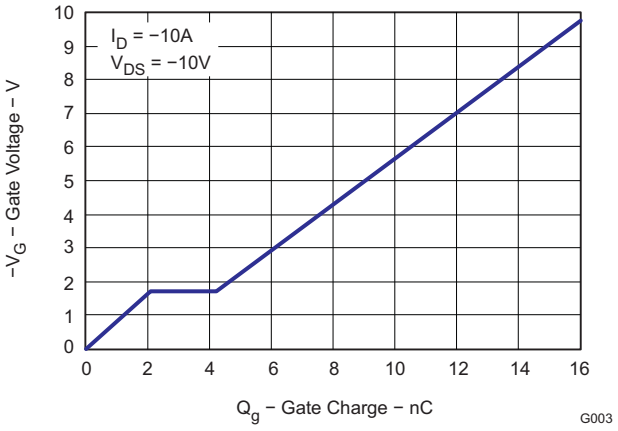


Figure 5. Gate Charge

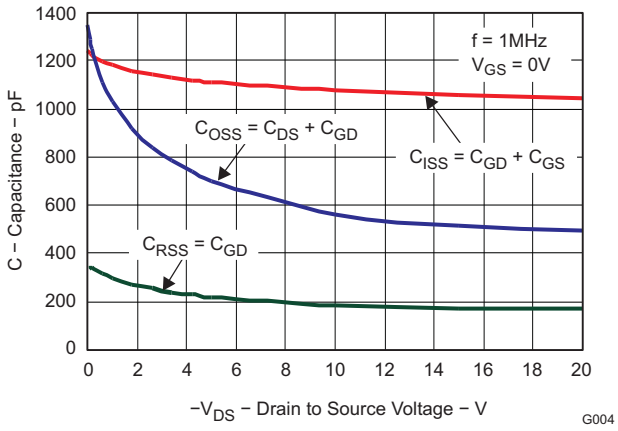


Figure 6. Capacitance

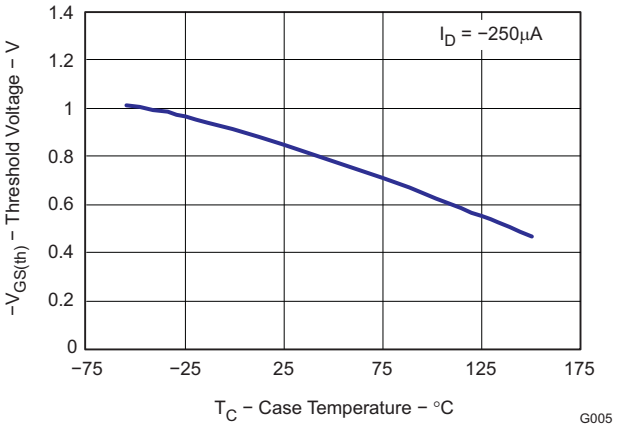


Figure 7. Threshold Voltage vs. Temperature

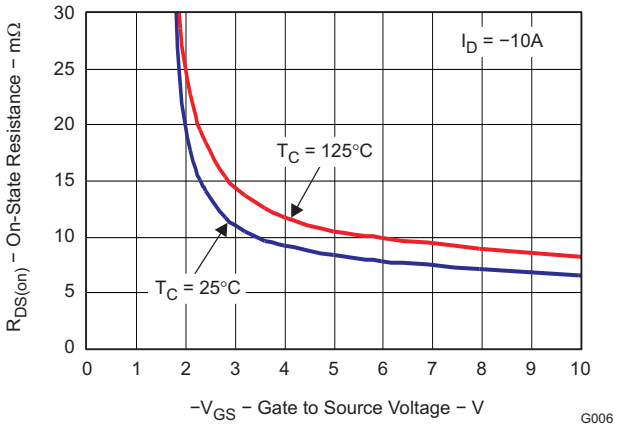


Figure 8. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

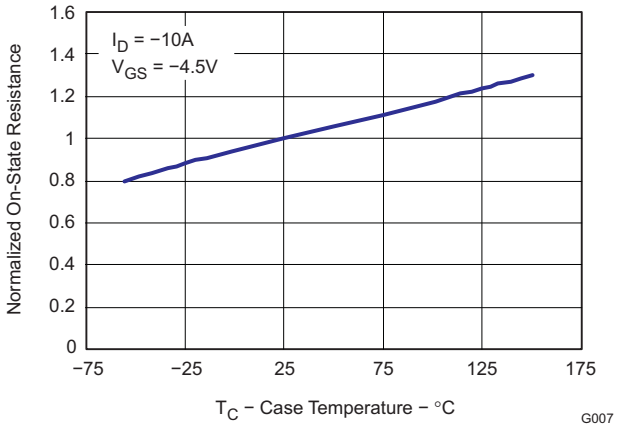


Figure 9. On Resistance vs. Temperature

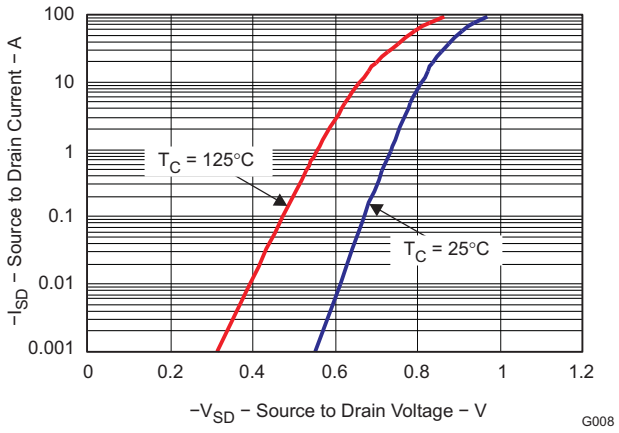


Figure 10. Typical Diode Forward Voltage

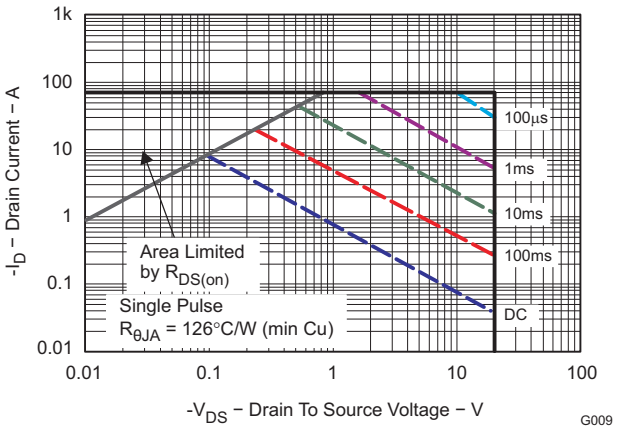


Figure 11. Maximum Safe Operating Area

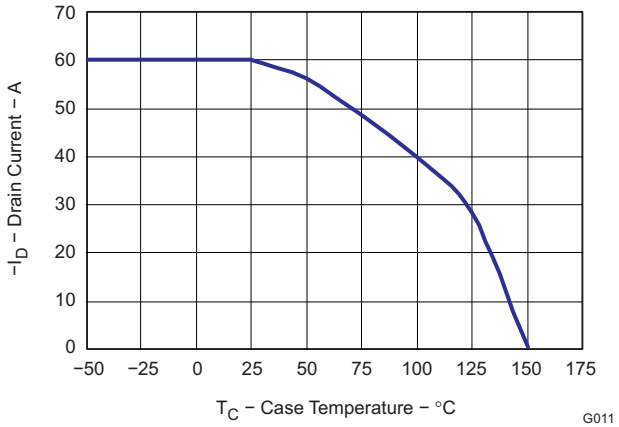
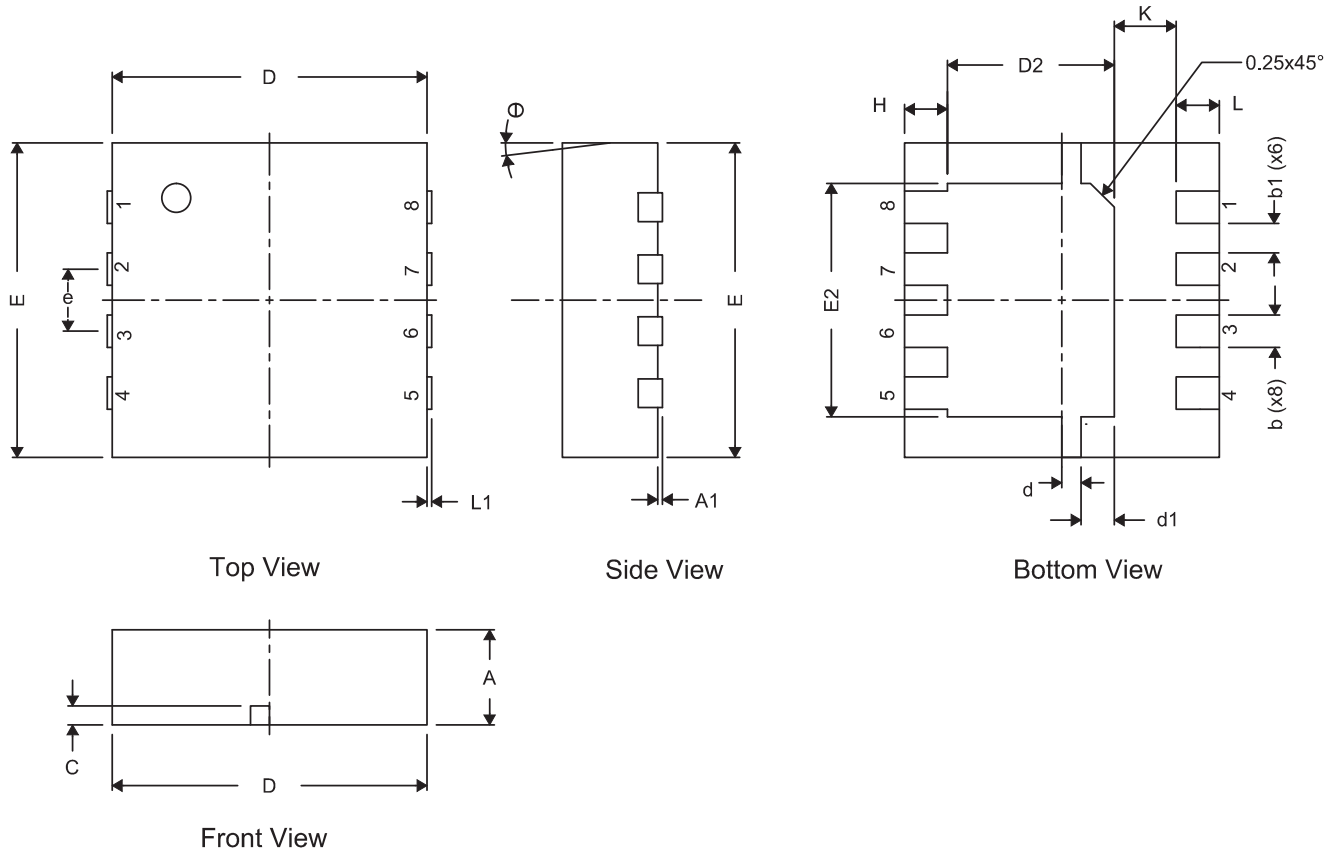


Figure 12. Maximum Drain Current vs. Temperature

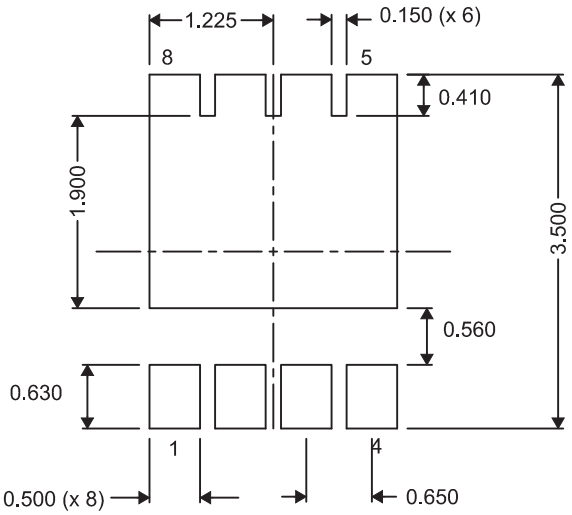
MECHANICAL DATA

CSD25401Q3 Package Dimensions

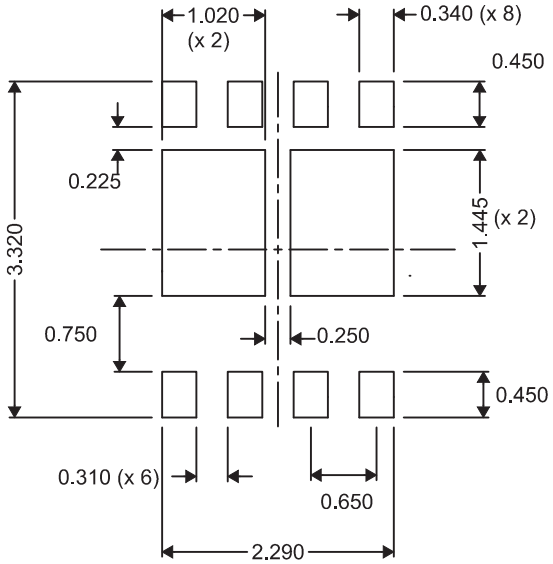


DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1		0.310 NOM			0.012 NOM	
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e		0.650 TYP			0.026 TYP	
H	0.35	0.450	0.550	0.014	0.018	0.022
K		0.650 TYP			0.026 TYP	
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0		0	0		0
θ	0		0	0		0

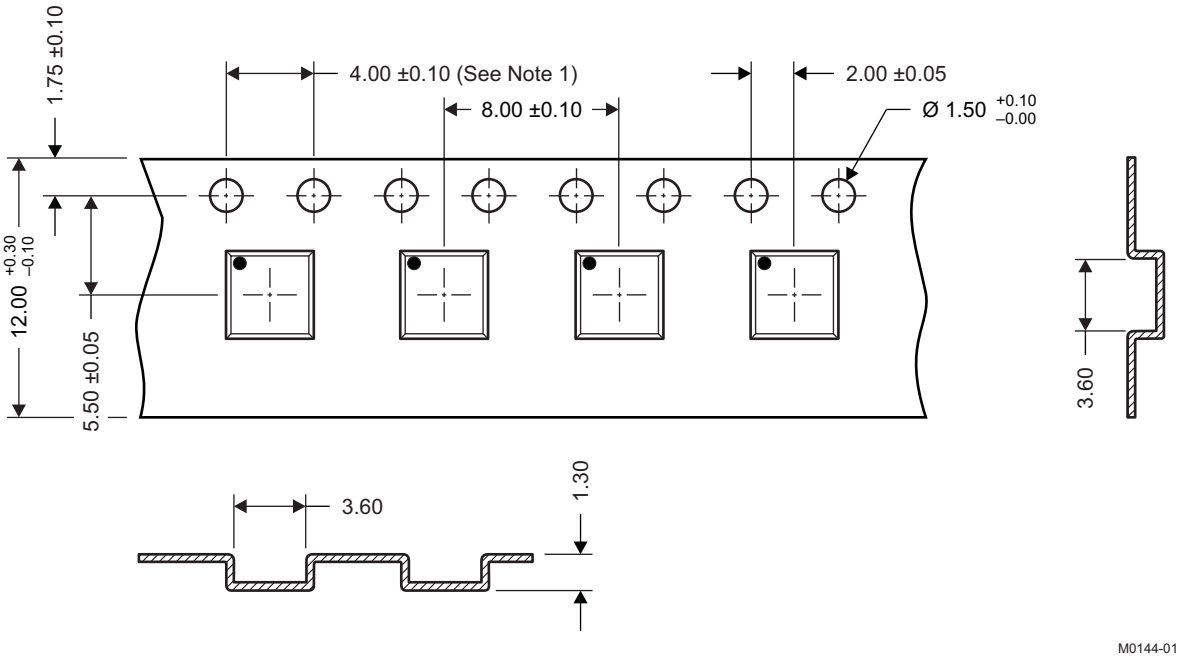
Recommended PCB Pattern



Recommended Stencil Opening



Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material:black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: 0.30 ±0.05mm
6. MSL1 260°C (IR and Conection) PbF Reflow Compatible

REVISION HISTORY

Changes from Original (August 2009) to Revision A	Page
• Changed 300s to 300µs in Note 2 of the Abs Max Ratings table	1
• Changed Q_g Gate Charge Total (4.5V) - max value From: 2.3 To: 12.3	2

Changes from Revision A (October 2009) to Revision B	Page
• Deleted the Package Marking Information section	8

Changes from Revision B (October 2010) to Revision C	Page
• Replaced the THERMAL CHARACTERISTICS table with the new Thermal Information Table	2
• Changed the CSD25401Q3 Package Dimensions section	6
• Changed the Recommended PCB Pattern section	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25401Q3	OBSOLETE	VSON-CLIP	DQG	8		TBD	Call TI	Call TI	-55 to 150	CSD25401	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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