CSD25483F4 20 V P-Channel FemtoFET™ MOSFET

1 Features

- Ultra-Low On-Resistance
- Ultra-Low Q_g and Q_{gd}
- High Operating Drain Current
- Ultra-Small Footprint (0402 Case Size)
  - 1.0 mm × 0.6 mm
- Ultra-Low Profile
  - 0.35 mm Max Height
- Integrated ESD Protection Diode
  - Rated >4 kV HBM
  - Rated >2 kV CDM
- Lead and Halogen Free
- RoHS Compliant

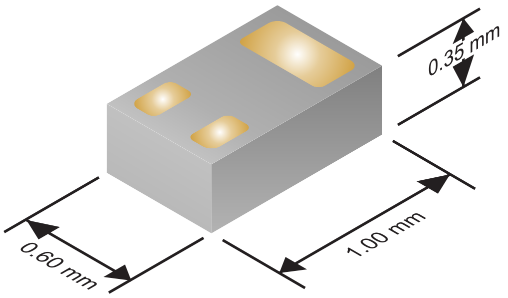
2 Applications

- Optimized for load Switch Applications
- Optimized for General Purpose Switching Applications
- Battery Applications
- Handheld and Mobile Applications

3 Description

This 210 mΩ, 20 V P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

Typical Part Dimensions



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	959		pC
Q_{gd}	Gate Charge Gate-to-Drain	161		pC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V	530	mΩ
		V_{GS} = –2.5 V	338	mΩ
		V_{GS} = –4.5 V	210	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.95		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD25483F4	3000	7-Inch Reel	Femto (0402) 1.0 mm × 0.6 mm Land Grid Array (LGA)	Tape and Reel
CSD25483F4T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–12	V
I_D	Continuous Drain Current(1)	–1.6	A
I_{DM}	Pulsed Drain Current(2)	–6.5	A
I_G	Continuous Gate Clamp Current	–35	mA
	Pulsed Gate Clamp Current(2)	–350	
P_D	Power Dissipation(1)	500	mW
$V_{(ESD)}$	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	2	kV
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Typical $R_{\theta JA}$ = 85°C/W on 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300 μs, duty cycle ≤2%

Top View

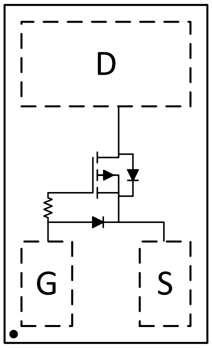


Table of Contents

4 Revision History

Changes from Revision C (July 2014) to Revision D	Page
• Corrected timing V_{DS} to read –10 V	3

Changes from Revision B (February 2014) to Revision C	Page
• Corrected capacitance units to read pF in Figure 5	5

Changes from Revision A (December 2013) to Revision B	Page
• Updated lead and halogen free in features	1
• Added I_G parameter	1
• Lowered I_{DSS} limit	3
• Lowered I_{GSS} limit	3

Changes from Original (October 2013) to Revision A	Page
• Fixed resistance typo	1
• Added small reel	1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–20			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–100	nA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –12 V			–50	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.70	–0.95	–1.2	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		530	1070	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.5 A		338	390	mΩ
		V_{GS} = –4.5 V, I_{DS} = –0.5 A		210	245	mΩ
		V_{GS} = –8 V, I_{DS} = –0.5 A		175	205	mΩ
g_{fs}	Transconductance	V_{DS} = –10 V, I_{DS} = –0.5 A		1.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		198		pF
C_{oss}	Output Capacitance			82		pF
C_{rss}	Reverse Transfer Capacitance			5.8		pF
R_G	Series Gate Resistance			20		Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = –10 V, I_{DS} = –0.5 A		959		pC
Q_{gd}	Gate Charge Gate-to-Drain			160		pC
Q_{gs}	Gate Charge Gate-to-Source			252		pC
$Q_{g(th)}$	Gate Charge at V_{th}			122		pC
Q_{oss}	Output Charge	V_{DS} = –10 V, V_{GS} = 0 V		1081		pC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.5 A,R_G = 2 Ω		4.3		ns
t_r	Rise Time			3.7		ns
$t_{d(off)}$	Turn Off Delay Time			17.4		ns
t_f	Fall Time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = –0.5 A, V_{GS} = 0 V		–0.75		V
Q_{rr}	Reverse Recovery Charge	V_{DS}= –10 V, I_F = –0.5 A, di/dt = 100 A/μs		1060		pC
t_{rr}	Reverse Recovery Time			7.5		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{θJA}$	Junction-to-Ambient Thermal Resistance (1)	85	°C/W
	Junction-to-Ambient Thermal Resistance (2)	245	

(1) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

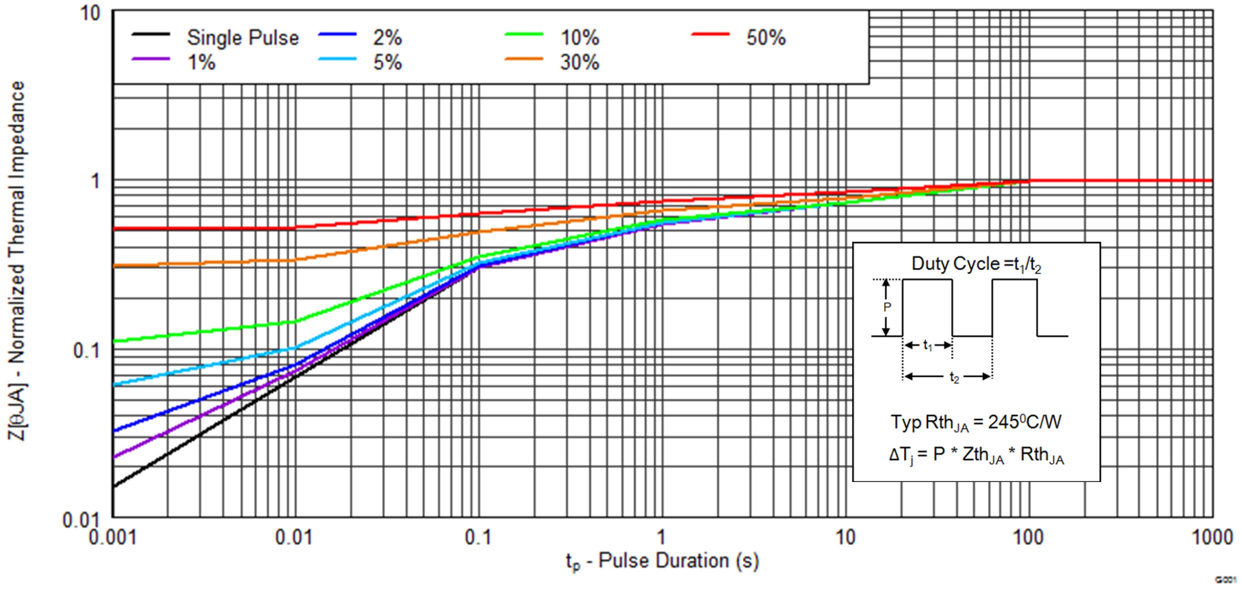


Figure 1. Transient Thermal Impedance

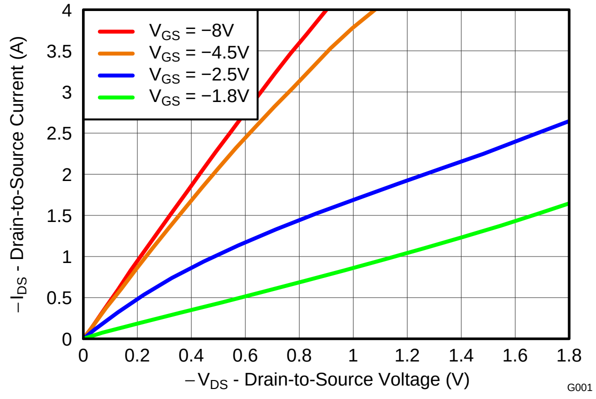


Figure 2. Saturation Characteristics

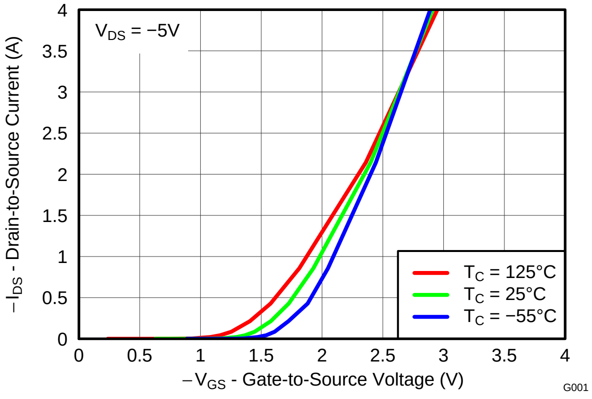


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

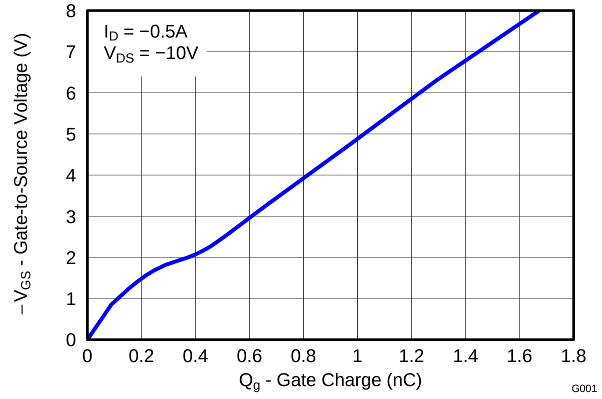


Figure 4. Gate Charge

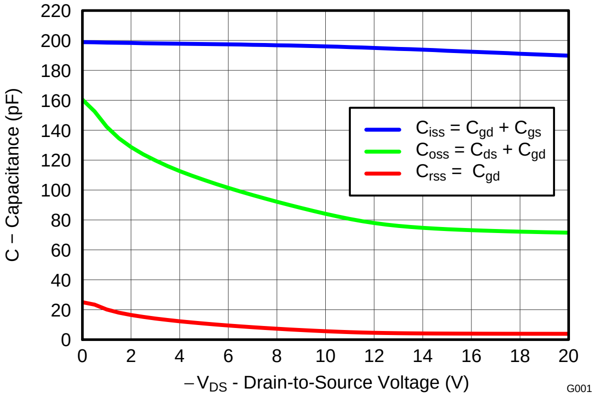


Figure 5. Capacitance

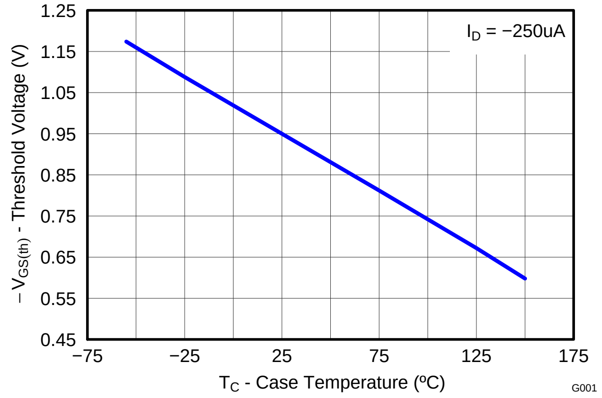


Figure 6. Threshold Voltage vs Temperature

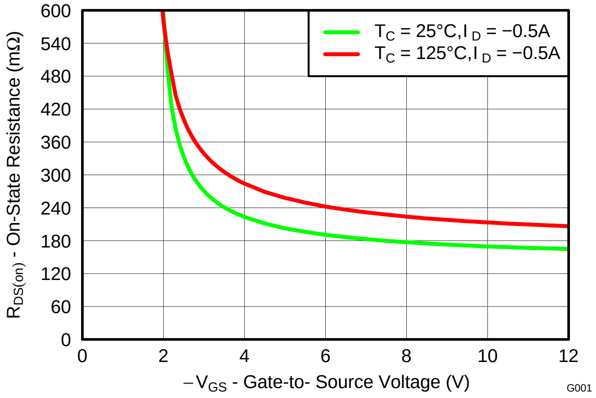


Figure 7. On-State Resistance vs Gate-to-Source Voltage

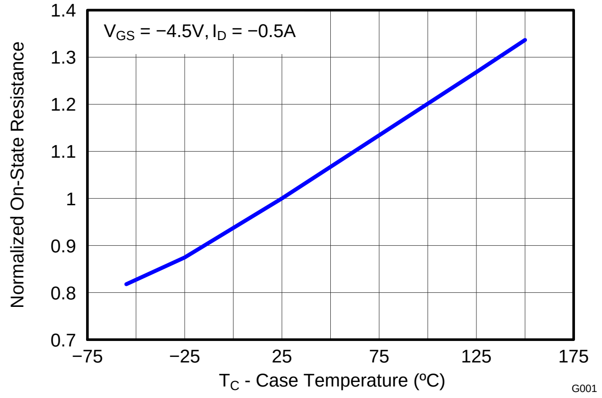


Figure 8. Normalized On-State Resistance vs Temperature

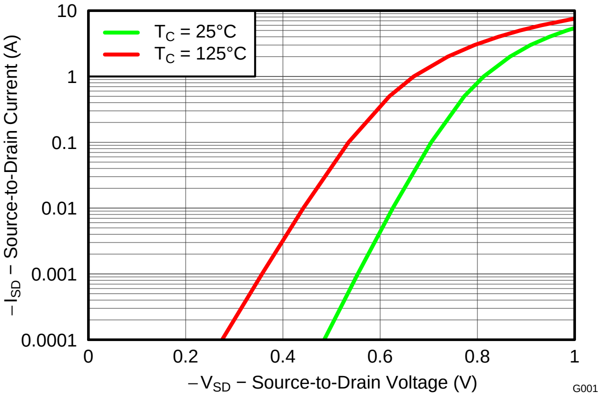


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

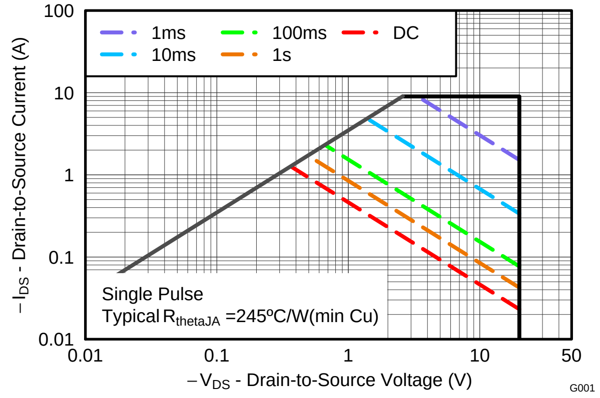


Figure 10. Maximum Safe Operating Area

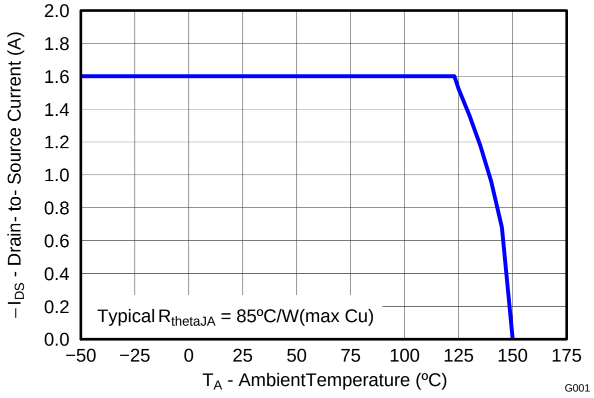


Figure 11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

FemtoFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

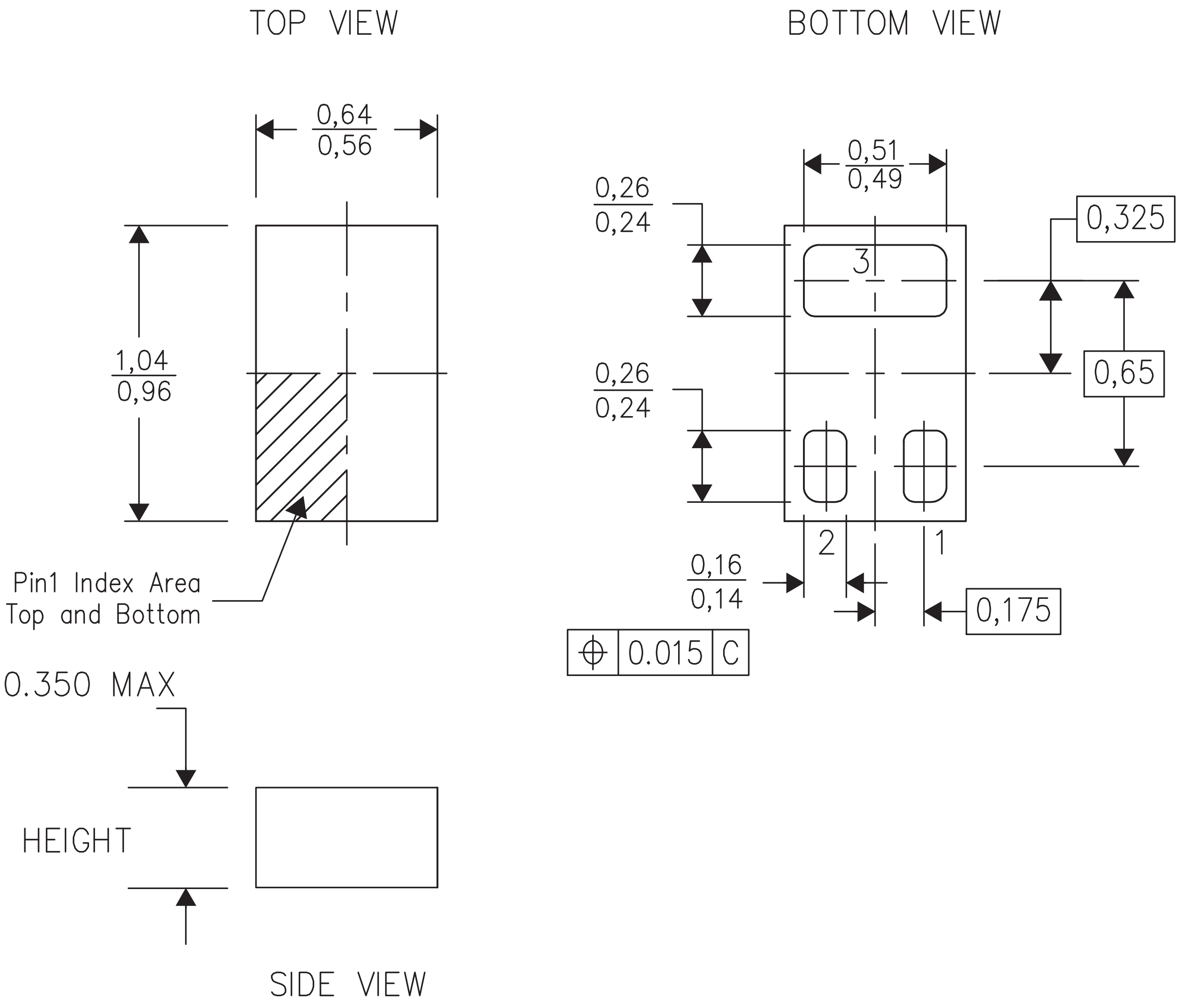
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical Data

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



(1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).

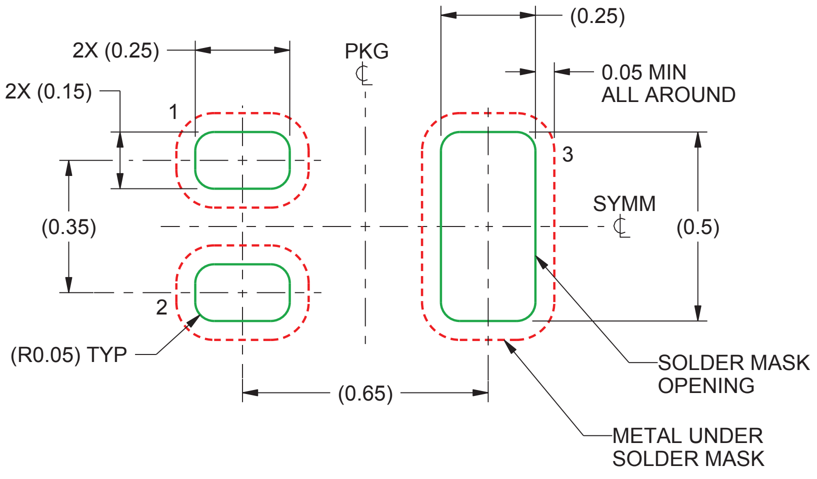
(2) This drawing is subject to change without notice.

(3) This package is a PB-free solder land design.

Pin Configuration

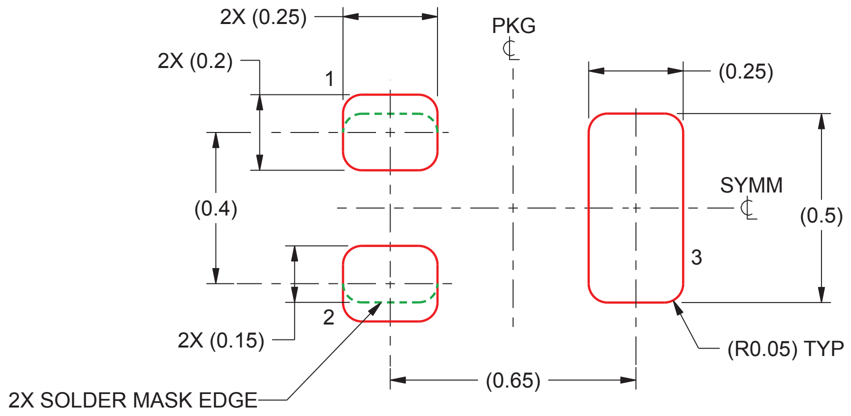
Position	Designation
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



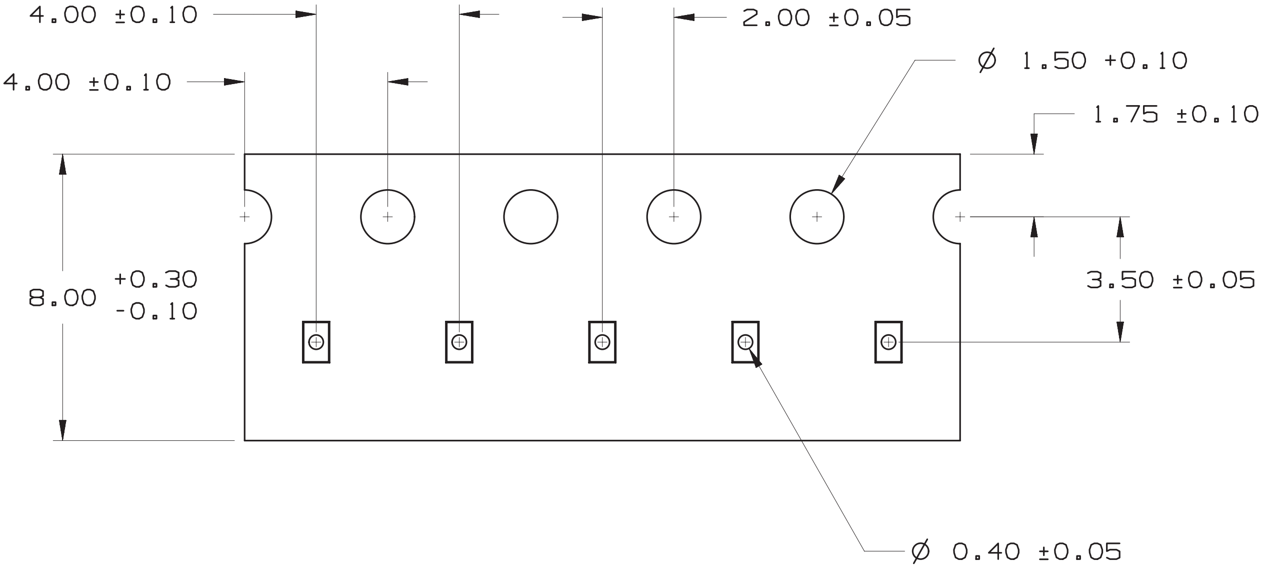
(1) All dimensions are in millimeters.

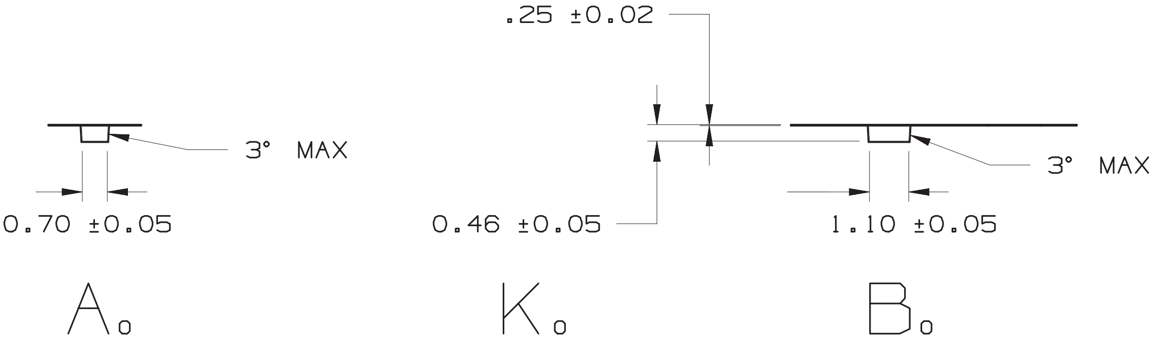
7.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

7.4 CSD25483F4 Embossed Carrier Tape Dimensions





(1) Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25483F4	ACTIVE	PICOSTAR	YJC	3	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-55 to 150	DR	Samples
CSD25483F4T	ACTIVE	PICOSTAR	YJC	3	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-55 to 150	DR	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

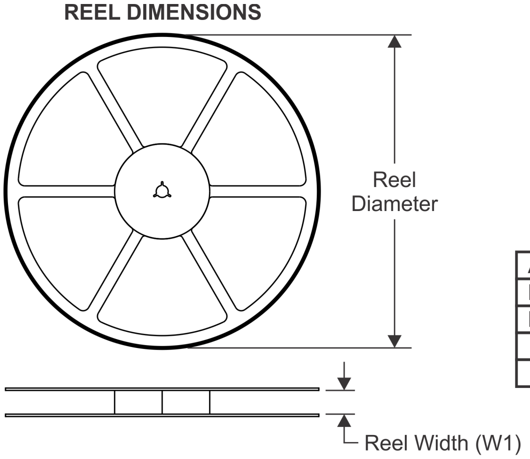
[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

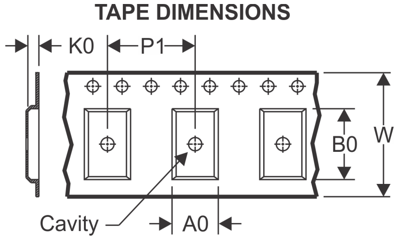
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

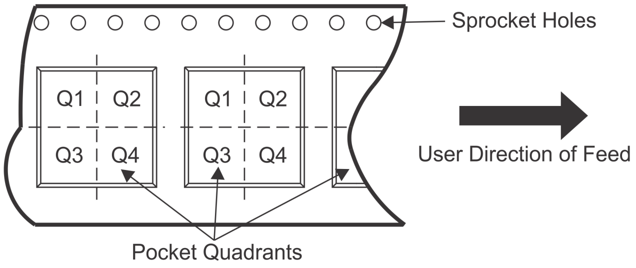
TAPE AND REEL INFORMATION


REEL DIMENSIONS


TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

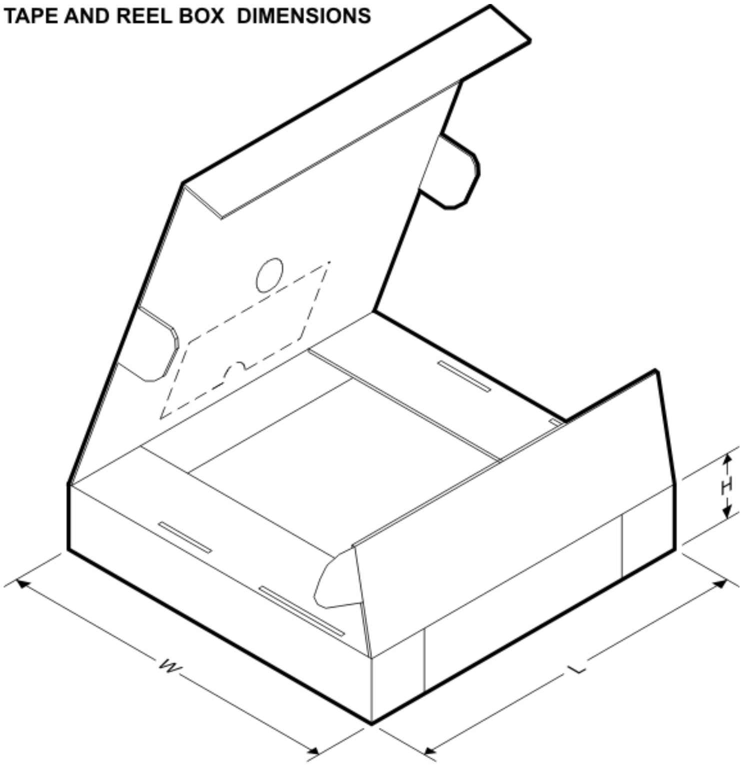
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25483F4	PICOSTAR	YJC	3	3000	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD25483F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD25483F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD25483F4T	PICOSTAR	YJC	3	250	178.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25483F4	PICOSTAR	YJC	3	3000	220.0	220.0	35.0
CSD25483F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD25483F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0
CSD25483F4T	PICOSTAR	YJC	3	250	220.0	220.0	35.0

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated