CSD25484F4 –20-V P-Channel FemtoFET™ MOSFET

1 Features

- Low On-Resistance
- Ultra-Low Q_g and Q_{gd}
- Low-Threshold Voltage
- Ultra-Small Footprint (0402 Case Size)
  - 1.0 mm × 0.6 mm
- Ultra-Low Profile
  - 0.2-mm Height
- Integrated ESD Protection Diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and Halogen Free
- RoHS Compliant

2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Battery Applications
- Handheld and Mobile Applications

3 Description

This 80-mΩ, –20-V, P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	1090		pC
Q_{gd}	Gate Charge Gate-to-Drain	150		pC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V	405	mΩ
		V_{GS} = –2.5 V	150	
		V_{GS} = –4.5 V	93	
		V_{GS} = –8.0 V	80	
$V_{GS(th)}$	Threshold Voltage	–0.95		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD25484F4	3000	7-Inch Reel	Femto (0402) 1.00-mm × 0.60-mm Land Grid Array (LGA)	Tape and Reel
CSD25484F4T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

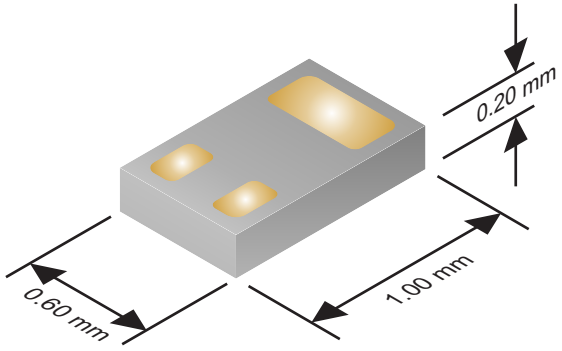
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–12	V
I_D	Continuous Drain Current(1)	–2.5	A
I_{DM}	Pulsed Drain Current(1)(2)	–22	A
I_G	Continuous Gate Clamp Current	–35	mA
	Pulsed Gate Clamp Current(2)	–350	
P_D	Power Dissipation(1)	500	mW
$V_{(ESD)}$	Human-Body Model (HBM)	4	kV
	Charged-Device Model (CDM)	2	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C

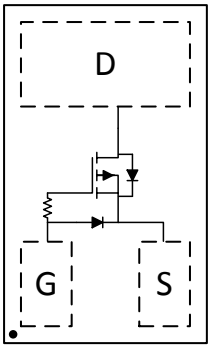
(1) Typical $R_{\theta JA}$ = 85°C/W on 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤ 100 μs, duty cycle ≤ 1%.

Typical Part Dimensions



Top View



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4 Revision History

Changes from Original (May 2015) to Revision A **Page**

- Added the *Receiving Notification of Documentation Updates* and the *Community Resources* sections to *Device and Documentation Support* ... 7
- Updated the *Recommended Minimum PCB Layout* and the *Recommended Stencil Pattern* sections ... 8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –16 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V			–50	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.7	–0.95	–1.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		405	825	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.5 A		150	180	
		V_{GS} = –4.5 V, I_{DS} = –0.5 A		93	109	
		V_{GS} = –8 V, I_{DS} = –0.5 A		80	94	
g_{fs}	Transconductance	V_{DS} = –10 V, I_{DS} = –0.5 A		3.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		175	230	pF
C_{oss}	Output capacitance			78	102	pF
C_{rss}	Reverse transfer capacitance			5.5	7.2	pF
R_G	Series gate resistance			20		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –0.5 A		1090	1415	pC
Q_{gd}	Gate charge gate-to-drain			150		pC
Q_{gs}	Gate charge gate-to-source			350		pC
$Q_{g(th)}$	Gate charge at V_{th}			210		pC
Q_{oss}	Output charge	V_{DS} = –10 V, V_{GS} = 0 V		1290		pC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.5 A, R_G = 10 Ω		9.5		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turnoff delay time			18		ns
t_f	Fall Time			8.5		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.5 A, V_{GS} = 0 V		–0.75		V
Q_{rr}	Reverse recovery charge	V_{DS}= –10 V, I_F = –0.5 A, di/dt = 100 A/µs		970		pC
t_{rr}	Reverse recovery time			7.5		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	85	°C/W
	Junction-to-ambient thermal resistance(2)	245	

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

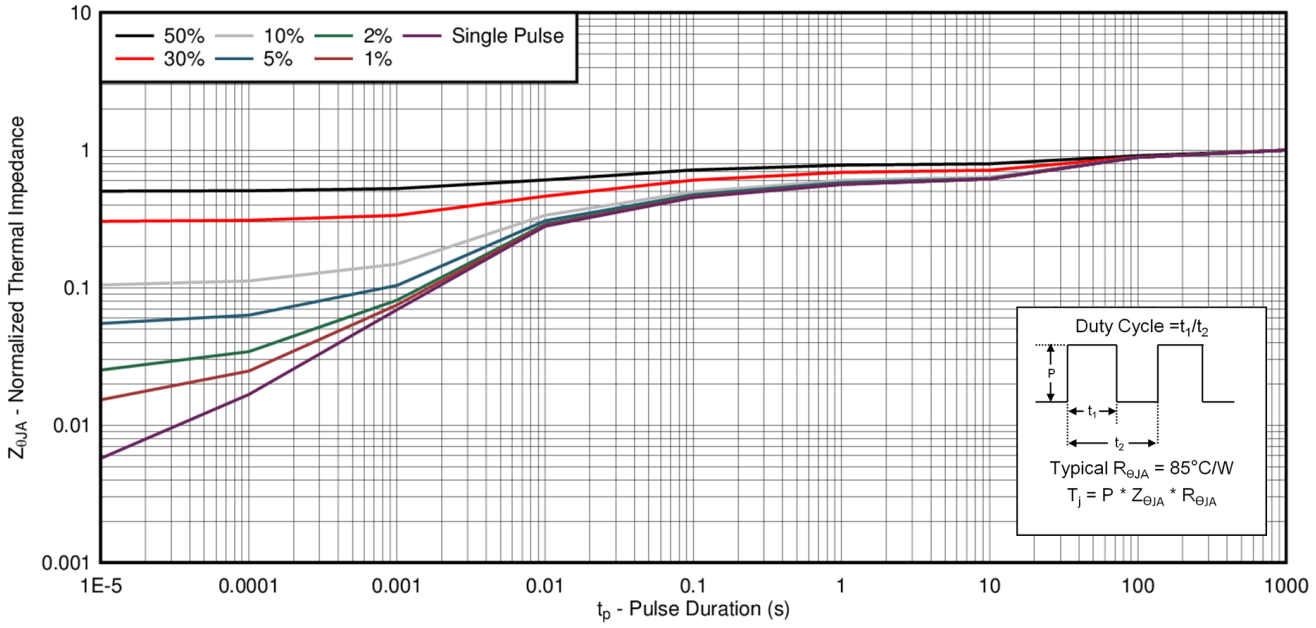


Figure 1. Transient Thermal Impedance

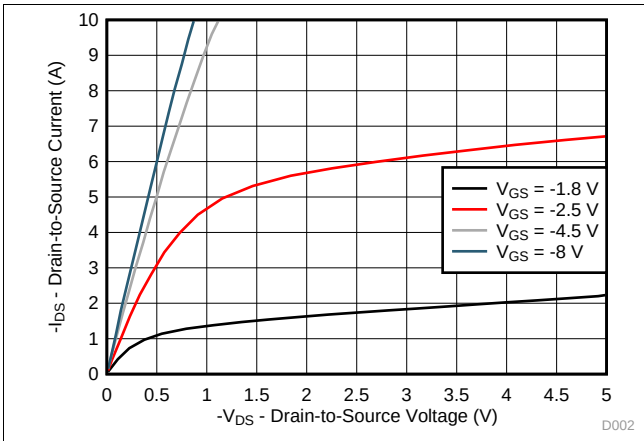


Figure 2. Saturation Characteristics

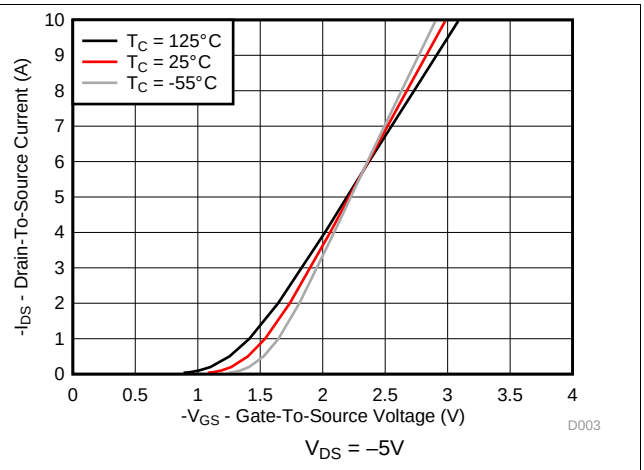


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

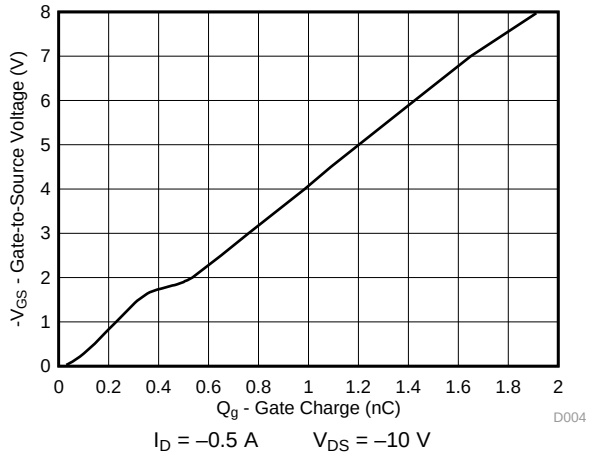


Figure 4. Gate Charge

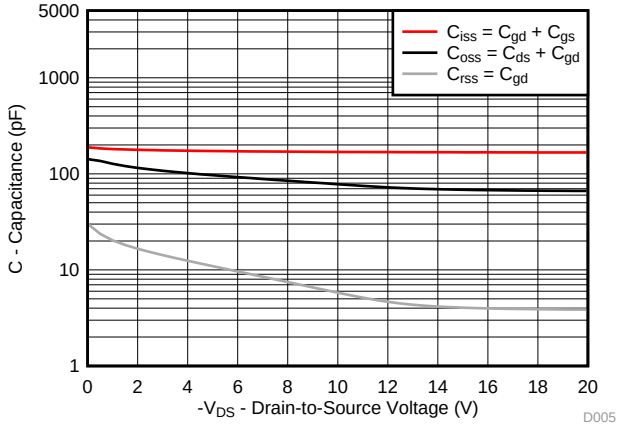


Figure 5. Capacitance

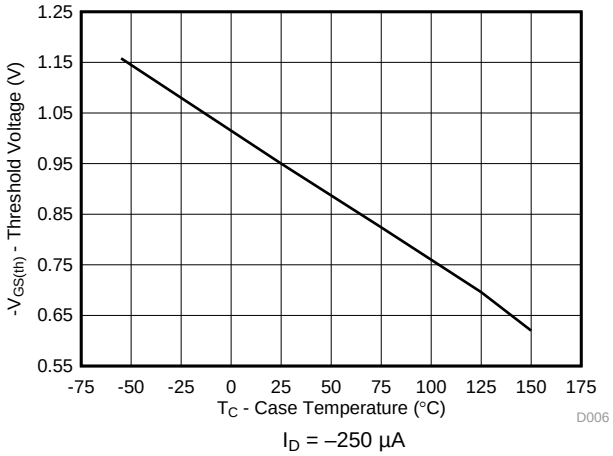


Figure 6. Threshold Voltage vs Temperature

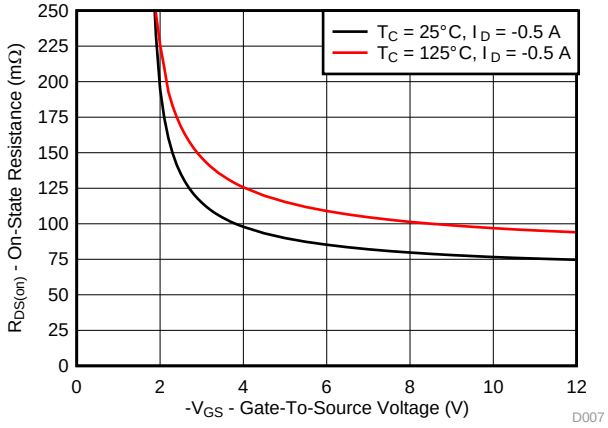


Figure 7. On-State Resistance vs Gate-to-Source Voltage

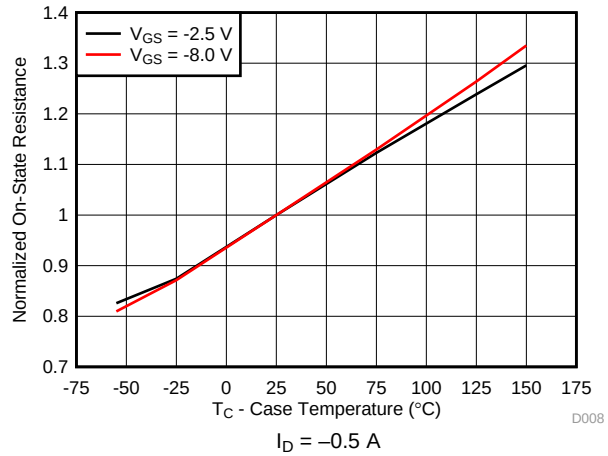


Figure 8. Normalized On-State Resistance vs Temperature

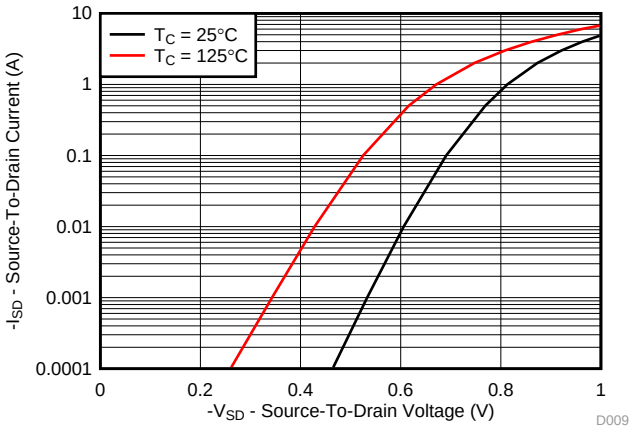


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

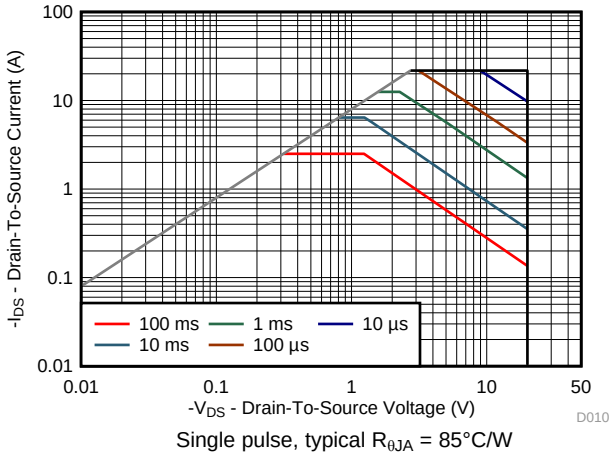


Figure 10. Maximum Safe Operating Area

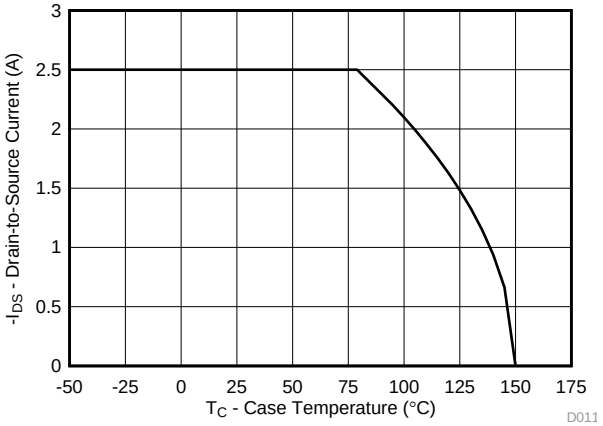


Figure 11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

FemtoFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

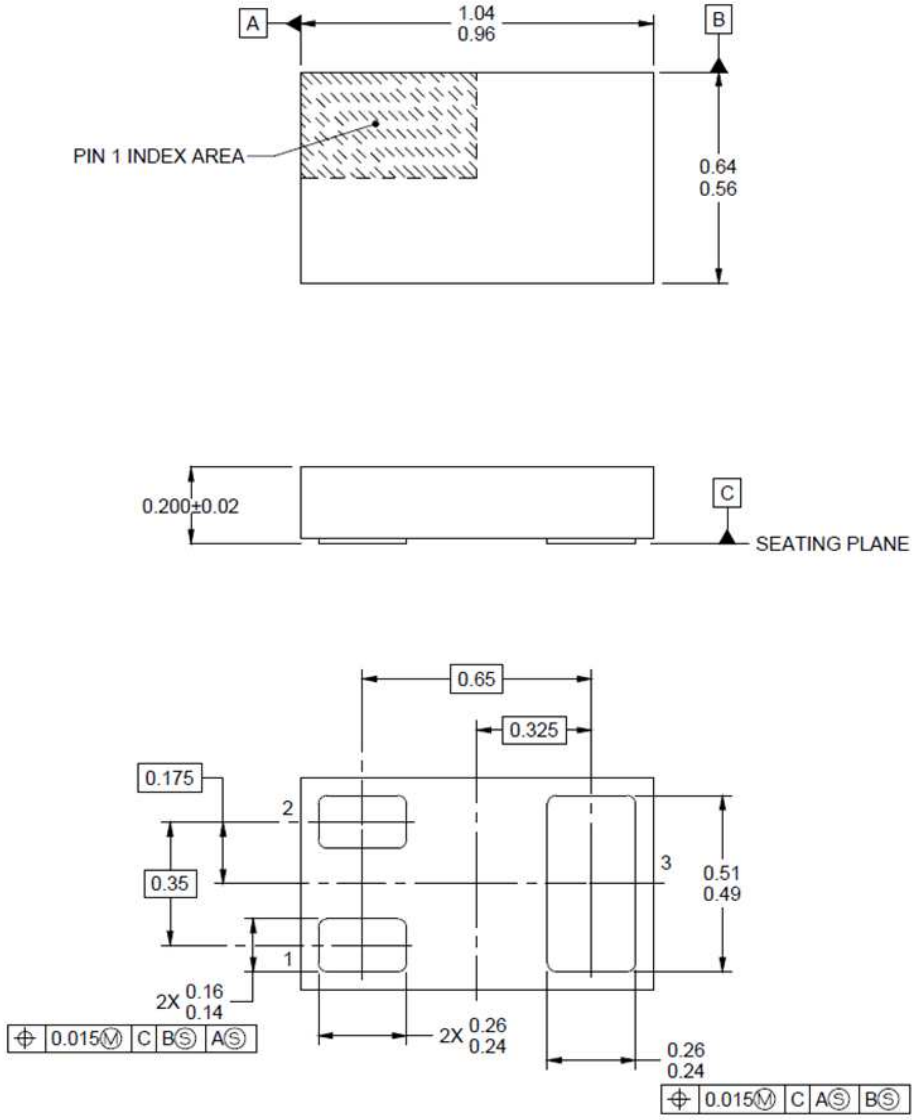
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



(1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).

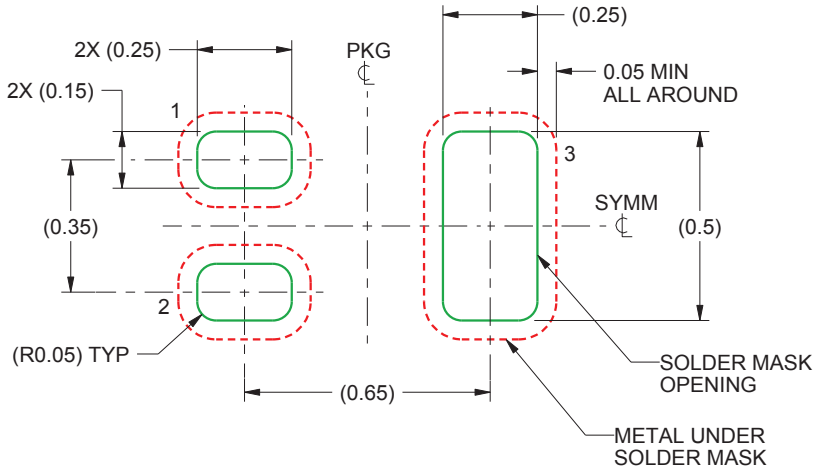
(2) This drawing is subject to change without notice.

(3) This package is a PB-free solder land design.

Table 1. Pin Configuration

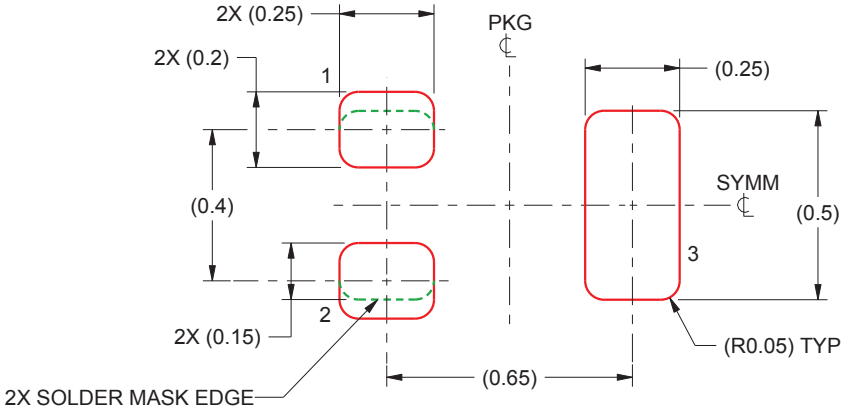
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



(1) All dimensions are in millimeters.

7.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25484F4	ACTIVE	PICOSTAR	YJJ	3	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-55 to 150	G3	Samples
CSD25484F4T	ACTIVE	PICOSTAR	YJJ	3	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-55 to 150	G3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

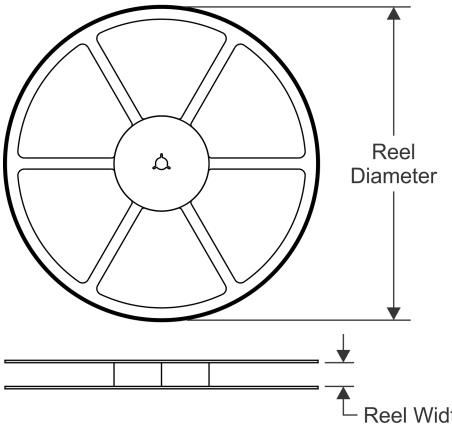
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

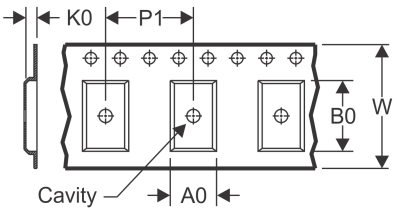
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

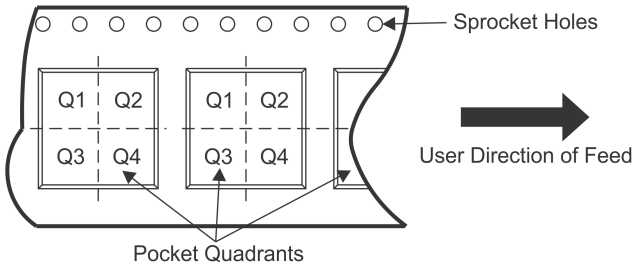


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

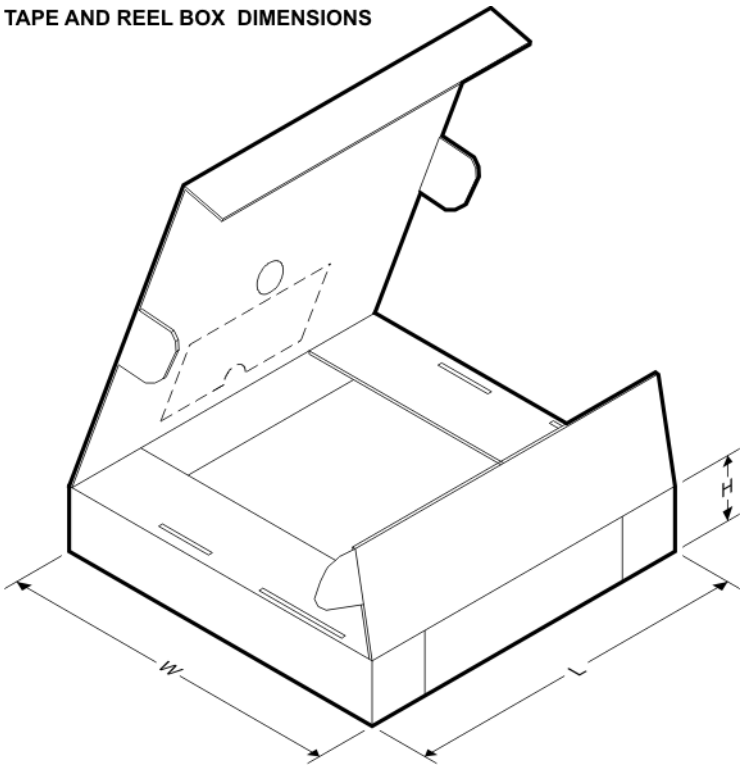
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25484F4	PICOSTAR	YJJ	3	3000	178.0	9.2	0.7	1.1	0.28	4.0	8.0	Q2
CSD25484F4T	PICOSTAR	YJJ	3	250	178.0	9.2	0.7	1.1	0.28	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25484F4	PICOSTAR	YJJ	3	3000	220.0	220.0	35.0
CSD25484F4T	PICOSTAR	YJJ	3	250	220.0	220.0	35.0

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265