

N-Channel Trench Power MOSFET

General Description

The CSD40N160 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a wide variety of applications.

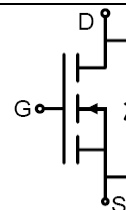
Features

- $V_{DS} = 40V, I_D = 30A$
 $R_{DS(ON)} < 20m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 34m\Omega @ V_{GS} = 4.5V$
- High Power and current handling capability
- Lead free product is acquired
- Surface Mount Package

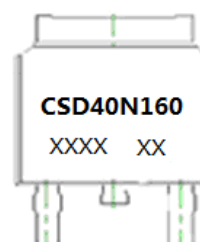
Application

- PWM applications
- Load switch
- Power management

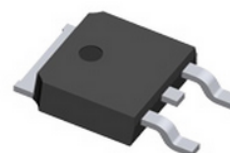
100% UIS TESTED!
100% ΔV_{ds} TESTED!



Schematic Diagram



Marking and pin Assignment



TO-252(DPAK) top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
CSD40N160	CSD40N160	TO-252	325mm	16mm	2500

Table 1. Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS} = 0V$)	40	V
V_{GS}	Gate-Source Voltage ($V_{DS} = 0V$)	± 20	V
I_D	Drain Current-Continuous ($T_C = 25^\circ\text{C}$)	30	A
	Drain Current-Continuous ($T_C = 100^\circ\text{C}$)	21	A
$I_{DM (pulse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	120	A
P_D	Maximum Power Dissipation ($T_C = 25^\circ\text{C}$)	38	W
	Maximum Power Dissipation ($T_C = 100^\circ\text{C}$)	19	W
E_{AS}	Avalanche energy (Note 2)	100	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ\text{C}$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	4	$^\circ\text{C/W}$

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

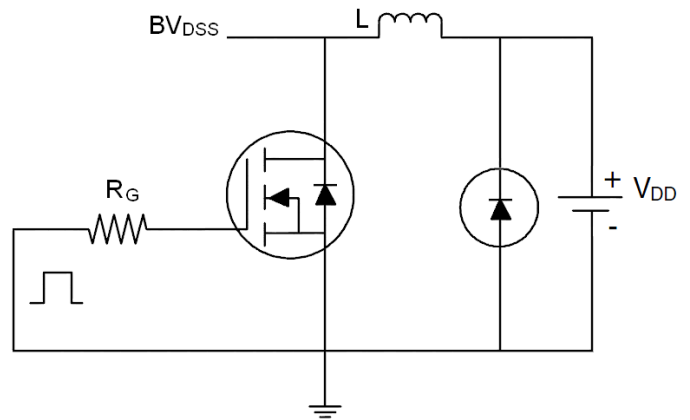
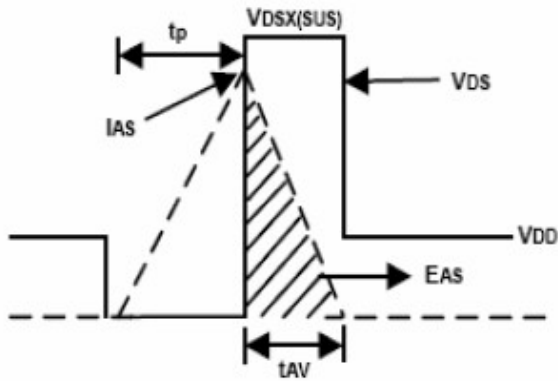
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	2	3	V
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =10A		18		S
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =20A		14	20	mΩ
		V _{GS} =4.5V, I _D =15A		24	34	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		840		pF
C _{oss}	Output Capacitance			92		pF
C _{rss}	Reverse Transfer Capacitance			60		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1.0MHz		2.7		Ω
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		5		nS
t _r	Turn-on Rise Time			12		nS
t _{d(off)}	Turn-Off Delay Time			20		nS
t _f	Turn-Off Fall Time			4.5		nS
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		20		nC
Q _{gs}	Gate-Source Charge			2.5		nC
Q _{gd}	Gate-Drain Charge			4.5		nC
Source-Drain Diode Characteristics						
I _{SD}	Source-Drain Current(Body Diode)				30	A
V _{SD}	Forward on Voltage	V _{GS} =0V, I _S =20A			1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=100A/μs		7		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=100A/μs		5		nC

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

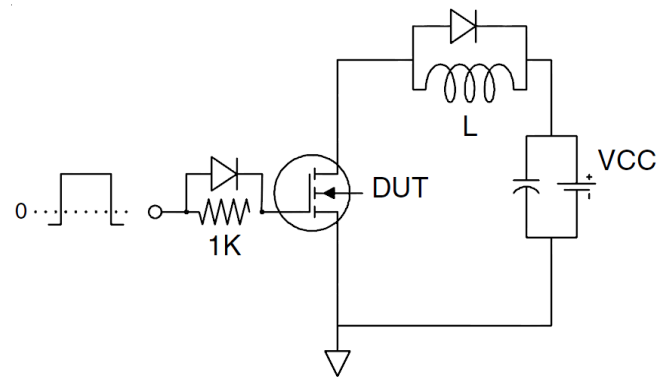
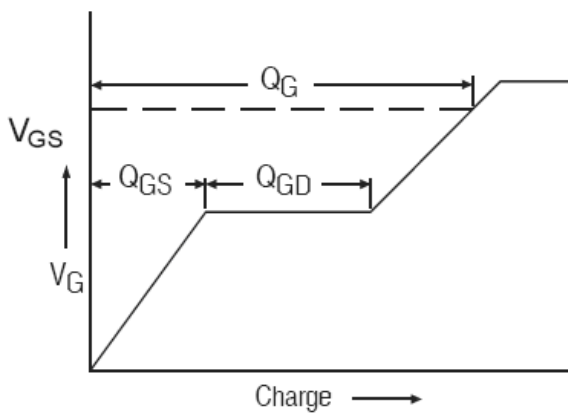
Notes 2.EAS condition: T_J=25°C, V_{DD}=15V, V_G=10V, R_G=25Ω

Test Circuit

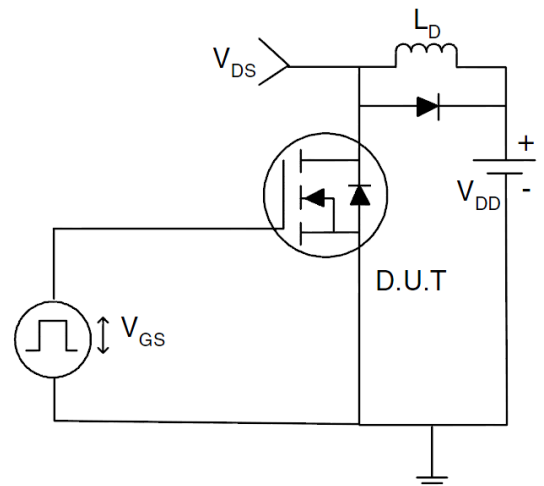
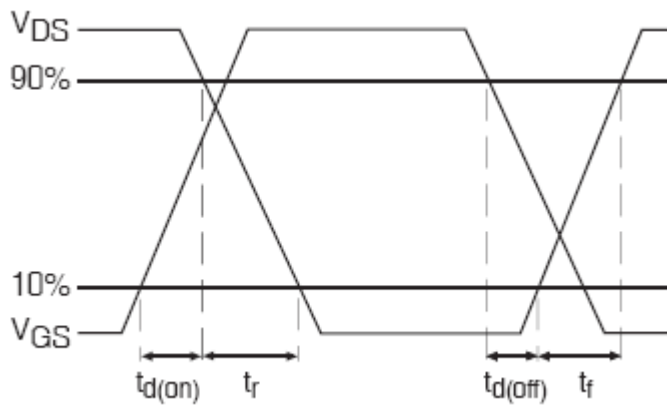
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure 1. Output Characteristics

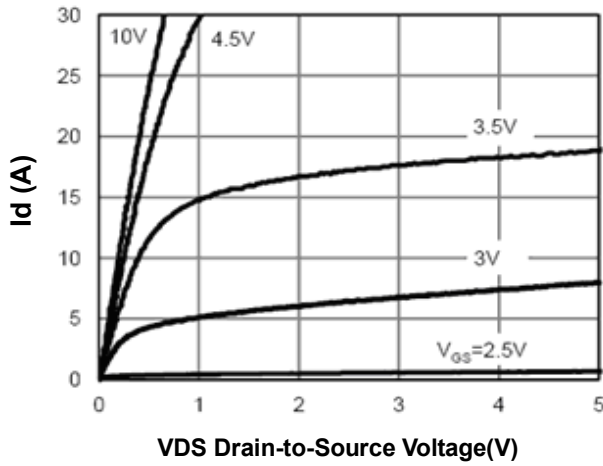


Figure 2. Transfer Characteristics

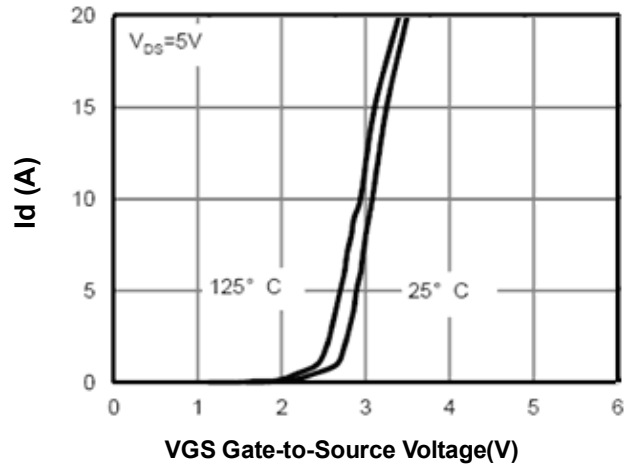


Figure 3. Max BV_{DSS} vs Junction Temperature

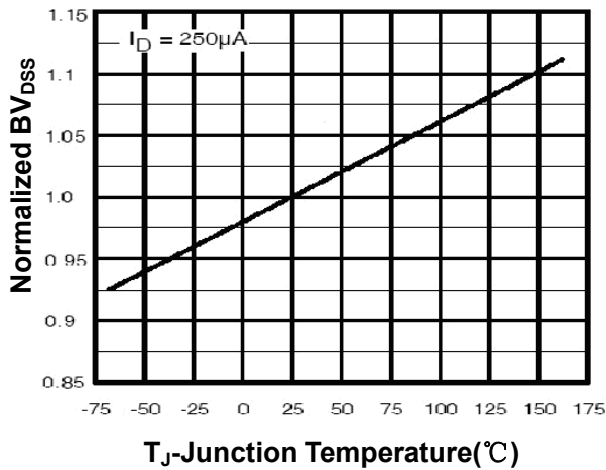


Figure 4. Drain Current

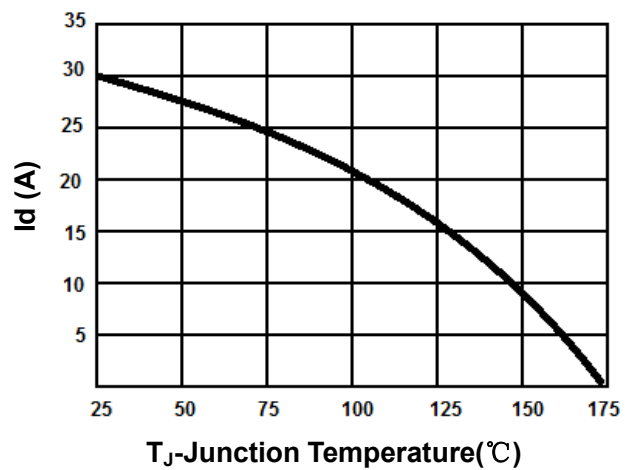


Figure 5. $V_{GS(th)}$ vs Junction Temperature

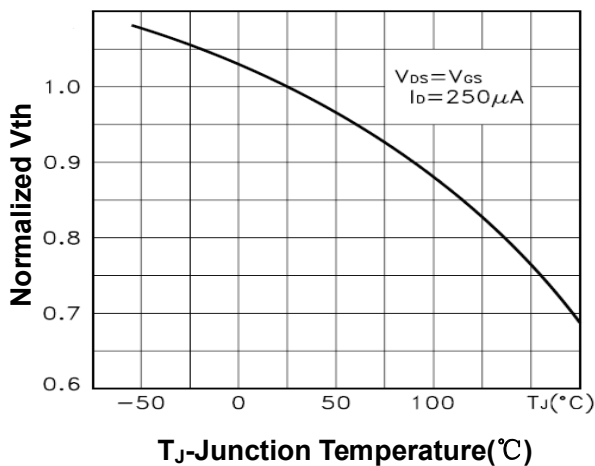


Figure 6. $R_{DS(on)}$ vs Junction Temperature

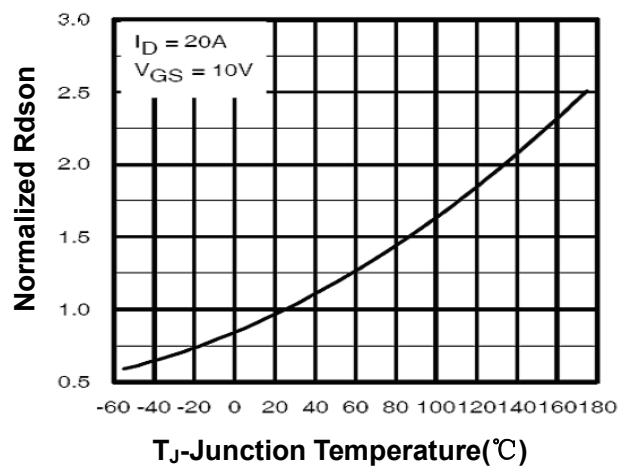


Figure 7. Gate Charge Waveforms

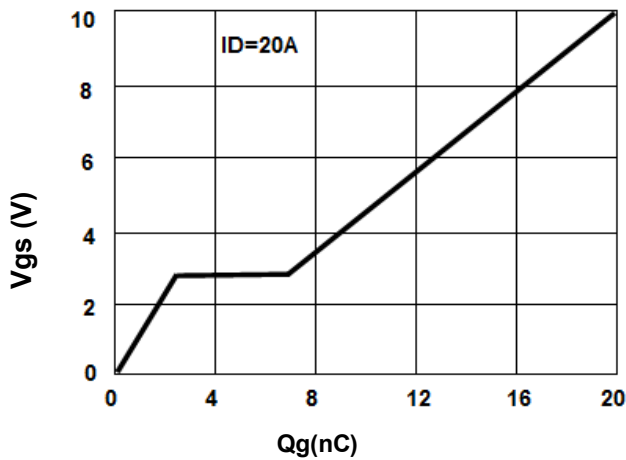


Figure 8. Capacitance

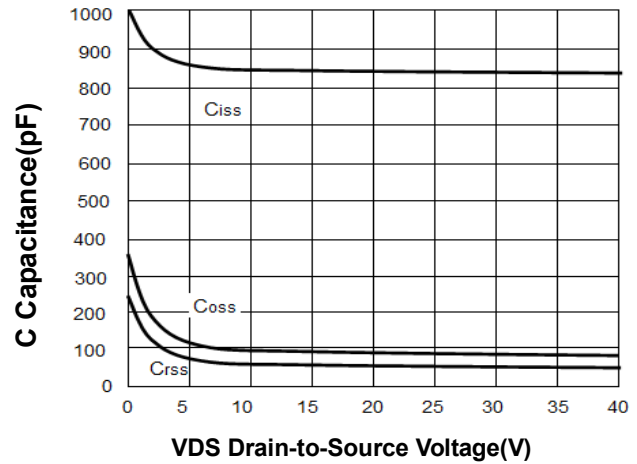


Figure 9. Body-Diode Characteristics

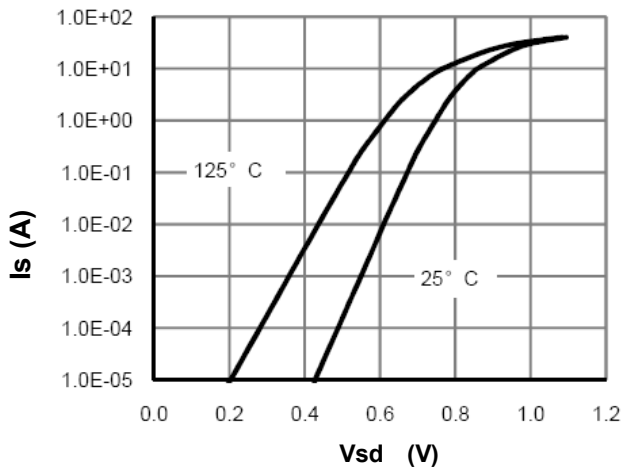


Figure 10. Maximum Safe Operating Area

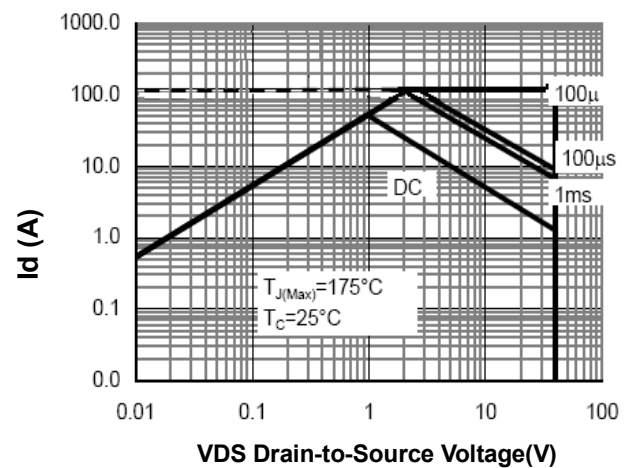
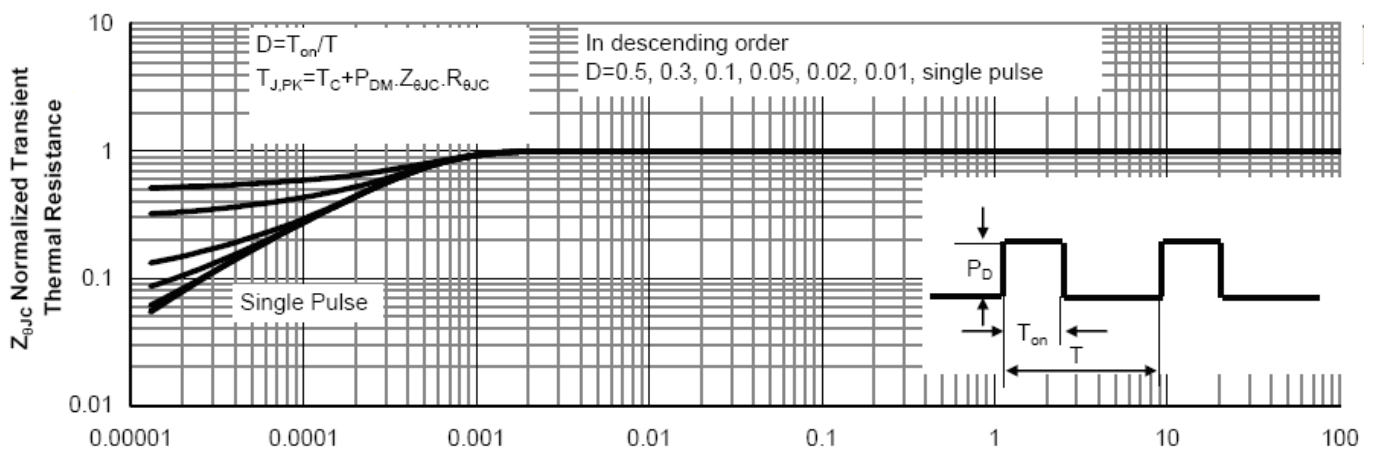
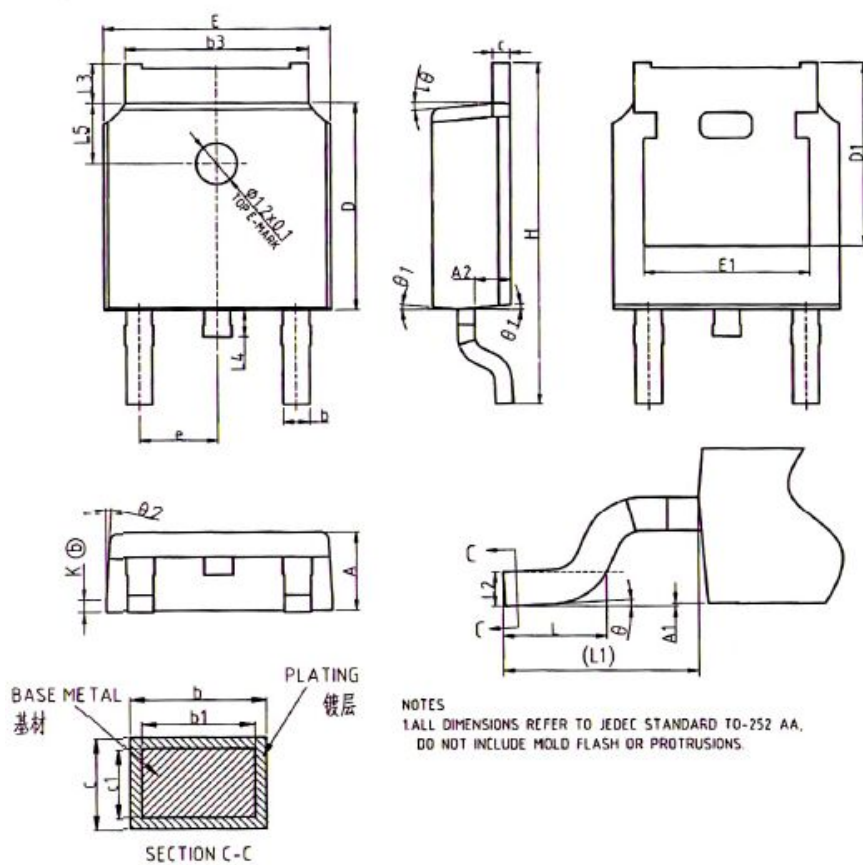


Figure 11. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



NOTES
 1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AA.
 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

COMMON DIMENSIONS			
SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
θ	0°	-	8°
θ_1	5°	7°	9°
θ_2	5°	7°	9°
K	0.40REF		