

N-Channel Trench Power MOSFET

General Description

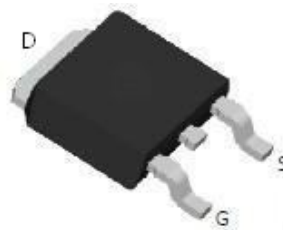
The CSD50N06 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. Those devices are suitable for use in PWM, load switching and general purpose applications.

Features

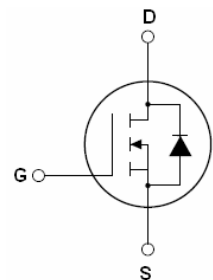
- $V_{DS}=60V$; $I_D=45A$
 $R_{DS(ON)} < 15m\Omega$ @ $V_{GS}=10V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Power switching application
- load switching



To-252 Top View



Schematic Diagram

$$V_{DS} = 60V$$

$$I_D = 45A$$

$$R_{DS(ON)} = 11.5m\Omega$$

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
CSD50N06	CSD50N06	TO-252	-	-	-

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	60	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 25	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	45	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	31	A
$I_{DM(pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	180	A
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	68	W
E_{AS}	Single Pulse Avalanche Energy (Note 2)	196	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, V_{DD}=30V, V_G=10V, R_G=25\Omega$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	---	2.2	$^{\circ}C/W$

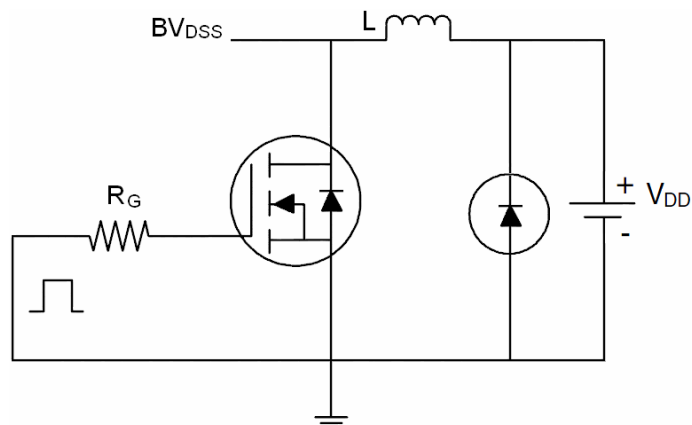
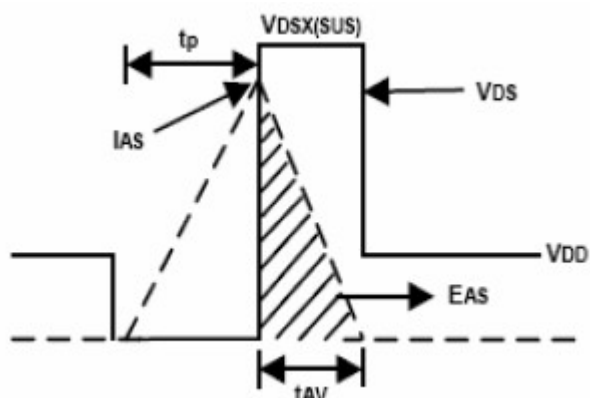
Table 3. Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	60			V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V _{DS} =60V,V _{GS} =0V			1	μA
I _{DSS}	Zero Gate Voltage Drain Current(Tc=100℃)	V _{DS} =60V,V _{GS} =0V			5	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±25V,V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	2		4	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =40A		11.5	15	mΩ
Dynamic Characteristics						
g _{FS}	Forward Transconductance	V _{DS} =10V,I _D =15A	18			S
C _{iss}	Input Capacitance	V _{DS} =25V,V _{GS} =0V f=1.0MHz		1659		PF
C _{oss}	Output Capacitance			180		PF
C _{rss}	Reverse Transfer Capacitance			128		PF
Q _g	Total Gate Charge	V _{DS} =30V,I _D =15A V _{GS} =10V		50		nC
Q _{gs}	Gate-Source Charge			12		nC
Q _{gd}	Gate-Drain Charge			23		nC
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{DS} =30V,R _L =2.5Ω V _{GS} =10V,R _G =3Ω		15		nS
t _r	Turn-on Rise Time			25		nS
t _{d(off)}	Turn-Off Delay Time			53		nS
t _f	Turn-Off Fall Time			23		nS
Source-Drain Diode Characteristics						
I _{SD}	Source-Drain Current(Body Diode)			45		A
I _{SDM}	Pulsed Source-Drain Current(Body Diode)			180		A
V _{SD}	Forward On Voltage ^(Note 1)	T _J =25℃,I _{SD} =1A,V _{GS} =0V		0.89	0.99	V
t _{rr}	Reverse Recovery Time ^(Note 1)	T _J =25℃,I _F =15A di/dt=100A/μs		24		nS
Q _{rr}	Reverse Recovery Charge ^(Note 1)			30		nC
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

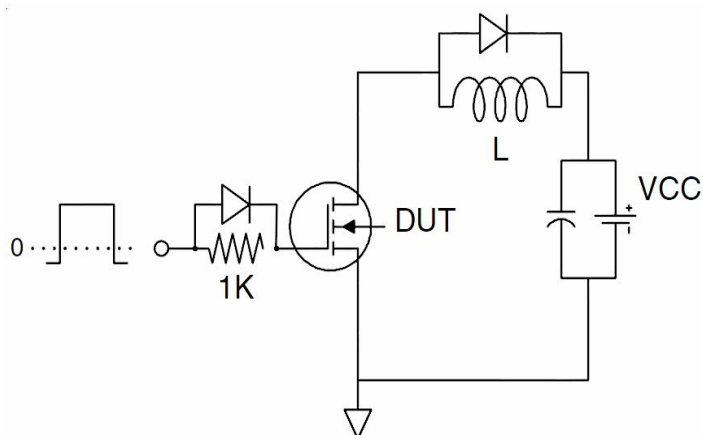
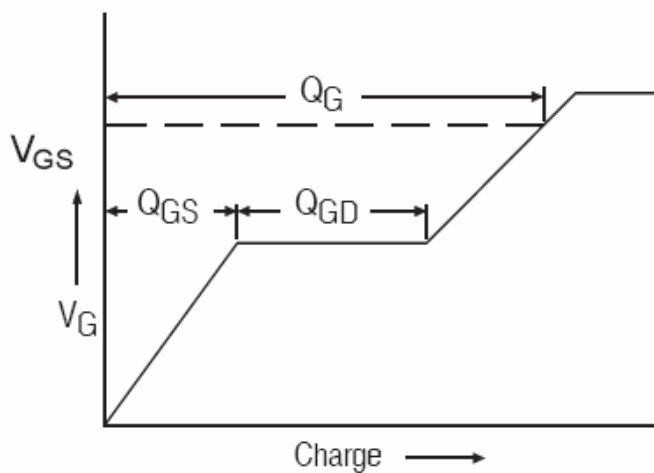
Notes 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1.5\%$, Starting $T_J=25^{\circ}C$

Test Circuit

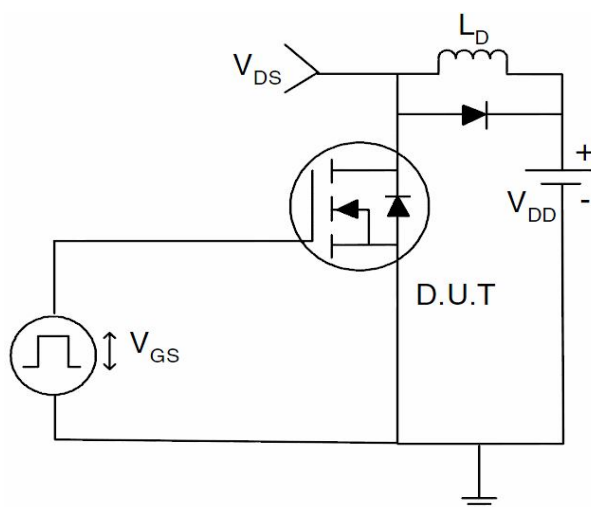
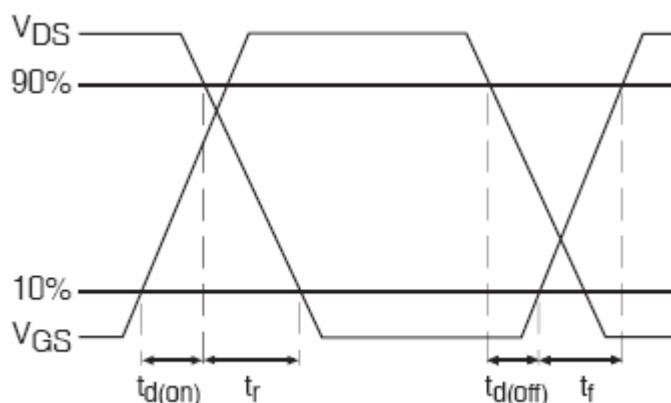
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

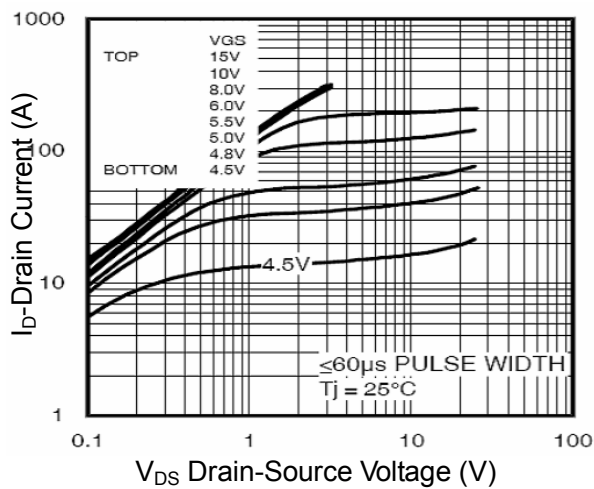


Figure2. Transfer Characteristics

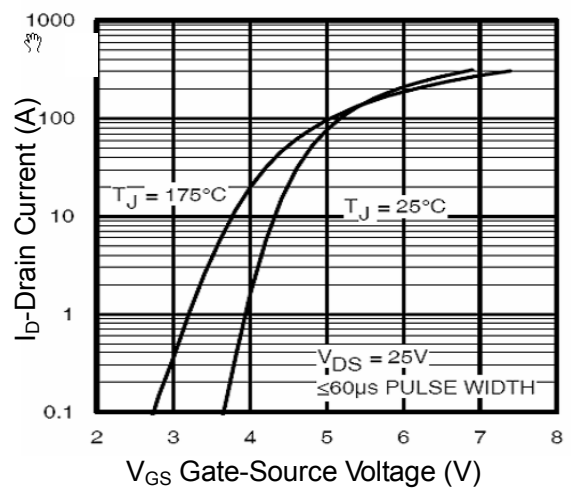


Figure3. BVDSS vs Junction Temperature

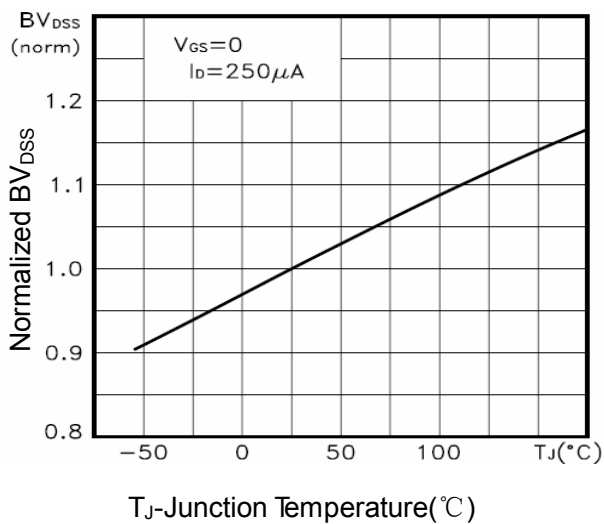


Figure4. ID vs Junction Temperature

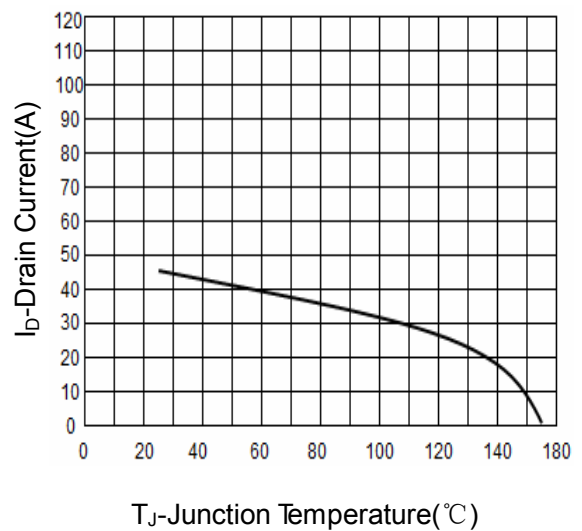


Figure5. VGS(th) vs Junction Temperature

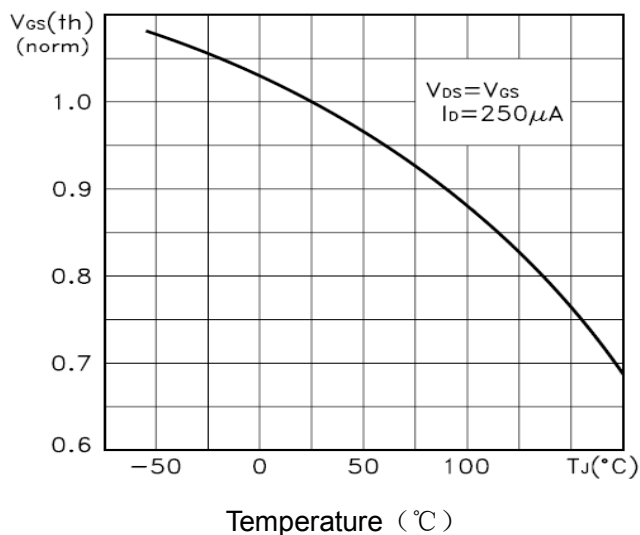


Figure6. Rds(on) Vs Junction Temperature

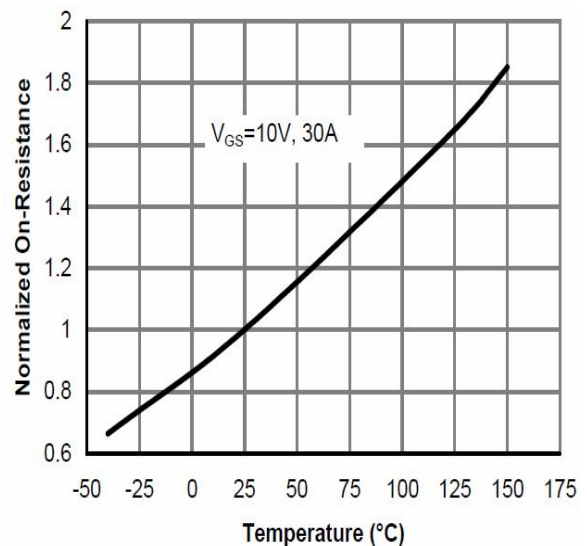


Figure7. Gate Charge

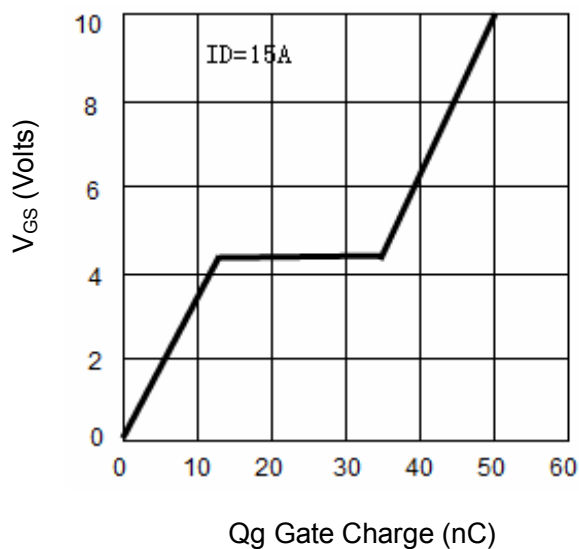


Figure8. Capacitance vs Vds

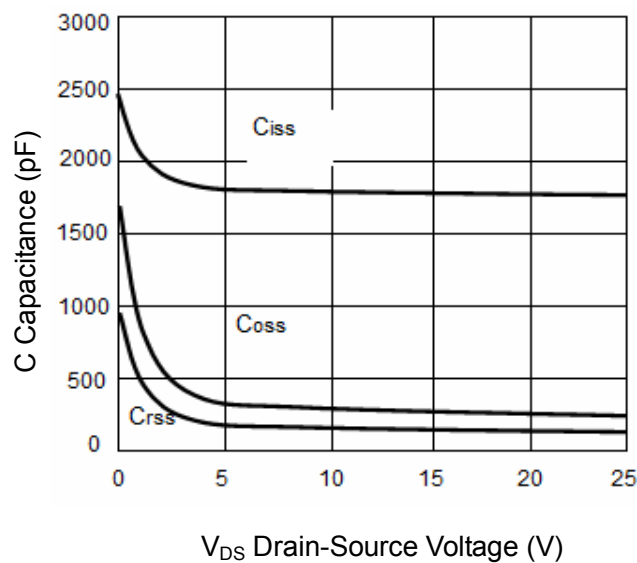


Figure9. Source- Drain Diode Forward

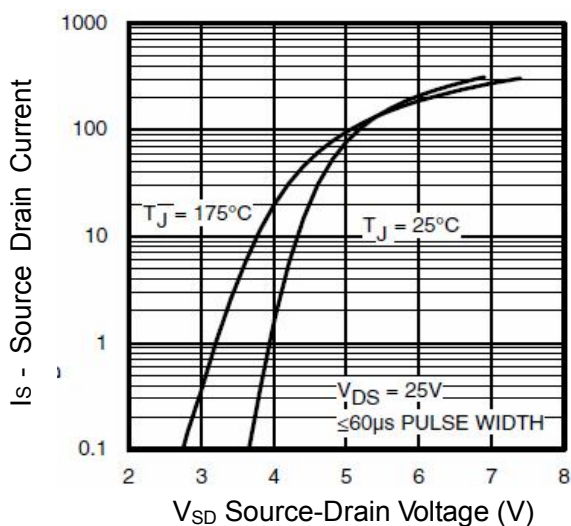


Figure10. Safe Operation Area

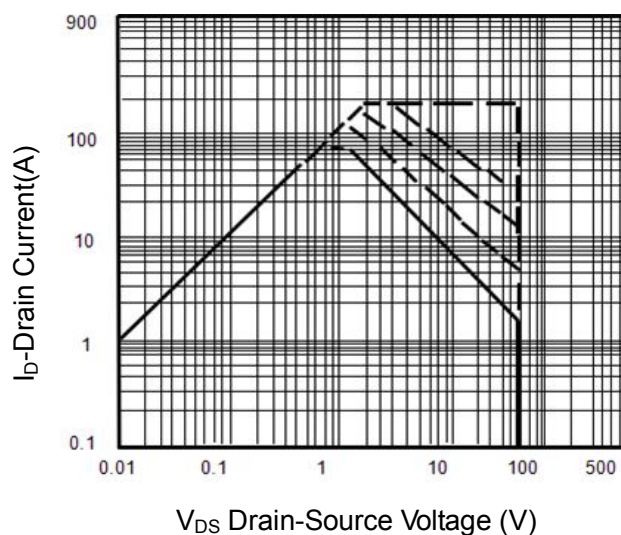
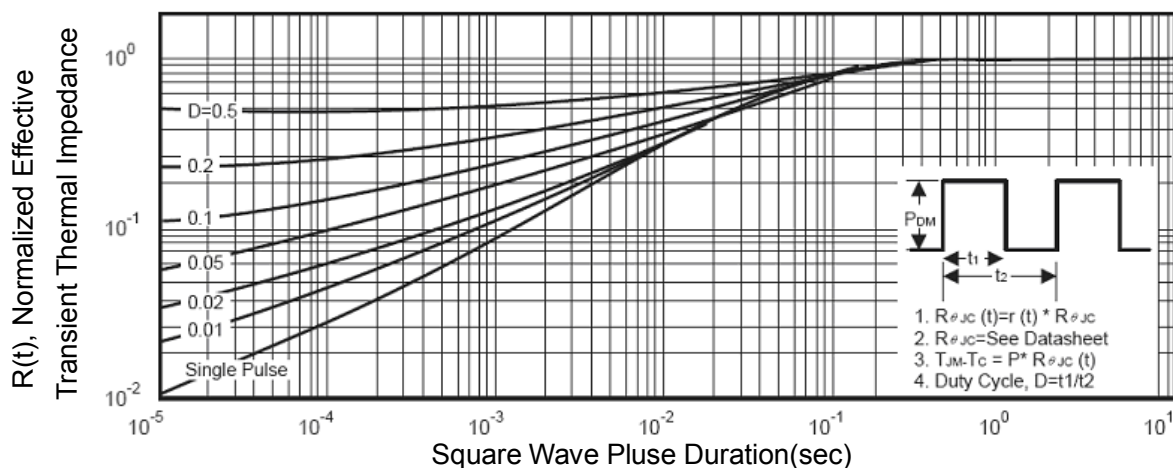
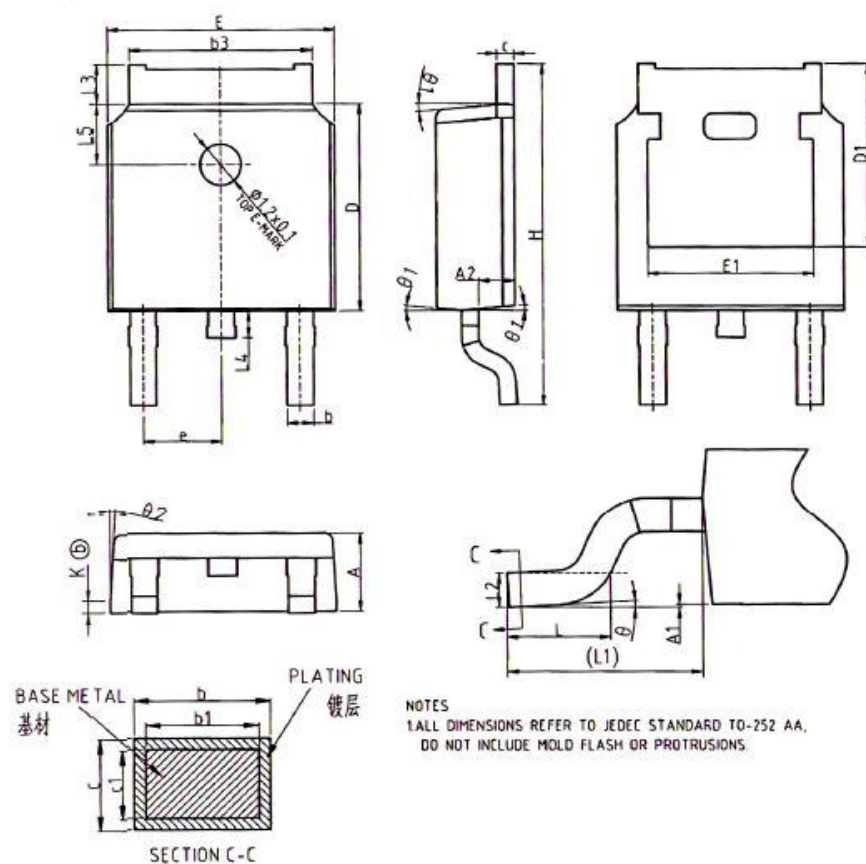


Figure11. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



COMMON DIMENSIONS			
SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
$\theta 1$	0°	-	8°
$\theta 2$	5°	7°	9°
K	0.40REF		