N-Channel Trench Power MOSFET

General Description

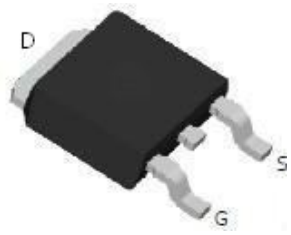
The CSD60N100 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. Those devices are suitable for use in PWM, load switching and general purpose applications.

Features

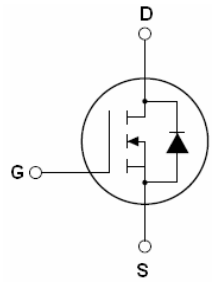
- V_{DS}=60V; I_D=45A
  $R_{DS(ON)}$<15mΩ @ V_{GS}=10V
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Power switching application
- load switching



To-252 Top View



Schematic Diagram

V_{DS} =60V

I_D = 45A

$R_{DS(ON)}$= 11mΩ

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
CSD60N100	CSD60N100	TO-252	-	-	-

Table 1. Absolute Maximum Ratings (TA=25℃)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS}=0V)	60	V
V_{GS}	Gate-Source Voltage (V_{DS}=0V)	±20	V
$I_{D\ (DC)}$	Drain Current (DC) at Tc=25℃	45	A
$I_{D\ (DC)}$	Drain Current (DC) at Tc=100℃	31	A
$I_{DM\ (pluse)}$	Drain Current-Continuous@ Current-Pulsed **(Note 1)**	180	A
P_D	Maximum Power Dissipation(Tc=25℃)	68	W
E_{AS}	Single Pulse Avalanche Energy **(Note 2)**	182	mJ
T_J,T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	℃

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.E_{AS} condition:T_J=25℃,V_{DD}=30V,V_G=10V, R_G=25Ω

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	---	2.2	℃/W

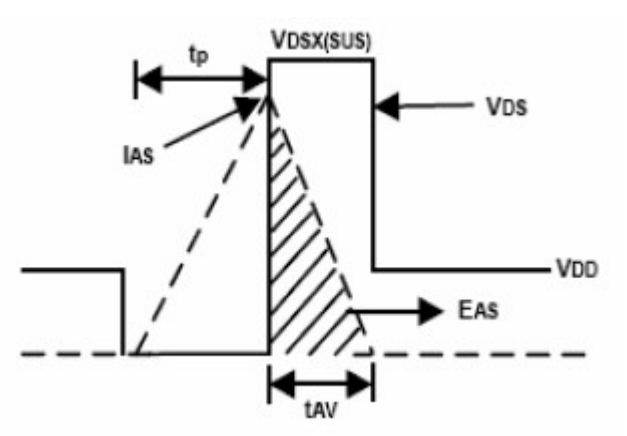
Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

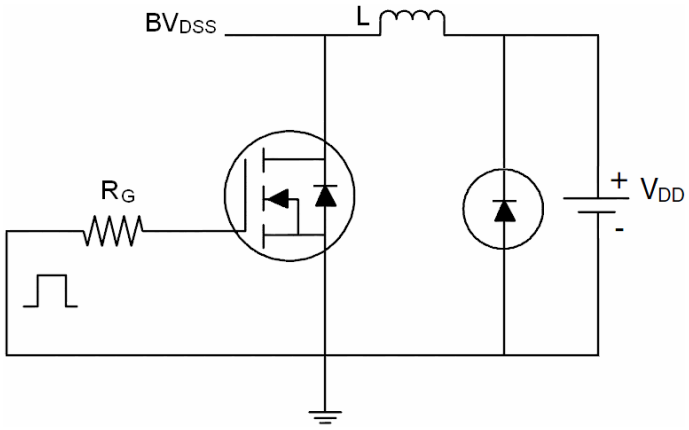
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	60			V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=60V,V_{GS}=0V			1	μA
I_{DSS}	Zero Gate Voltage Drain Current(Tc=100℃)	V_{DS}=60V,V_{GS}=0V			5	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1		3	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=40A		11	15	mΩ
Dynamic Characteristics						
g_{FS}	Forward Transconductance	V_{DS}=10V,I_D=15A	18			S
C_{iss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V f=1.0MHz		2489		PF
C_{oss}	Output Capacitance			276		PF
C_{rss}	Reverse Transfer Capacitance			128		PF
Q_g	Total Gate Charge	V_{DS}=30V,I_D=15A V_{GS}=10V		80		nC
Q_{gs}	Gate-Source Charge			19		nC
Q_{gd}	Gate-Drain Charge			37		nC
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=30V,R_L=2.5Ω V_{GS}=10V,R_G=3Ω		15		nS
t_r	Turn-on Rise Time			25		nS
$t_{d(off)}$	Turn-Off Delay Time			50		nS
t_f	Turn-Off Fall Time			23		nS
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current(Body Diode)			45		A
I_{SDM}	Pulsed Source-Drain Current(Body Diode)			180		A
V_{SD}	Forward On Voltage**(Note 1)**	T_J=25℃,I_{SD}=1A,V_{GS}=0V		0.74	0.99	V
t_{rr}	Reverse Recovery Time**(Note 1)**	T_J=25℃,I_F=15A di/dt=100A/μs		24		nS
Q_{rr}	Reverse Recovery Charge**(Note 1)**			30		nC
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

Notes 1.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, Starting T_J=25℃

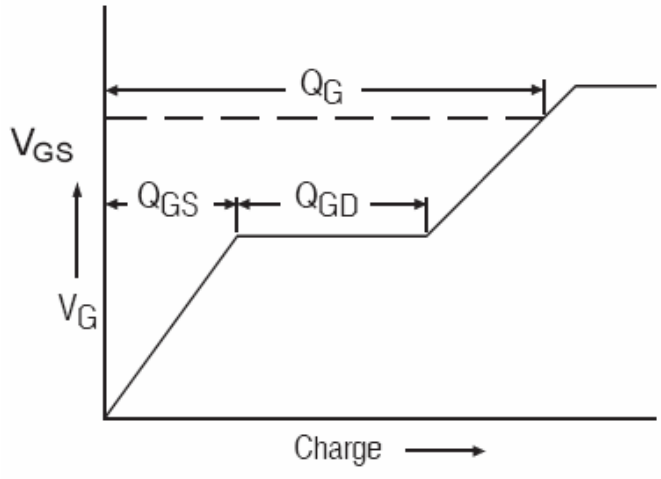
Test Circuit

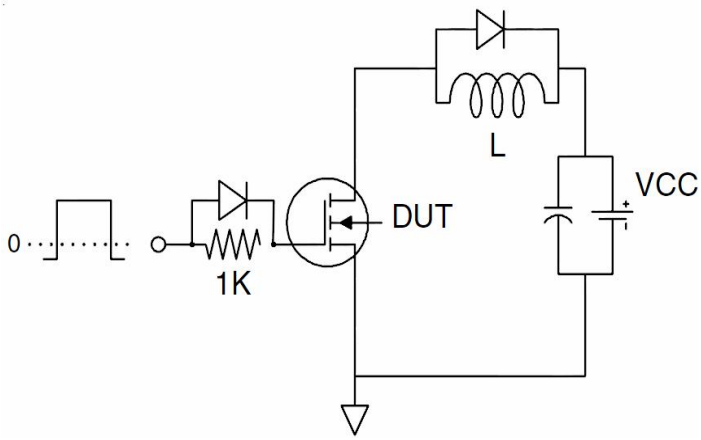
1) E_{AS} Test Circuits



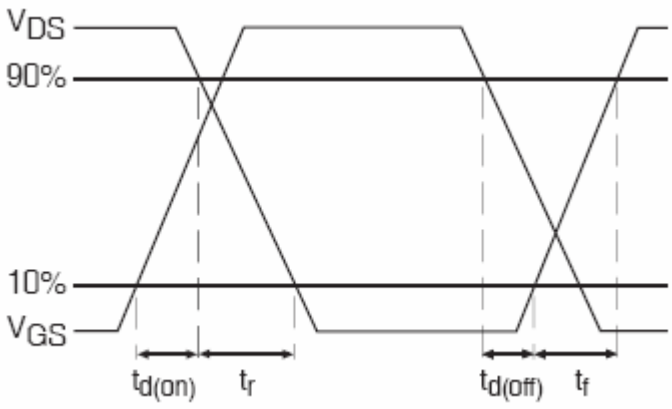


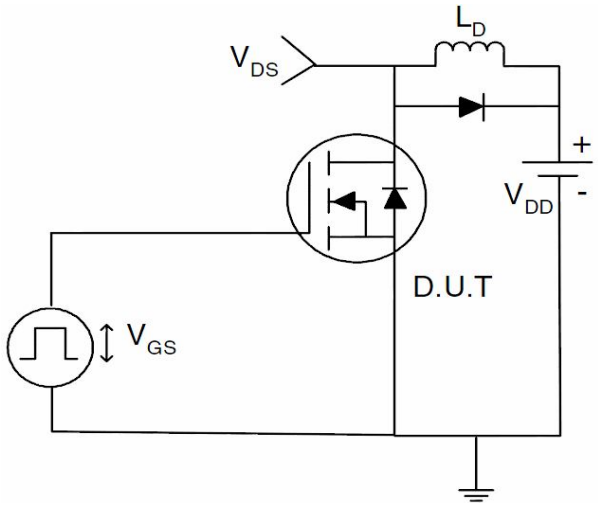
2) Gate Charge Test Circuit:





3) Switch Time Test Circuit:





TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

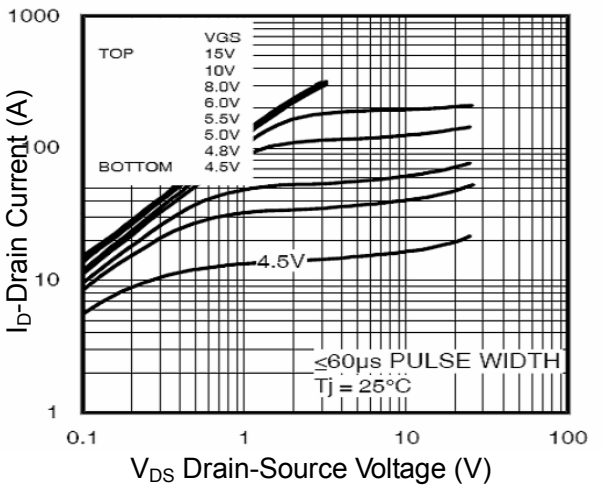


Figure2. Transfer Characteristics

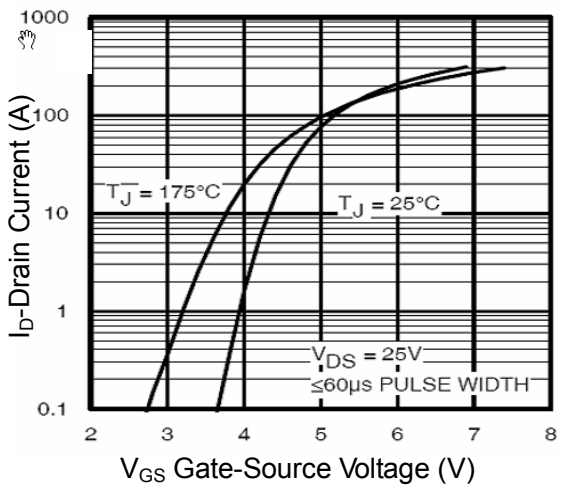


Figure3. BVDSS vs Junction Temperature

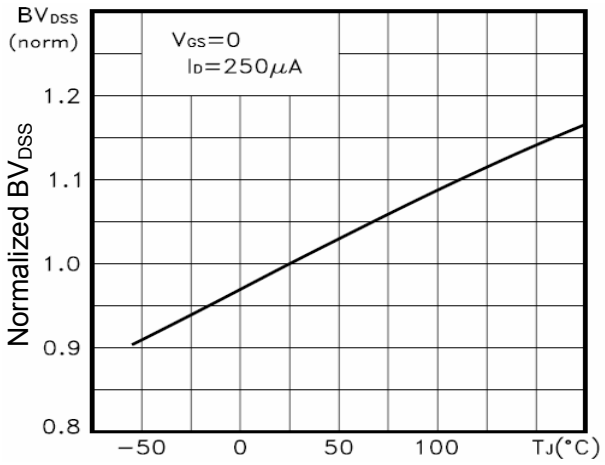


Figure4. ID vs Junction Temperature

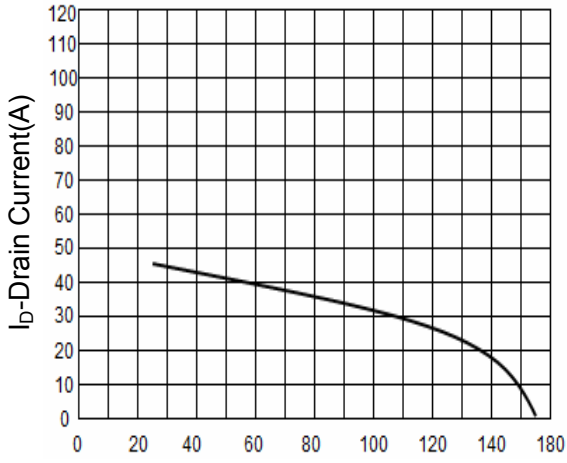


Figure5. VGS(th) vs Junction Temperature

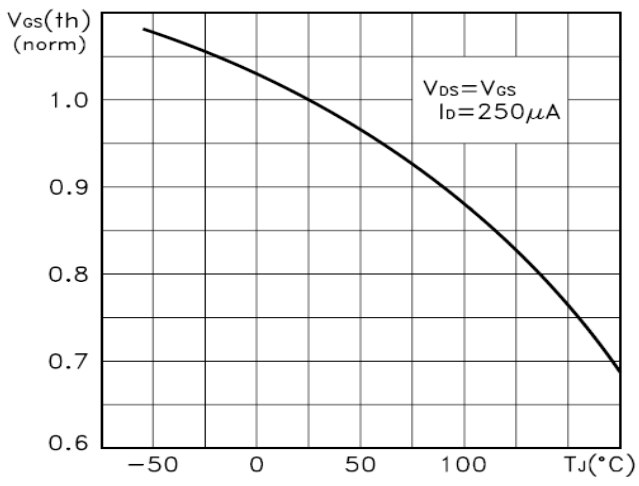


Figure6. Rdson Vs Junction Temperature

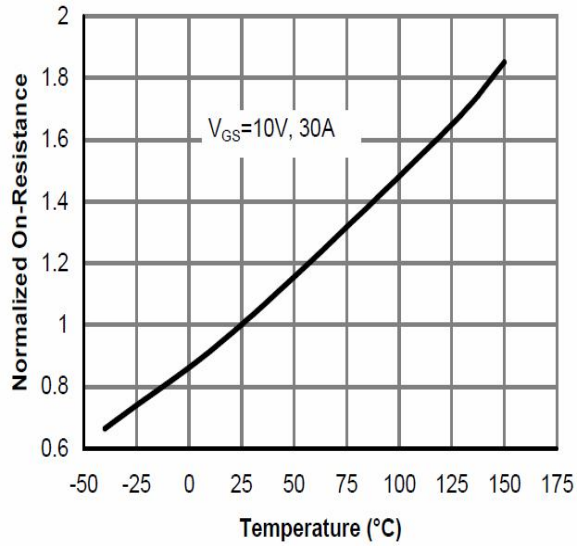


Figure7. Gate Charge

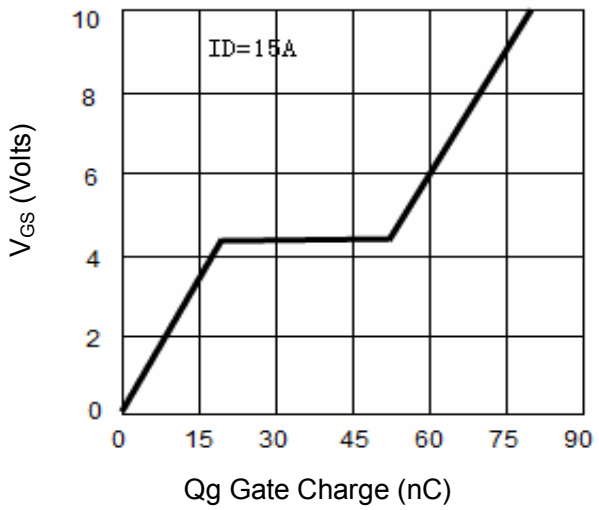


Figure8. Capacitance vs Vds

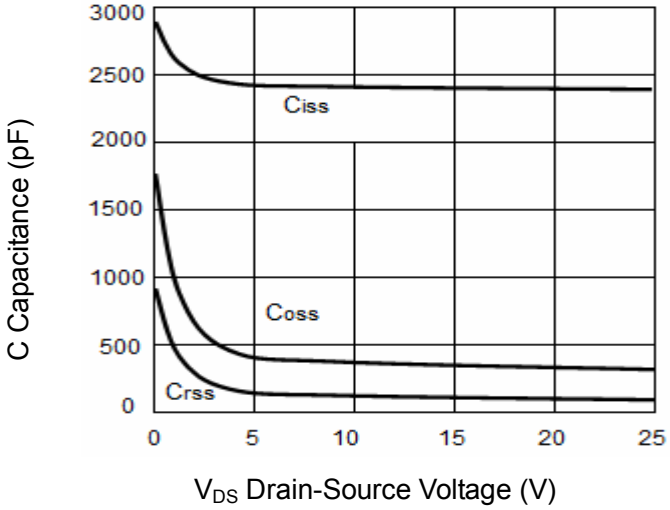


Figure9. Source- Drain Diode Forward

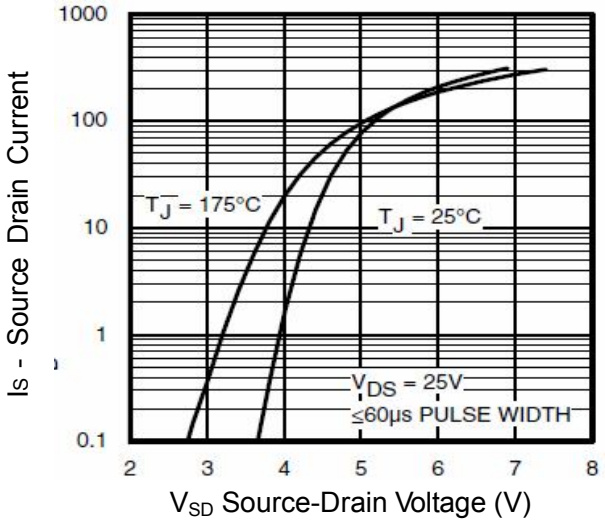


Figure10. Safe Operation Area

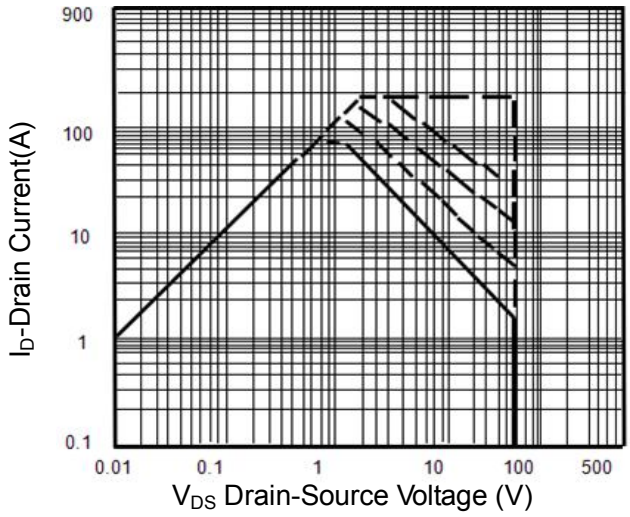
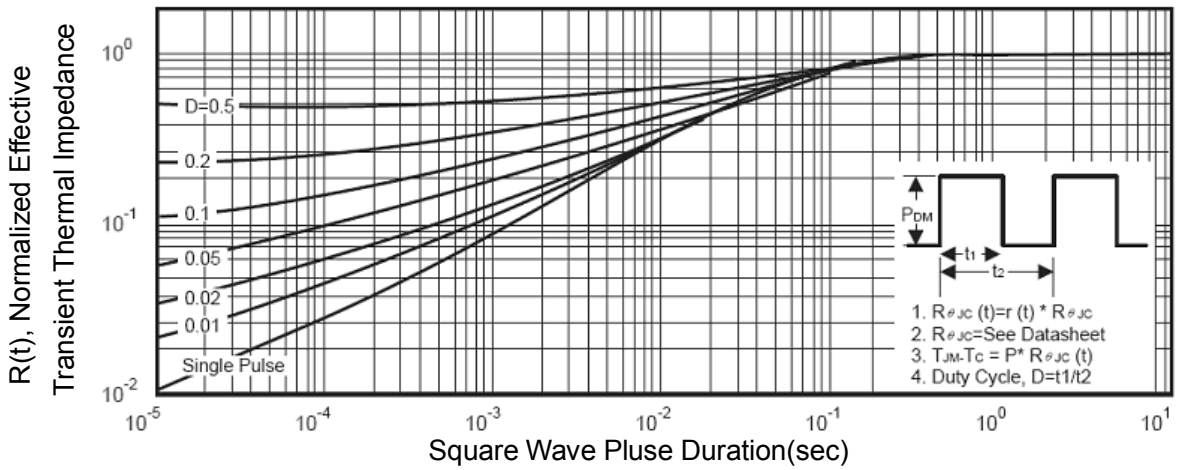
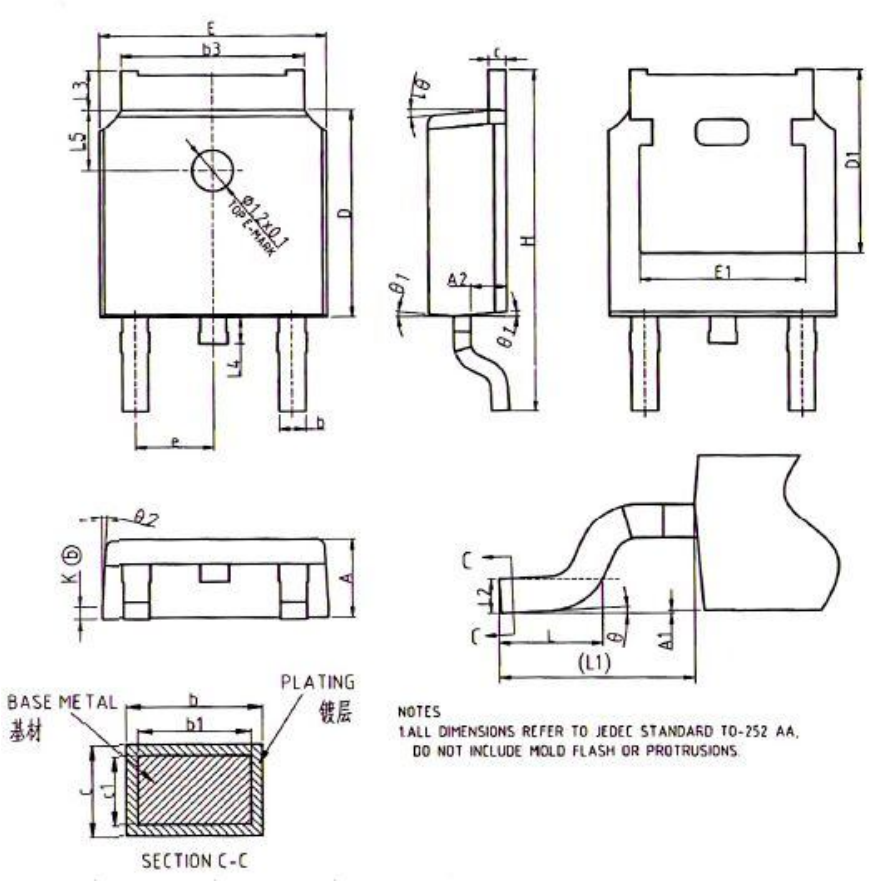


Figure11. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



NOTES
1.ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AA.
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

COMMON DIMENSIONS			
SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1		5.30REF	
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e		2.286BSC	
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1		2.90REF	
L2		0.51BSC	
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
θ	0°	-	8°
θ1	5°	7°	9°
θ2	5°	7°	9°
K		0.40REF	