

N-Channel Trench Power MOSFET

General Description

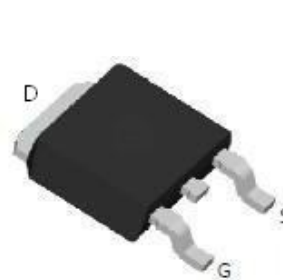
The CSD60N70 is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged EAS capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching applications.

Features

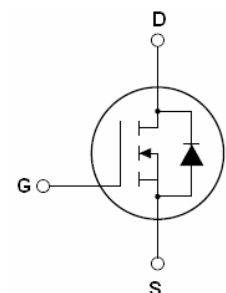
- $V_{DS}=60V$; $I_D=56A@V_{GS}=10V$;
 $R_{DS(ON)}<9.0m\Omega @V_{GS}=10V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



To-252 Top View



Schematic Diagram

$$V_{DS} = 60 V$$

$$I_D = 56A$$

$$R_{DS(ON)} = 7.5m\Omega$$

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
CSD60N70	CSD60N70	TO-252	-	-	-

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	60	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	±25	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	56	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	39	A
$I_{DM(pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	224	A
dv/dt	Peak Diode Recovery Voltage	9.8	V/ns
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	64	W
	Derating Factor	0.43	W/°C
E_{AS}	Single Pulse Avalanche Energy (Note 2)	350	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, V_{DD}=33V, V_G=10V$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	---	2.34	°C/W

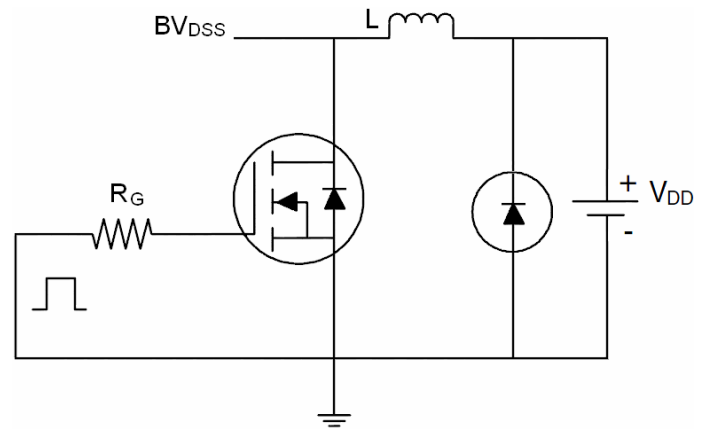
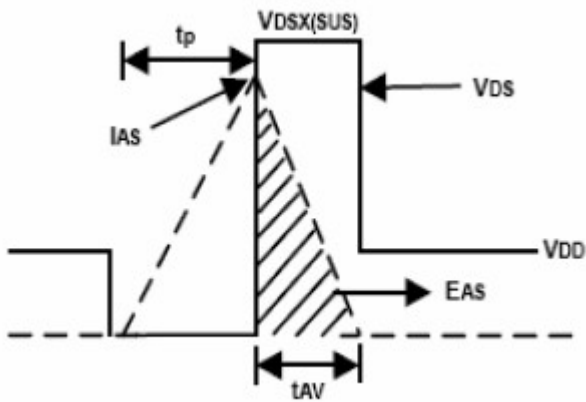
Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60			V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25°C)	V _{DS} =60V, V _{GS} =0V			1	μA
I _{DSS}	Zero Gate Voltage Drain Current(Tc=125°C)	V _{DS} =60V, V _{GS} =0V			10	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±25V, V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2		4	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =40A		7.5	9.0	mΩ
Dynamic Characteristics						
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =15A	18			S
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		2860		pF
C _{oss}	Output Capacitance			281		pF
C _{rss}	Reverse Transfer Capacitance			265		pF
Q _g	Total Gate Charge	V _{DS} =50V, I _D =40A, V _{GS} =10V		77		nC
Q _{gs}	Gate-Source Charge			15.7		nC
Q _{gd}	Gate-Drain Charge			35.2		nC
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V, I _D =2A, R _L =15Ω V _{GS} =10V, R _G =2.5Ω		18		nS
t _r	Turn-on Rise Time			29		nS
t _{d(off)}	Turn-Off Delay Time			55		nS
t _f	Turn-Off Fall Time			27		nS
Source-Drain Diode Characteristics						
I _{SD}	Source-Drain Current(Body Diode)			56		A
I _{SDM}	Pulsed Source-Drain Current(Body Diode)			224		A
V _{SD}	Forward On Voltage ^(Note 1)	T _J =25°C, I _{SD} =40A, V _{GS} =0V		0.89	0.99	V
t _{rr}	Reverse Recovery Time ^(Note 1)	T _J =25°C, I _F =75A di/dt=100A/μs		26		nS
Q _{rr}	Reverse Recovery Charge ^(Note 1)			33		nC
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

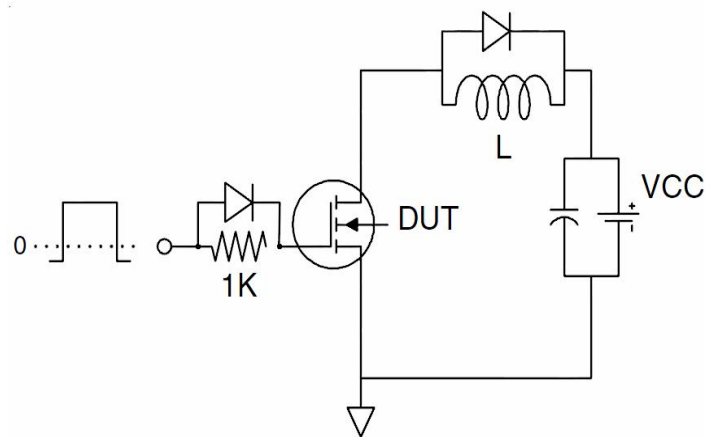
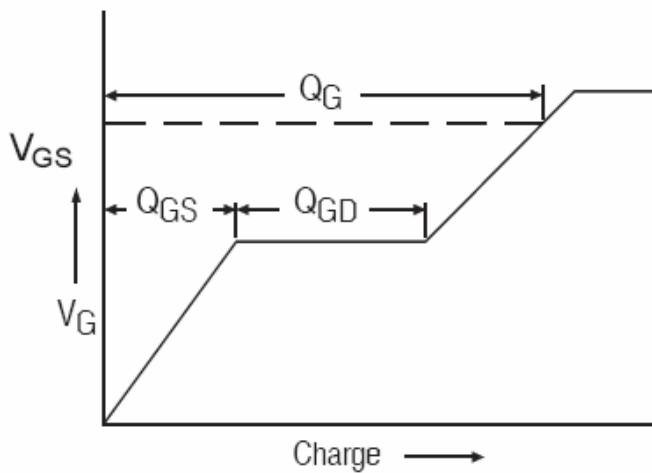
Notes 1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, R_G=25Ω, Starting T_J=25°C

Test Circuit

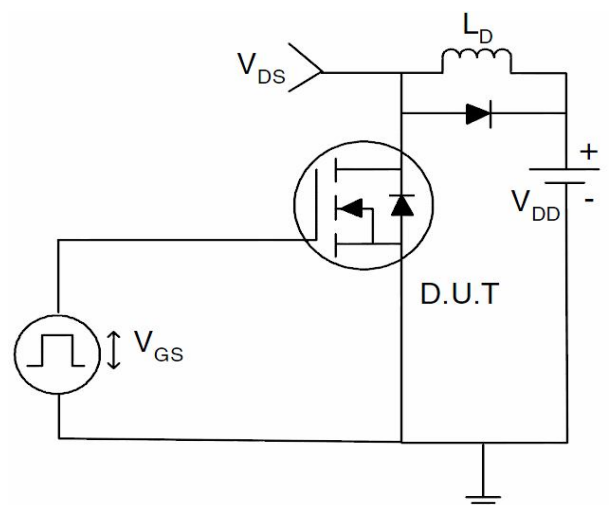
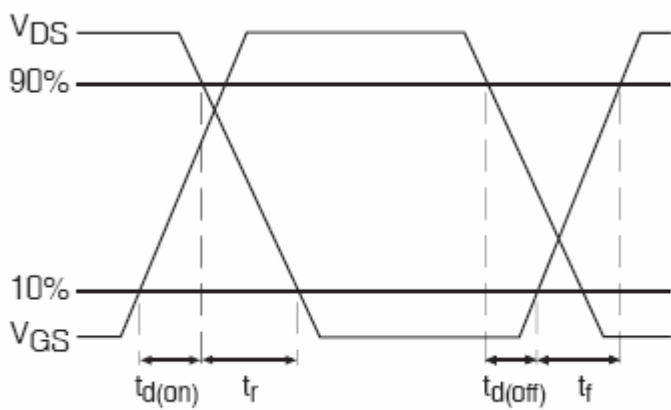
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

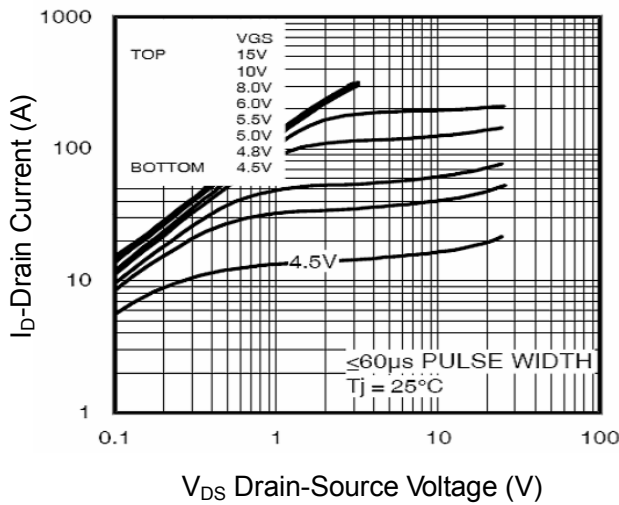


Figure2. Transfer Characteristics

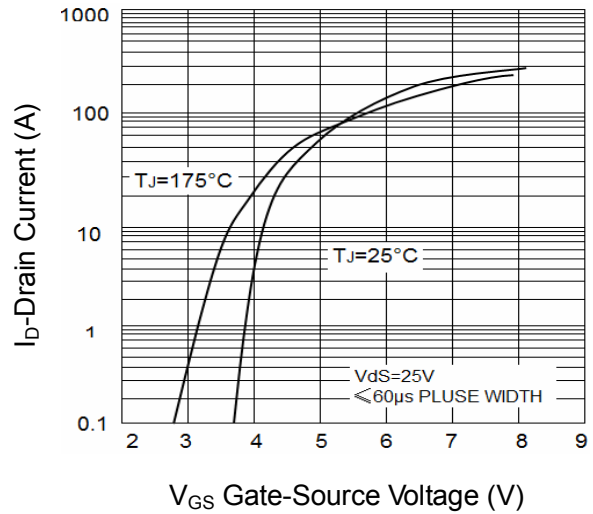


Figure3. BV_{DSS} vs Junction Temperature

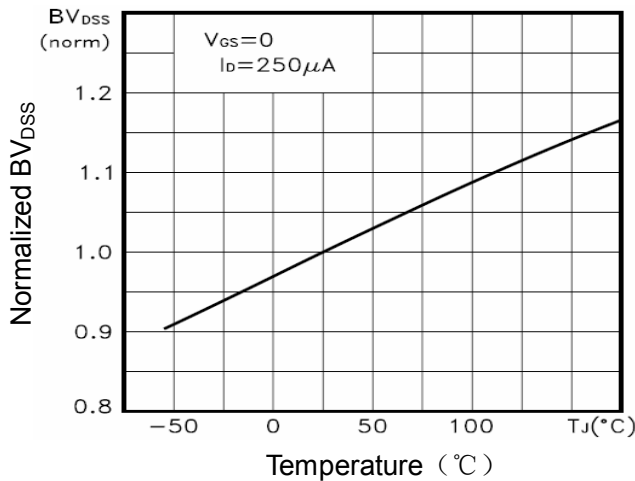


Figure4. ID vs Junction Temperature

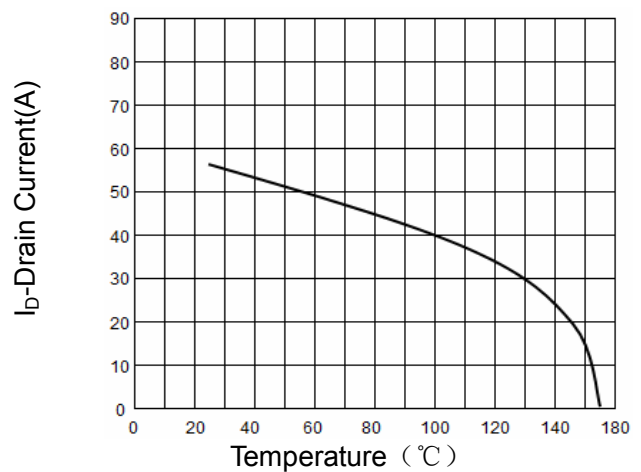


Figure5. VGS(th) vs Junction Temperature

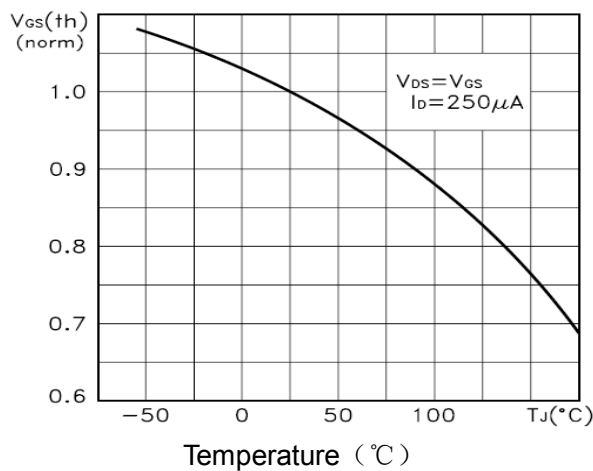


Figure6. R_{dson} Vs Junction Temperature

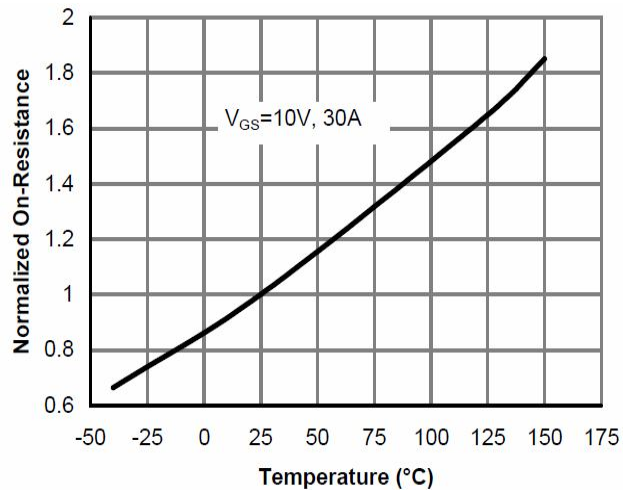


Figure7. Gate Charge

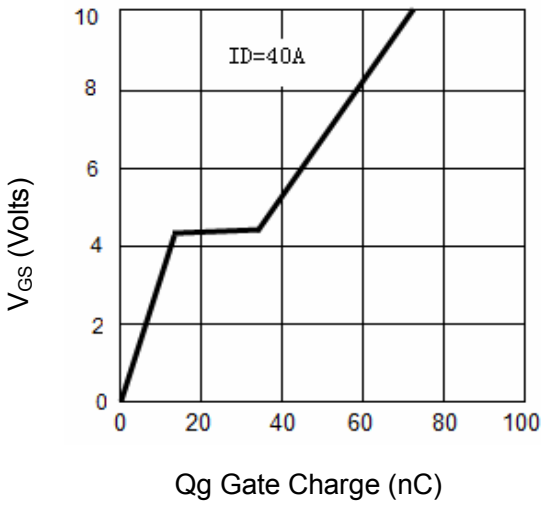


Figure8. Capacitance vs Vds

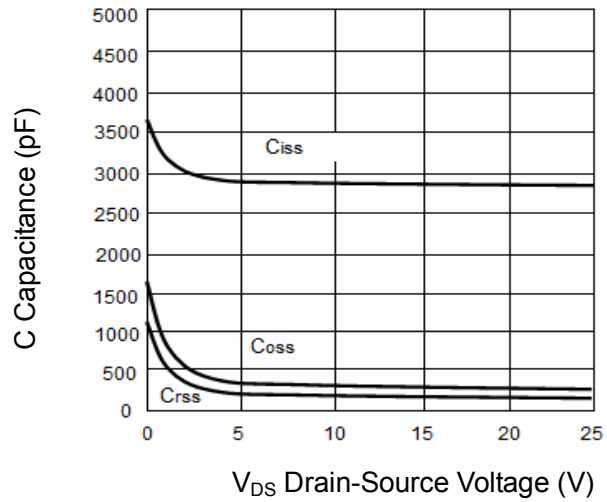


Figure9. Source- Drain Diode Forward

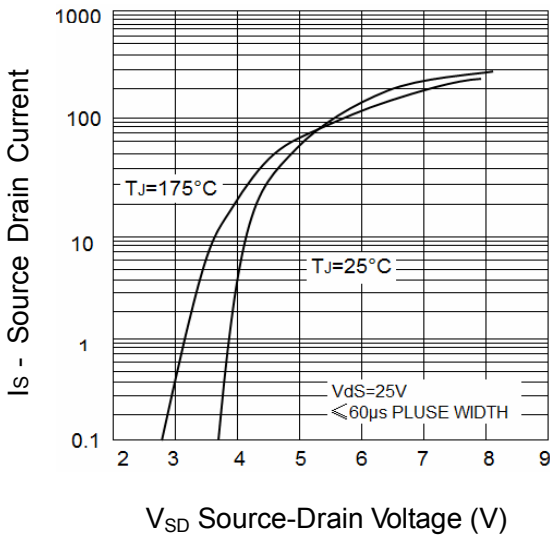


Figure10. Safe Operation Area

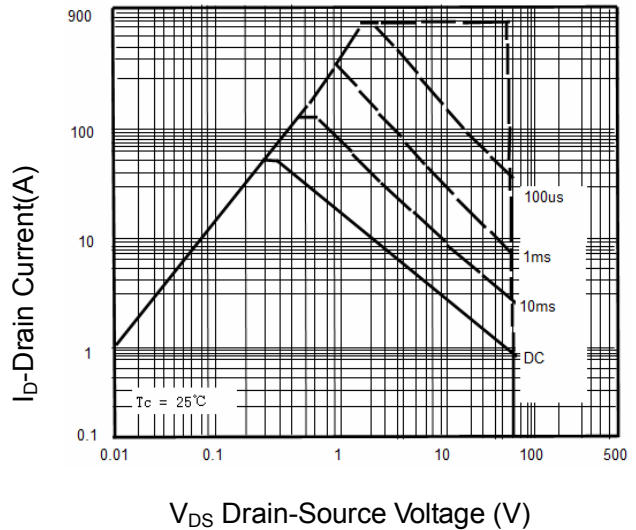
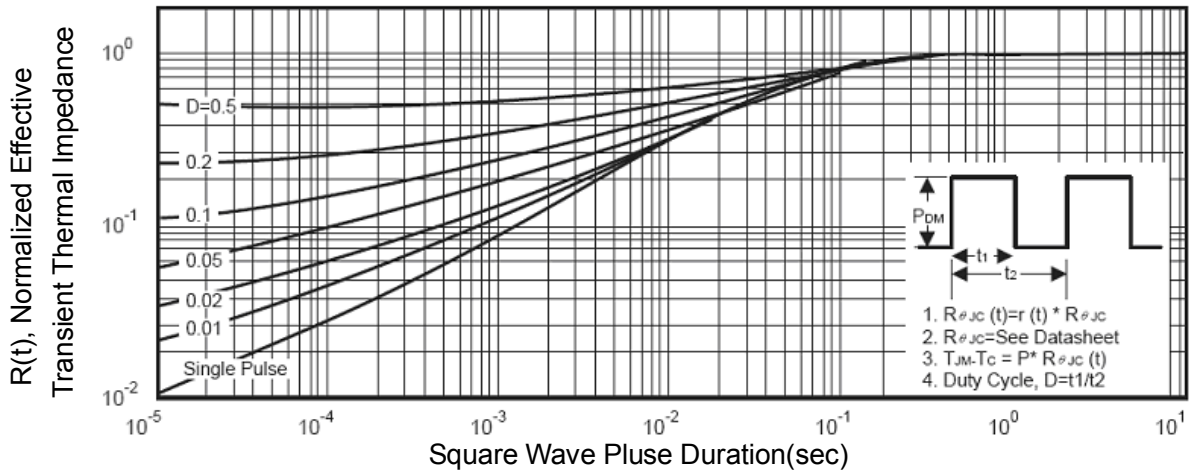
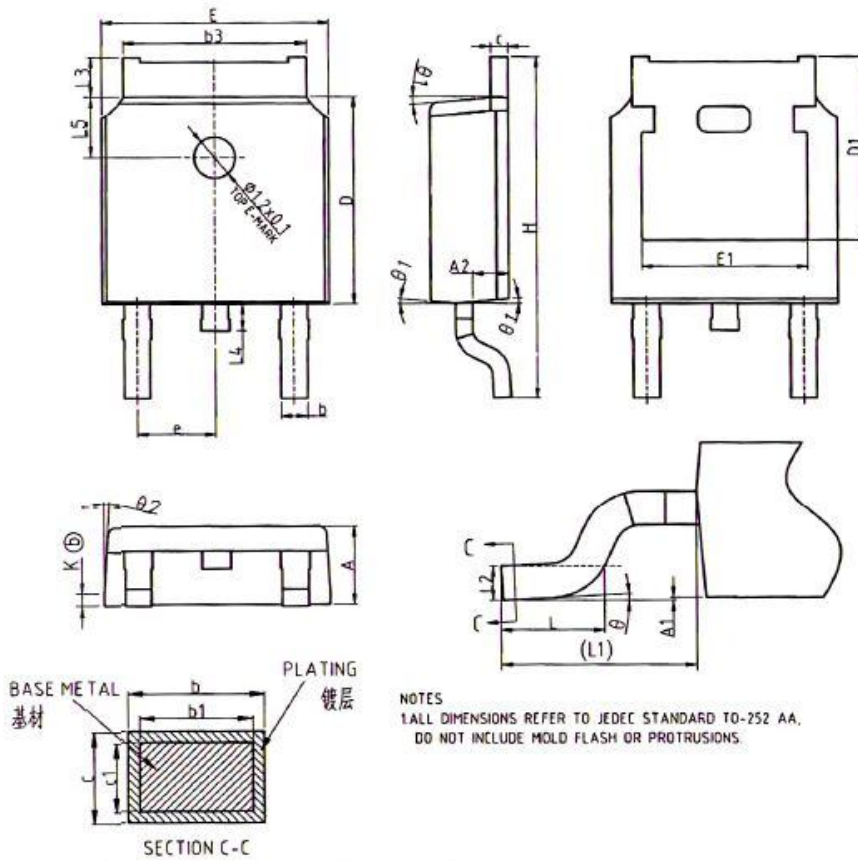


Figure11. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



COMMON DIMENSIONS			
SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
θ	0°	-	8°
$\theta 1$	5°	7°	9°
$\theta 2$	5°	7°	9°
K	0.10REF		

NOTES
 1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AA.
 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.