BlueCore® CSR8311™ QFN Automotive

Features

- Fully qualified Bluetooth ® v4.0 system
- Full-speed Bluetooth operation with full piconet and scatternet support
- Class 1 Bluetooth power level supported
- High-sensitivity Bluetooth receiver
- Wideband speech
- On-chip SBC encoding
- On-chip balun
- Low-power selectable 1.2 to 3.6V I/O
- No external regulators required for USB supply operation
- Full-speed USB 2.0 interface
- Integrated I/O and core regulators
- High-speed UART port (up to 4Mbps)
- 2 x PCM/I²S digital audio interfaces
- Support for IEEE 802 ®.11 coexistence
- Optimised for use on low-cost PCBs
- 40-lead 6 x 6 x 0.9mm, 0.5mm pitch QFN
- Green (RoHS compliant and no antimony or halogenated flame retardants)

Bluetooth® v4.0 Specification
Including Bluetooth low energy

CSR8311A08

Production Information

Issue 9

General Description

BlueCore® CSR8311™ QFN Automotive is a product from CSR's Connectivity Centre. It is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including EDR to 3Mbps and Bluetooth low energy.

Dedicated signal and baseband processing is included for full Bluetooth operation.

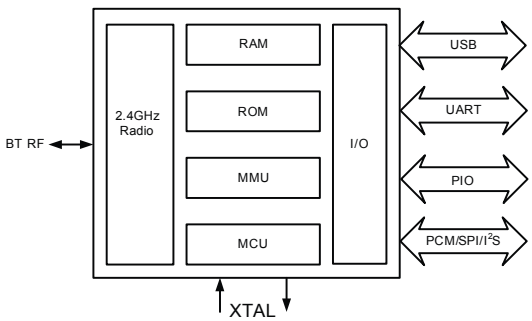
When used with CSR's Synergy host software suite, CSR8311 QFN provides a system fully qualified to the Bluetooth v4.0 specification for data and voice communications.

Applications

- Automotive
- USB Bluetooth dongles

CSR designed CSR8311 QFN to reduce PCB area and the number of external components, including no requirement for an external balun. This ensures that production costs are minimised.

The device incorporates auto-calibration and BIST routines to simplify development, type approval and production test.



Device Details

Bluetooth low energy

- Dual-mode Bluetooth low energy radio
- Support for Bluetooth basic rate/EDR and low energy connections
- 3 Bluetooth low energy connections at the same time as basic rate A2DP

Bluetooth Radio

- Integrated balun (50Ω impedance in TX and RX modes)
- No external trimming is required in production
- Bluetooth v4.0 specification compliant

Bluetooth Transmitter

- 9.5dBm (typical) RF transmit power with level control from on-chip 6-bit DAC
- Class 1, Class 2 and Class 3 support without need for external power amplifier or TX/RX switch
- DQPSK and 8DPSK

Bluetooth Receiver

- -92.5dBm (typical) π/4 DQPSK sensitivity
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Channel classification for AFH
- 2Mbps and 3Mbps EDR support

Baseband and Software

- Internal RAM enables full-speed data transfer, mixed voice and data, and full piconet operation, including all medium rate packet types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Includes support for eSCO and AFH.
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Bluetooth Stack

- CSR's Bluetooth Protocol Stack runs up to HCI on the on-chip MCU

Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter
- Compatible with external clock 16MHz to 40MHz and crystal oscillator 16MHz to 32MHz

Physical Interfaces

- Full-speed (12Mbps) USB 2.0 interface
- Synchronous serial interface up to 4Mbps for system debugging
- UART interface with programmable baud rate up to 4Mbps
- BCSP, H4, H4DS and H5 support
- 2 x PCM interface/I²S interface

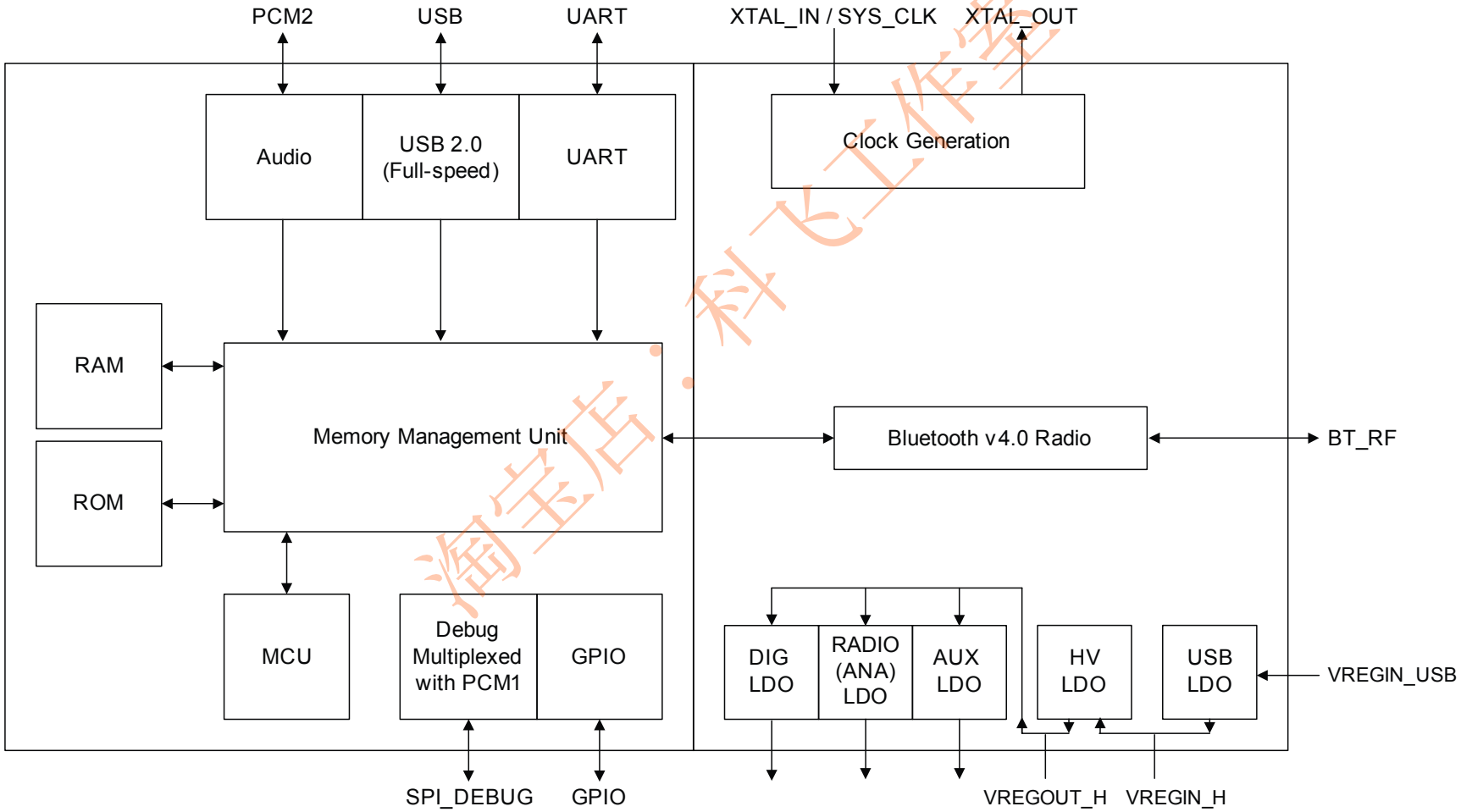
Auxiliary Features

- Power management includes digital shutdown and wake up commands with an integrated low power oscillator
- Auto Baud Rate setting, depending on host interface
- Integrated linear regulators:
  - USB: USB bus supply to 3.3V
  - High-voltage: 2.3V to 4.8V input to 1.85V
  - Low-voltage: VDD_DIG, VDD_ANA and VDD_AUX regulators
- Power-on-reset cell detects low supply voltage
- Arbitrary sequencing of power supplies is permitted

Package

- 40-lead 6 x 6 x 0.9mm, 0.5mm pitch QFN
- Low-cost PCB with no laser via needed

Functional Block Diagram



Document History

Revision	Date	Change Reason
1	28 MAY 10	Original publication of this document.
2	30 SEP 10	Changed CSR8310 to CSR8311 throughout. Added Wideband Speech and low energy features.
3	09 MAR 2011	Updated USB_UART pin description
4	14 MAR 2011	Updated power supply table
5	15 MAR 2011	Editorial update
6	03 OCT 2011	Pre-production Information added.
7	25 OCT 2011	Editorial updates.
8	02 DEC 2011	Change from Pre-production to Production Status.
9	06 MAR 2012	Storage temperature max rating updated. If you have any comments about this document, email Comments@csr.com giving the number, title and section with your feedback.

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

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While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

Refer to www.csrsupport.com for compliance and conformance to standards information.

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1 Package Information

1.1 Pinout Diagram

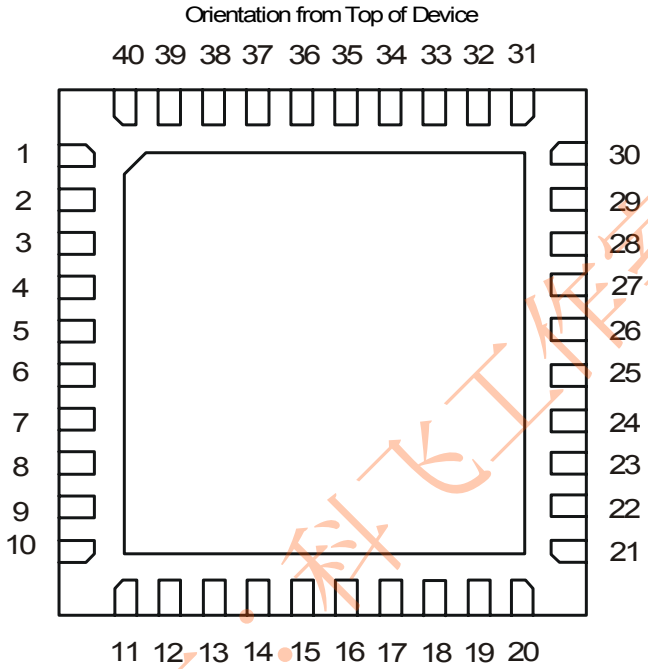

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Figure 1.1: Pinout Diagram

1.2 Device Terminal Functions

Bluetooth RF	Lead	Pad Type	Supply Domain	Description
BT_RF	38	RF	VDD_RADIO	Bluetooth RF transmit/ receive port
VDD_BT_LO	39	Analogue regulator decoupler	-	Connect to pin VDD_ANA and VDD_RADIO via short track.

Oscillator	Lead	Pad Type	Supply Domain	Description
XTAL_IN	4	Analogue	N/A	Crystal connection. Alternative function is as external reference clock input, see Section 3.2.
XTAL_OUT	3			Crystal connection. When in external reference clock mode, see Section 3.2, ground XTAL_OUT on PCB.

UART Interface	Ball	Pad Type	On Reset	Supply Domain	Description
UART_TX	12	Bidirectional, tristate, with weak internal pull-up	Weak PU	VDD_HOST	UART data output, active high
UART_RX	13				UART data input, active high
UART_CTS	17				UART clear to send, active low
UART_RTS	14				UART request to send, active low

USB Interface	Lead	Pad Type	Supply Domain	Description
USB_DP	16	Bidirectional	VDD_HOST	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	15			USB data minus
USB_UART#	19	Input	VDD_HOST	Host select. The state of this pin on boot determines the host transport used. High = USB mode, Low = UART mode. Pin sensed only on boot, and host transport cannot be changed on the fly. Note this pin should be tied directly to GND or VDD_HOST.

PCM Interface	Lead	Pad Type	Supply Domain	Description
PCM_OUT SPI_MISO / PIO[22]	33	Output, tristate, with weak internal pull-down	VDD_PADS	PCM1 port synchronous data output
				SPI data output
				Programmable input/output line
PCM_IN / SPI_MOSI / PIO[21]	34	Input, tristate, with weak internal pull-down	VDD_PADS	PCM1 port synchronous data input
				SPI data input
				Programmable input/output line
PCM_SYNC / SPI_CS# / PIO[23]	36	Bidirectional, tristate, with weak internal pull-down	VDD_PADS	PCM1 port synchronous data sync
				SPI chip select, active low output
				Programmable input/output line

PCM Interface	Lead	Pad Type	Supply Domain	Description
PCM_CLK / SPI_CLK / PIO[24]	35	Bidirectional, tristate, with weak internal pull-down	VDD_PADS	PCM1 port synchronous data clock
				SPI clock
				Programmable input/output line
RST#	11	Pulled down internally until the VDD_DIG rail is turned on, then the pull switches to a strong pull up.	VDD_HOST	Active low reset to the chip
PCM2_CLK	23	Bidirectional, tristate, with weak internal pull-down	VDD_PADS	PCM2 port synchronous data clock
PCM2_SYNC	24	Bidirectional, tristate, with weak internal pull-down	VDD_PADS	PCM2 port synchronous data sync
PCM2_IN	25	Bidirectional, tristate, with weak internal pull-down	VDD_PADS	PCM2 port synchronous data input
PCM2_OUT	26	Bidirectional, tristate, with weak internal pull-down	VDD_PADS	PCM2 port synchronous data output
SPI_PCM#_SEL	21	Input with weak internal pull-down	VDD_PADS	High switches SPI/PCM lines to SPI, low switches SPI/ PCM lines to PCM/PIO use.

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO_5	22	Bidirectional, tristate, with weak internal pull-down	VDD_PADS	Programmable input/output line
PIO_4	27			
PIO_3	30			
PIO_2	28			
PIO_1	29			
PIO_0	32			

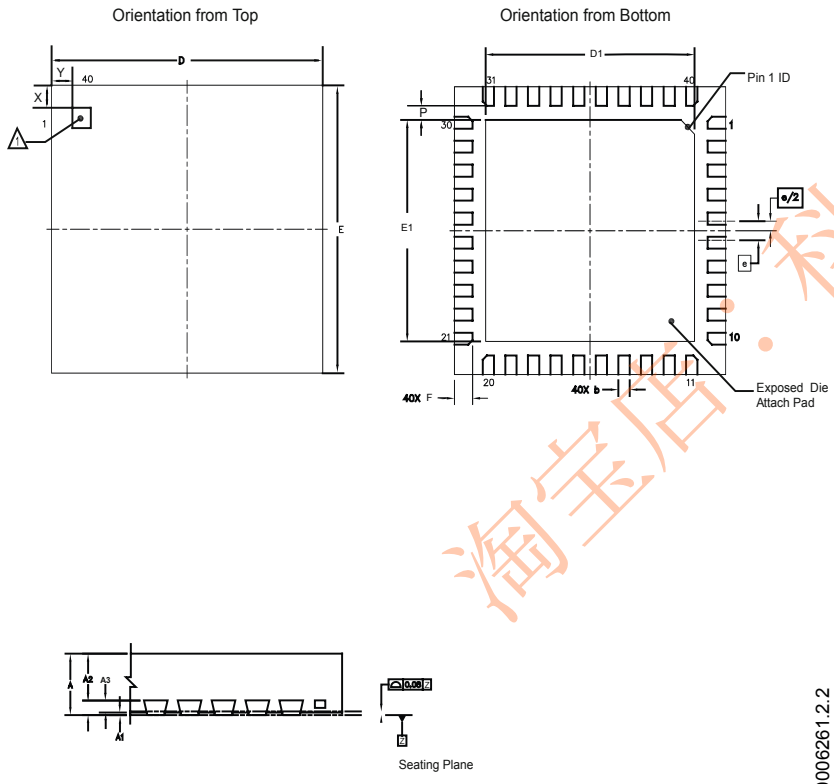
Power Supplies	Lead	Description
VREG_EN	8	Take high to enable internal regulators. Maximum voltage is VREG_IN_HV. **Note:** USB regulator is always enabled and not controlled by VREG_EN
VREG_IN_HV	5	Input to internal high voltage regulator to 1.8V regulator.
VREG_IN_USB	10	Input to USB regulator. Connect to external USB bus supply, e.g. USB_VBUS.
VREG_OUT_USB	9	Output from USB regulator. Connect to external minimum 1µF decoupling capacitor.
VREG_OUT_HV	6	Output from internal high-voltage to 1.8V regulator. Input to second stage internal regulators.
VDD_AUX	40	Internal regulator decoupling capacitor
VDD_DIG	7, 20	Internal regulator decoupling capacitor
VDD_HOST	18	Positive supply for USB and UART pins
VDD_PADS	31	Positive supply for digital input/output pads
VDD_RADIO	37	Internal regulator decoupling capacitor
VDD_ANA	2	Positive supply from auxiliary regulator
VSS	Exposed pad	Ground connection

Unconnected Terminals	Lead	Description
N/C	1	Leave unconnected

Note:

The following leads are not connected: 1

1.3 Package Dimensions



Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.80	0.85	0.90	D1	4.52	4.62	4.72
A1	0.00	0.035	0.05	E1	4.52	4.62	4.72
A2	-	0.65	0.67	F	0.35	0.40	0.45
A3	-	0.203	-	X	-	0.50	-
b	0.20	0.25	0.30	Y	-	0.50	-
D	5.9	6.00	6.05	P	0.22	-	-
E	5.9	6.00	6.05				
e	-	0.5	-				

Notes	1. Top-side polarity mark.		
Description	40-lead Quad Flat No-lead Package		
Size	6 x 6 x 0.9mm	**JEDEC**	MO-220
Pitch	0.5	**Units**	mm

1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 6 x 6 x 0.9mm QFN 40-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- CSR recommends that the PCB land pattern is in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

1.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

2 Bluetooth Modem

2.1 Bluetooth Radio Ports

2.1.1 BT_RF

CSR8311 QFN contains an on-chip balun which combines the balanced outputs of the PA on transmit and produces the balanced input signals for the LNA required on receive. No matching components are needed as the receive mode impedance is 50Ω and the transmitter has been optimised to deliver power in a 50Ω load.

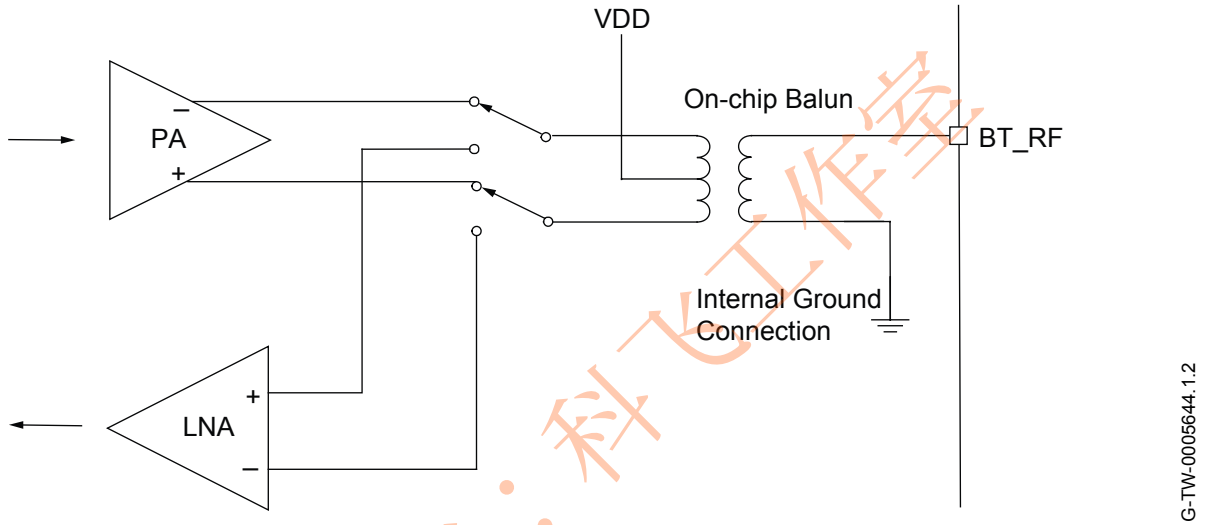


Figure 2.1: Simplified Circuit BT_RF

2.2 Bluetooth Receiver

The receiver features a near-zero IF architecture that enables the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input enables the receiver to operate in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised.

For both basic rate and EDR, an ADC digitises the IF received signal.

2.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the balanced port of the on-chip balun.

2.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the mixer input signal within a limited range. This improves the dynamic range of the receiver, so improving performance in interference limited environments.

2.3 Bluetooth Transmitter

2.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.3.2 Power Amplifier

The internal PA output power is software controlled and configured through a PS Key. This enables CSR8311 QFN to be used in Class 1, Class 2, and Class 3 Bluetooth radios without an external RF PA.

2.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v4.0 specification.

2.5 Baseband

2.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

2.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

The hardware supports all optional and mandatory features of Bluetooth v4.0 specification including AFH and eSCO as well as Bluetooth low energy (to Bluetooth v4.0 specification).

3 Clock Input and Generation

The Bluetooth reference clock for the system is generated from an external clock source frequency of between 16 and 40MHz, or an external crystal.

Note:

CSR8311 QFN requires the sleep clock when using an external reference clock, see Section 3.5.

All CSR8311 QFN internal digital clocks are generated using a phase locked loop, which is locked to the frequency of the clock source.

For more information see *CSR8311 Clock Application Note*.

3.1 Input Frequencies

CSR8311 QFN must be configured to operate with the chosen reference frequency (using the appropriate PS Key, etc.). Until a clock reference frequency is explicitly set, either from EEPROM or over the host interface, radio operation is disabled.

If UART host is selected, CSR8311 QFN autodetects the UART baud rate to establish host communications, PS Keys can then be configured. This depends on the firmware build. Full details are in the *Release Note* for the CSR8311 QFN firmware build on www.csrsupport.com.

3.2 External Reference Clock

3.2.1 Input: XTAL_IN

CSR8311 QFN can use a TCXO reference clock input into XTAL_IN. In this mode, ground XTAL_OUT.

The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion. If peaks of the reference clock are either below VSS or above VDD_AUX, it must be driven through a DC blocking capacitor (approximately 33 to 100pF) connected to XTAL_IN.

Table 3.1 lists the specification for the external reference clock signal.

	Min	Typ	Max	Unit
Frequency[a]	16	26	40	MHz
Frequency tolerance	-20	-	20	ppm
Duty cycle	30:70	50:50	70:30	-
Edge jitter (at zero crossing)	-	-	1.6	ps rms

			Min	Typ	Max	Unit
Phase noise	f_{ref} = 26MHz	1kHz offset	-	-	-120	dBc/Hz
		10kHz offset	-	-	-130	
		100kHz offset	-	-	-135	
Signal level	AC coupled sinusoidal		200	-	VDD_AUX[b]	mV pk-pk
	DC coupled digital	V_{IL}	-	VSS[c]	-	V
		V_{IH}	-	VDD_AUX[b] [c]	-	V

Table 3.1: External Clock Specifications

[a] The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

[b] VDD_AUX is 1.35V nominal

[c] If driven via a DC blocking capacitor max amplitude is reduced to 700mV pk-pk for non 50:50 duty cycle

3.2.2 XTAL_IN Impedance in External Mode

The impedance of XTAL_IN does not change significantly between deep sleep and active modes.

3.2.3 Clock Start-up Delay

CSR8311 QFN hardware incorporates a default 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there are scenarios where the clock is not guaranteed to either exist or be stable after this period. Under these conditions, CSR8311 QFN firmware provides a software function that extends the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 1ms to 31ms. Zero is the default for 5ms delay.

This PS Key enables system optimisation where clock stability latencies are longer or shorter than 5ms, keeping the current consumption of CSR8311 QFN as low as possible. CSR8311 QFN consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

Clock accuracy must be within 20ppm after the delay specified in PSKEY_CLOCK_STARTUP_DELAY. This is to ensure that the radio meets the RF specification. Refer to your product software documentation for a description of PSKEY_CLOCK_STARTUP_DELAY.

3.3 Crystal Oscillator: XTAL_IN and XTAL_OUT

CSR8311 QFN contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. Figure 3.1 shows the external crystal is connected to pins XTAL_IN, XTAL_OUT.

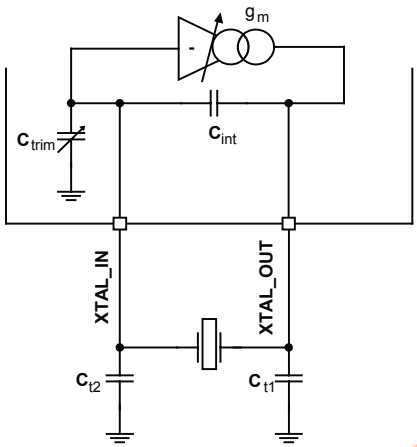


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Figure 3.1: Crystal Driver Circuit

Figure 3.2 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

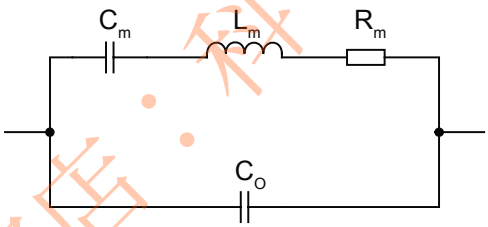

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Figure 3.2: Crystal Equivalent Circuit

The resonant frequency is trimmable with the crystal load capacitance. CSR8311 QFN contains variable internal capacitors to provide a fine trim.

Table 3.2 lists the specification for the crystal oscillator.

Parameter	Min	Typ	Max	Unit
Frequency	16	26	32	MHz
Initial frequency tolerance	-25	-	25	ppm
Pullability	10	15	30	ppm/pF
Amplifier transconductance	2	-	-	mA/V

Table 3.2: Crystal Specification

The CSR8311 QFN driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT.

3.3.1 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. CSR8311 QFN provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing and slew rate at XTAL_IN (to which all on-chip clocks are referred).

Crystal load capacitance, C_l is calculated using Equation 3.1:

$$C_l = C_{int} + \frac{(C_{t2} + C_{trim})\ C_{t1}}{C_{t2} + C_{trim} + C_{t1}}$$

Equation 3.1: Load Capacitance

Note:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

3.3.2 Frequency Trim

CSR8311 QFN enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with an on-chip trim capacitor, C_{trim}. The value of C_{trim} is set by a 6-bit word in PSKEY_ANA_FTRIM. Its value is calculated as follows:

$$C_{trim} = 125fF \times PSKEY\_ANA\_FTRIM$$

Equation 3.2: Trim Capacitance

The C_{trim} capacitor is connected between XTAL_IN and ground. When viewed from the crystal terminals, the combination of the tank capacitors and the trim capacitor presents a load across the terminals of the crystal which varies in steps of typically 125fF for each least significant bit increment of PSKEY_ANA_FTRIM.

Equation 3.3 describes the frequency trim.

$$\frac{\Delta(F_x)}{F_x} = pullability \times 0.110 \times \left(\frac{C_{t1}}{C_{t1} + C_{t2} + C_{trim}}\right)(ppm/LSB)$$

Equation 3.3: Frequency Trim

Note:

F_x = crystal frequency

Pullability is a crystal parameter with units of ppm/pF

Total trim range is 0 to 63

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 3.4.

$$\frac{\partial(F_X)}{\partial(C_l)} = F_X \bullet \frac{C_m}{2(C_l + C_O)^2}$$

Equation 3.4: Pullability

Note:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model), see Figure 3.2

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

3.3.3 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in CSR8311 QFN uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit oscillates if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 3.5.

$$g_m > 3\ \frac{(2\pi F_x)^2\ R_m\ ((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + C_{t1}\ (C_{t2} + C_{trim}))}{C_{t1}\ (C_{t2} + C_{trim})}$$

Equation 3.5: Transconductance Required for Oscillation

CSR8311 QFN guarantees a transconductance value of at least 2mA/V at maximum drive level.

Note:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance.

3.3.4 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the CSR8311 QFN crystal driver circuit is based on a transimpedance amplifier, it is possible to calculate an equivalent negative resistance for it using the formula in Equation 3.6.

$$R_{neg} > \frac{C_{t1}(C_{t2} + C_{trim})}{g_m(2\pi F_x)^2(C_0 + C_{int})((C_{t1} + C_{t2} + C_{trim}) + C_{t1}(C_{t2} + C_{trim}))^2}$$

Equation 3.6: Equivalent Negative Resistance

Equation 3.6 shows the negative resistance of the CSR8311 QFN driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

3.3.5 Crystal PS Key Settings

The CSR8311 QFN firmware automatically controls the drive level on the crystal circuit to achieve optimum input swing. PSKEY_XTAL_TARGET_AMPLITUDE (normal) and PSKEY_LP_XTAL_LVL (deep sleep) are used by the firmware to servo the required amplitude of crystal oscillation. These PS Keys default to a high drive strength and can be lowered to reduce power consumption. Users need to verify that their selected crystal operates under all conditions. Refer to the software build release note for a detailed description.

Configure the CSR8311 QFN to operate with the chosen reference frequency.

3.4 Timing for Frequency

Clock accuracy must be 20ppm after the delay specified by the PS Keys configuring the clock startup delay. This assumes PSKEY_CLOCK_STARTUP_DELAY is set to give a 5ms delay (the default). If not, the accuracy must be 20ppm at the point after the delay specified by that PS Key. For more information see the software documentation for a description of PSKEY_CLOCK_STARTUP_DELAY.

3.5 Sleep Clock

The sleep clock is an external 32.768kHz clock for deep sleep and other low-power modes. The sleep clock is required when CSR8311 QFN uses an external reference clock, see Section 3.2. When the CSR8311 QFN uses a crystal oscillator, see Section 3.3, an external sleep clock is not required, but if available, would slightly reduce system power consumption.

Figure 3.3 shows a typical application.

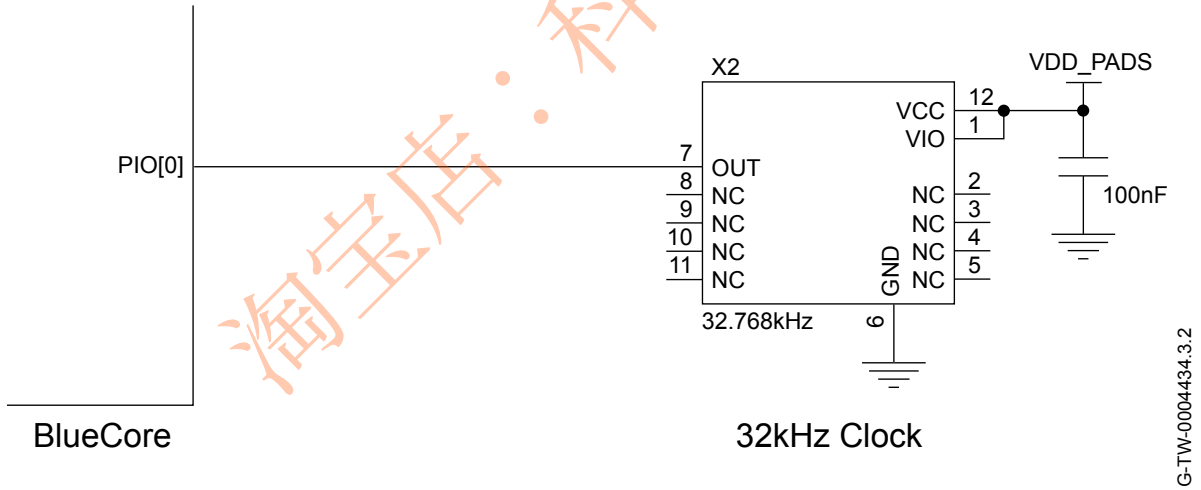

Figure 3.3: Example Sleep Clock Application Circuit

Section 11.3.8 lists the requirements for the sleep clock.

4 Bluetooth Stack Microcontroller

A 16-bit RISC MCU is used for low power consumption and efficient use of memory.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

4.1 Microcontroller

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

4.2 Programmable I/O Ports, PIO

CSR8311 QFN provides 6 standard lines of programmable bidirectional digital I/Os, PIO[5:0]. These I/Os are on the VDD_PADS power domain. If SPI or PCM is not required then these pins are available as PIO, PIO[24:21]. These I/Os are also on the VDD_PADS power domain.

The PIO lines are configured in software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

Note:

CSR cannot guarantee that the PIO assignments remain as described. See the relevant software release note for the build-specific firmware implementation of these PIO lines.

4.3 WLAN Coexistence Interface

There is dedicated hardware to implement a variety of coexistence schemes. There is support for:

- Channel skipping AFH
- Priority signalling
- Channel signalling
- Host passing of channel instructions

The firmware configures the features.

For more information see *BlueCore Bluetooth/IEEE 802.11 Coexistence Application Note*.

5 Memory Interface and Management

5.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

5.2 System RAM

56KB of integrated RAM supports the RISC MCU and is shared between the ring buffers for holding voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

5.3 Internal ROM Memory (5Mb)

5Mb of internal ROM memory is available on the CSR8311 QFN. The internal ROM memory is provided for system firmware, including CSR8311 QFN settings and program code.

5.4 External EEPROM

CSR8311 QFN can use an external I²C EEPROM to store device specific configuration information (PS Keys) such as Bluetooth address and USB descriptors.

An EEPROM is only scanned for if USB_UART# is tied high on boot. If EEPROM with UART host is required, then tie USB_UART# high, and the desired host interface set in the EEPROM.

CSR recommends a minimum 32Kb EEPROM. For more information see *Selection of I²C EEPROMS for Use with BlueCore* for CSR supported EEPROMs.

Table 5.1 shows the EEPROM I²C interface connections on the CSR8311 QFN.

EEPROM	CSR8311 QFN	Description
SCL	PIO[3]	I²C clock
SDA	PIO[4]	I²C data
WP	NC	Write protect, not driven by the CSR8311 QFN. Tie the EEPROM WP line active on PCB.

Table 5.1: EEPROM I²C Interface

Follow the I²C standard timing recommendations regarding correct pull-up and I²C bus data-line capacitance limits. By default, the EEPROM is accessed at I²C standard (100kHz or below) rate, and switchable to fast 400kHz mode by PS Key if the EEPROM supports fast I²C. CSR recommends 400kHz capable EEPROM in these applications to ensure the USB bus power mode boot timing specifications are met.

Alternatively, download the PS Keys from the USB host. This requires a 26MHz crystal operation, which enables the USB host interface to function using the default PS Key configuration. The host must then supply all required PS Key information on first attach.

6 Serial Interfaces

6.1 Programming and Debug Interface

Important Note:

This SPI programming and debug interface can configure the PS Keys stored in external EEPROM and debug the CSR8311 QFN. The interface is often required in production for programming Bluetooth addresses etc., ensuring suitable access is recommended.

CSR provides development and production tools to communicate over this interface from a PC, although a level translator circuit is often required. All are available from CSR.

CSR8311 QFN uses a 16-bit data and 16-bit address programming and debug interface. Transactions occur when the internal processor is running or is stopped.

Data is written or read one word at a time, or the auto-increment feature is available for block access.

7 Host Interface

Use the host interface to:

- Configure CSR8311 QFN to suit the target platform requirements
- Transfer data to and from other Bluetooth devices.

CSR8311 QFN has a new automatic host transport selection scheme that does not require the use of PIOs.

7.1 UART Interface

This is a standard UART interface for communicating with other serial devices.

CSR8311 QFN UART interface provides a simple mechanism for communicating with other serial devices according to RS-232.

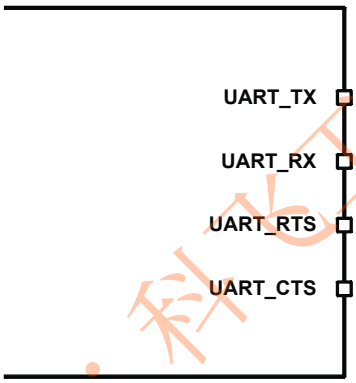

Figure 7.1: Universal Asynchronous Receiver Transmitter

Four signals implement the UART function, as shown in Figure 7.1. When CSR8311 QFN is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using CSR8311 QFN firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 7.1: Possible UART Settings

The UART interface can reset CSR8311 QFN on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 7.2. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOSTIO_UART_RESET_TIMEOUT, a reset occurs. This feature allows a host to initialise the system to a known state. Also, CSR8311 QFN can emit a break character that may be used to wake the host.

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Figure 7.2: Break Signal

Refer to PS Key PSKEY_UART_BITRATE for more information about the baud rates and their values.

Generated baud rate is independent of selected incoming clock frequency. Nokia-specified example rates can be supported with the following errors:

Baud Rate	Error (%)	Jitter (ns)
921.6kbps	0.03	±62.5
1.625Mbps	0.00	±62.5
3.6923Mbps	0.002	±62.5
4Mbps	0.00	0

Note:

The error/jitter figures listed above are those which are added by the CSR8311 QFN UART generator to the residual frequency error and jitter of the CSR8311 QFN VCO, which is linked to that of the incoming system clock.

7.2 USB Interface

CSR8311 QFN has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on CSR8311 QFN acts as a USB peripheral, responding to requests from a master host controller.

CSR8311 QFN supports the *Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification)* and *USB Battery Charging Specification*, available from http://www.usb.org. For more information on how to integrate the USB interface on CSR8311 QFN see the *Bluetooth and USB Design Considerations Application Note*.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
  - Global suspend
  - Selective suspend, includes remote wake
  - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
  - Suspend mode current draw
  - PIO status in suspend mode
  - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

8 Audio Interfaces

8.1 Audio Interface Overview

CSR8311 QFN provides 2 independent audio interfaces which can be configured independently as PCM interface or as Digital audio interface (I²S).

PCM2 has dedicated pins, whereas PCM1 pins are multiplexed with SPI and PIO lines. The information in this section applies to both PCM interfaces.

Each interface has its own set of PS keys.

8.2 PCM Interface

The audio PCM interface on the CSR8311 QFN supports:

- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data.
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
- Hardware on CSR8311 QFN for sending data to and from a SCO connection.
- Up to 3 SCO connections on the PCM interface at any one time.
- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
  - Long Frame Sync
  - Short Frame Sync
  - GCI timing environments
- 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats.
- Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting PSKEY_PCM_CONFIG32.

8.2.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, CSR8311 QFN generates PCM_CLK and PCM_SYNC.

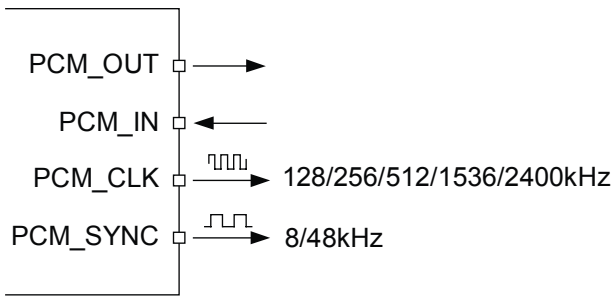

Figure 8.1: PCM Interface Master

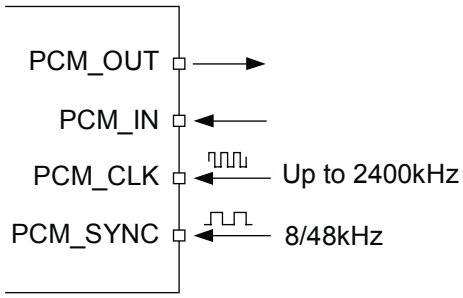

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Figure 8.2: PCM Interface Slave

8.2.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When CSR8311 QFN is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8 bits long. When CSR8311 QFN is configured as PCM Slave, PCM_SYNC is from 1 cycle PCM_CLK to half the PCM_SYNC rate.

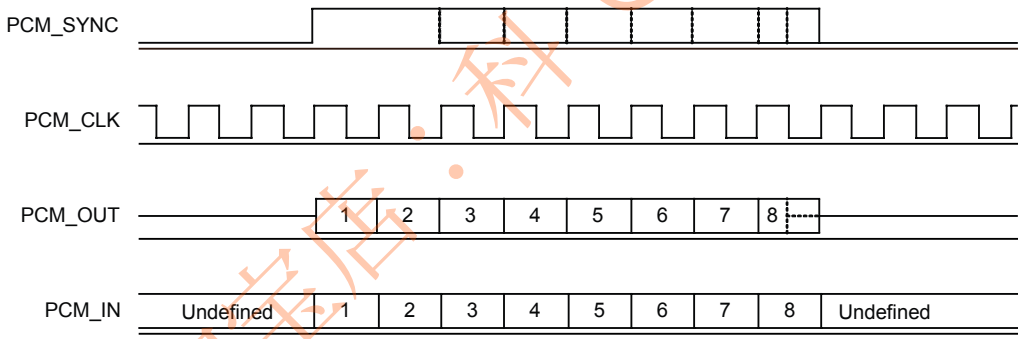

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Figure 8.3: Long Frame Sync (Shown with 8-bit Companded Sample)

CSR8311 QFN samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

8.2.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always 1 clock cycle long.

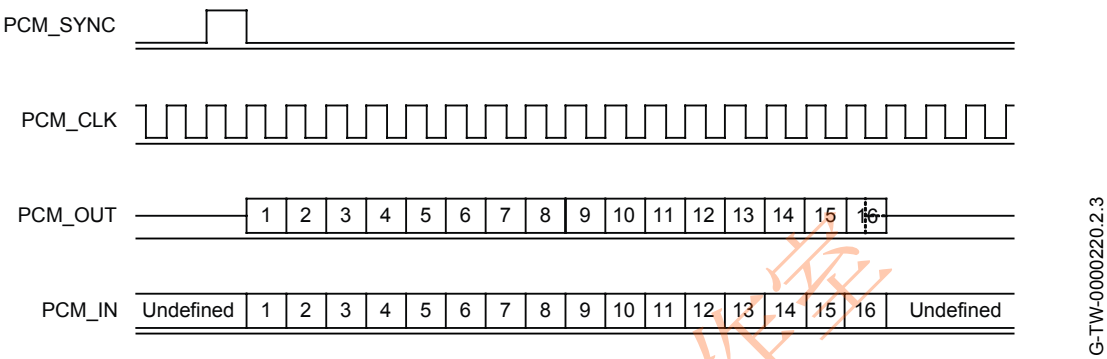


Figure 8.4: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, CSR8311 QFN samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

8.2.4 Multi-slot Operation

More than 1 SCO connection over the PCM interface is supported using multiple slots. Up to 3 SCO connections are carried over any of the first 4 slots.

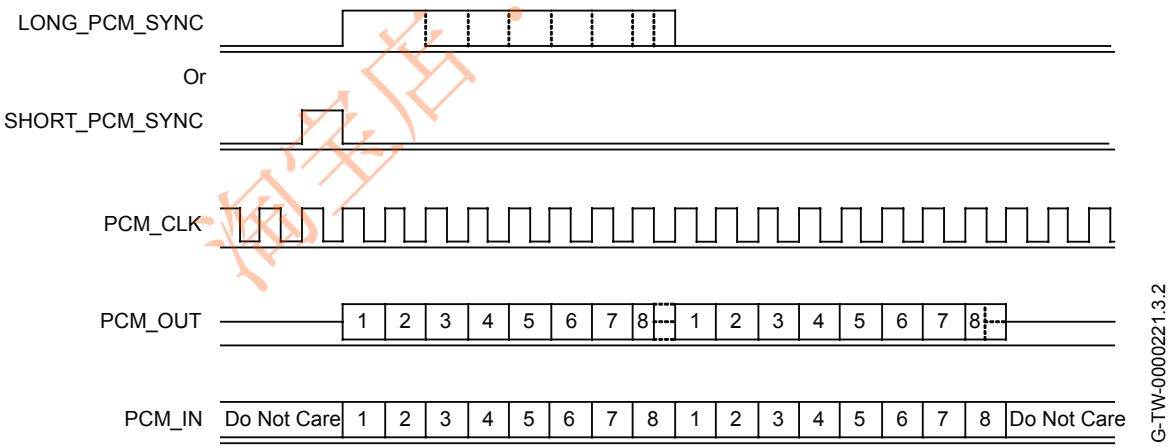


Figure 8.5: Multi-slot Operation with 2 Slots and 8-bit Companded Samples

8.2.5 GCI Interface

CSR8311 QFN is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The 2 64kbps B channels are accessed when this mode is configured.

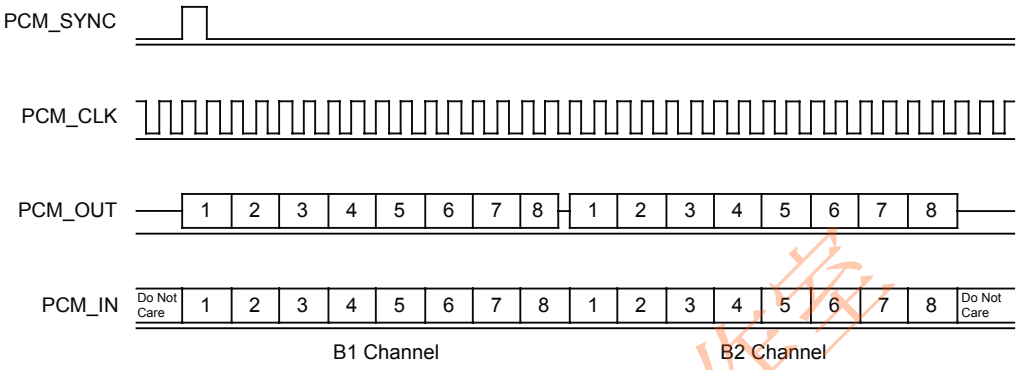


Figure 8.6: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz.

8.2.6 Slots and Sample Formats

CSR8311 QFN receives and transmits on any selection of the first 4 slots following each sync pulse. Slot durations are either 8 or 16 clock cycles:

- 8 clock cycles for 8-bit sample formats.
- 16 clock cycles for 8-bit, 13-bit or 16-bit sample formats.

CSR8311 QFN supports:

- 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats.
- A sample rate of 8ksps.
- Little or big endian bit order.
- For 16-bit slots, the 3 or 8 unused bits in each slot are filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some codecs.

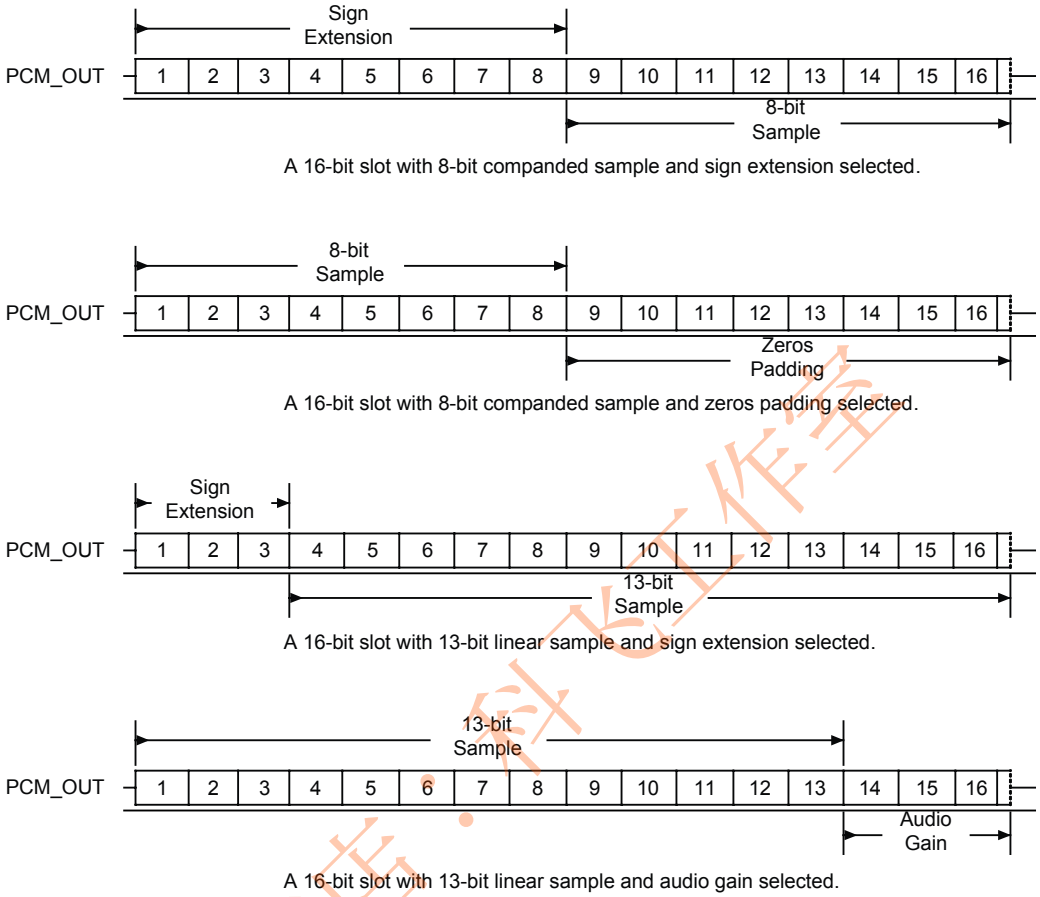


Figure 8.7: 16-bit Slot Length and Sample Formats

8.2.7 Additional Features

CSR8311 QFN has a mute facility that forces PCM_OUT to be 0. In master mode, CSR8311 QFN is compatible with some codecs which control power down by forcing PCM_SYNC to 0 while keeping PCM_CLK running.

8.2.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Frequency selection is programmable.	-	128	-	kHz
				256		
				512		
		48MHz DDS generation. Frequency selection is programmable.	2.9	-	-	kHz
-	PCM_SYNC frequency for SCO connection		-	8	-	kHz
t_{mclkh} [(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} [(a)]	PCM_CLK low	4MHz DDS generation	730	-	-	ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk

Table 8.1: PCM Master Timing

[(a)] Assumes normal system clock operation. Figures vary during low-power modes, when system clock speeds are reduced.

Symbol	Parameter		Min	Typ	Max	Unit
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high	4MHz DDS generation	-	-	20	ns
		48MHz DDS generation	-	-	40.83	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (long frame sync only)	4MHz DDS generation	-	-	20	ns
		48MHz DDS generation	-	-	40.83	ns

Symbol	Parameter		Min	Typ	Max	Unit
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low	4MHz DDS generation	-	-	20	ns
		48MHz DDS generation	-	-	40.83	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		20	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		0	-	-	ns

Table 8.2: PCM Master Mode Timing Parameters

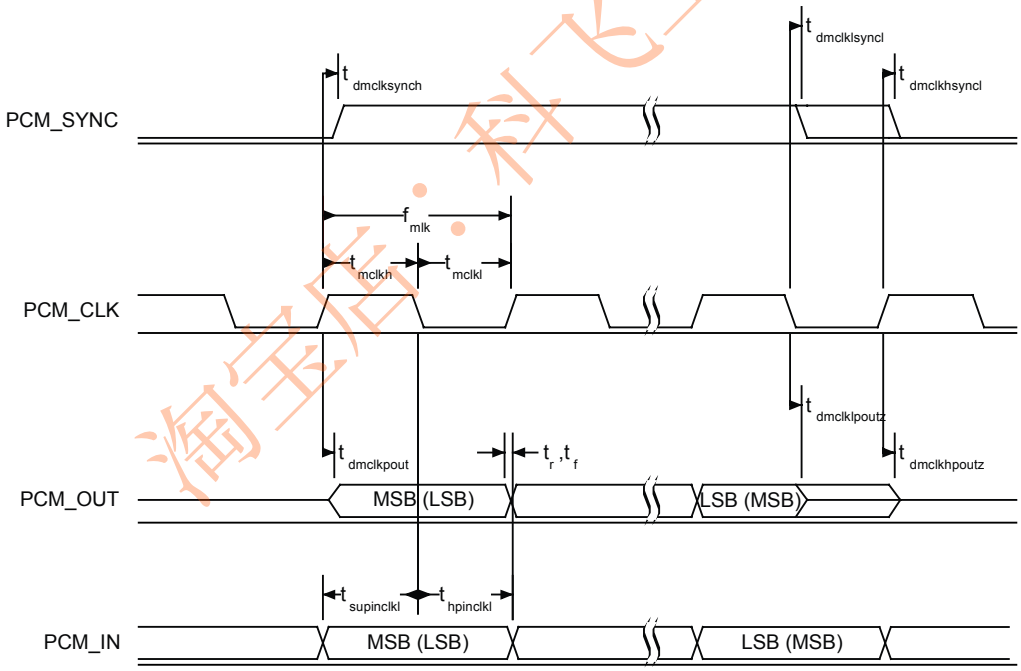


Figure 8.8: PCM Master Timing Long Frame Sync

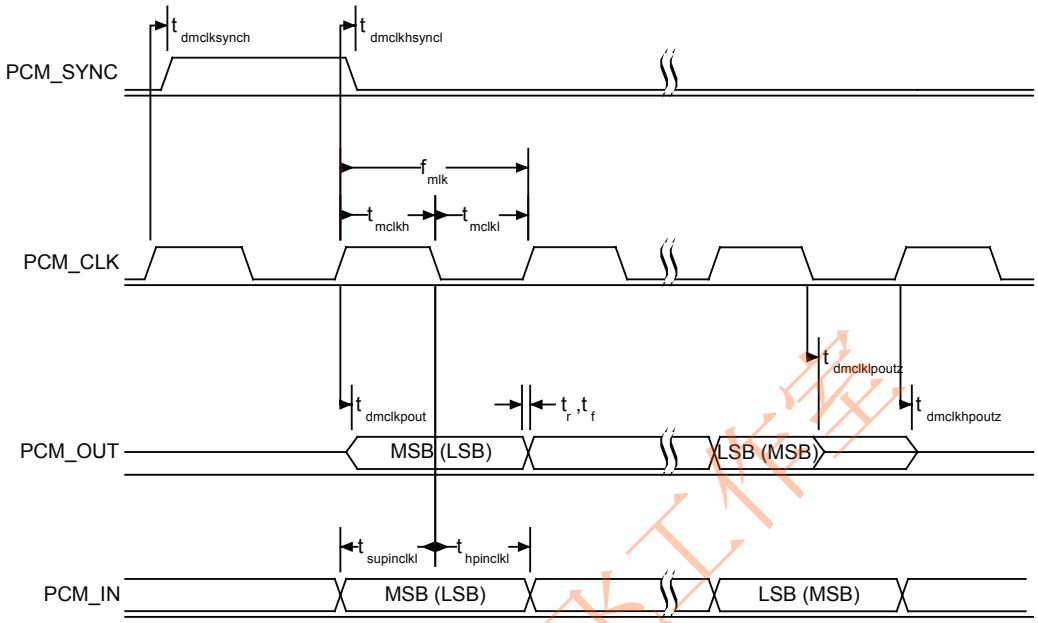


Figure 8.9: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns

Table 8.3: PCM Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	2	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	20	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (long frame sync only)	-	-	15	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	15	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	20	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	2	-	-	ns

Table 8.4: PCM Slave Mode Timing Parameters

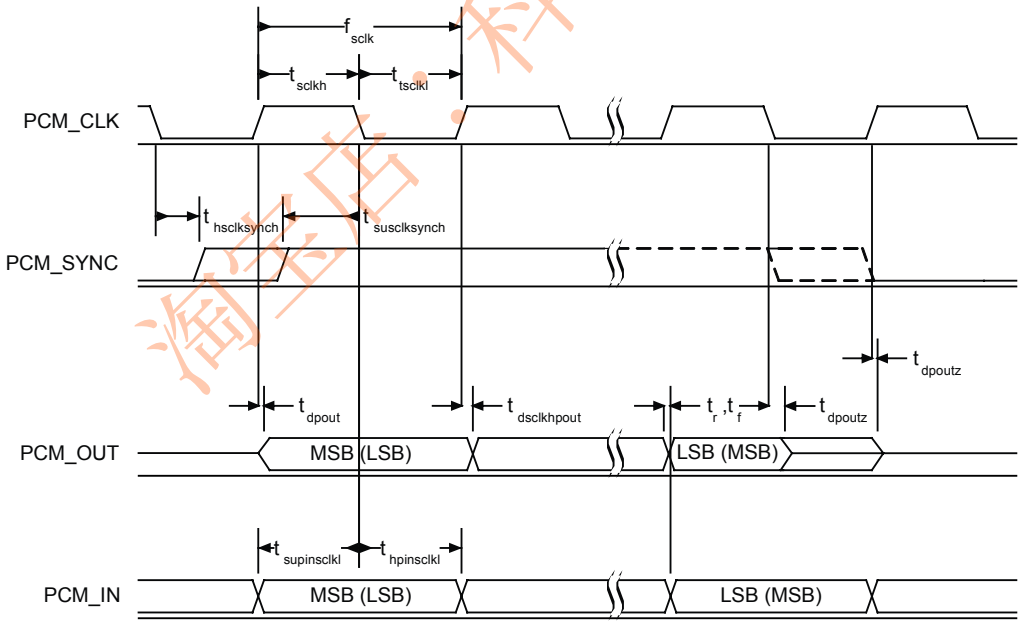


Figure 8.10: PCM Slave Timing Long Frame Sync

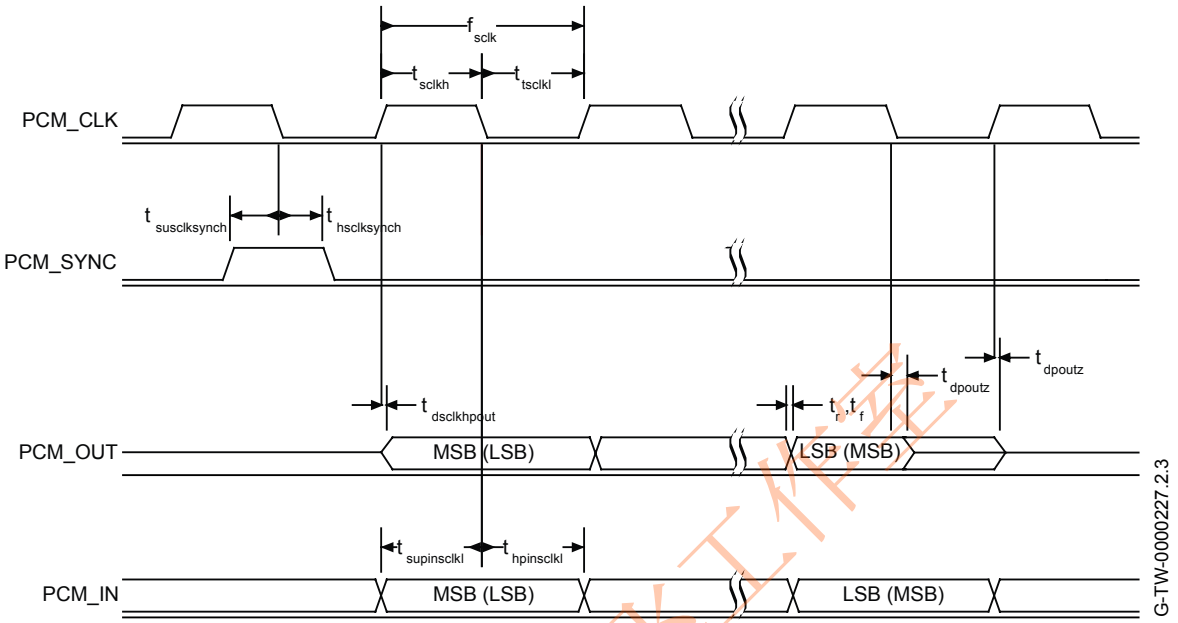


Figure 8.11: PCM Slave Timing Short Frame Sync

8.2.9 PCM_CLK and PCM_SYNC Generation

CSR8311 QFN has 2 methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from CSR8311 QFN internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating these signals by DDS from an internal 48MHz clock, which enables a greater range of frequencies to be generated with low jitter but consumes more power. To select this second method set bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC is either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 8.1 describes PCM_CLK frequency when generated from the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 8.1: PCM_CLK Frequency Generated Using the Internal 48MHz Clock

Set the frequency of PCM_SYNC relative to PCM_CLK using Equation 8.2:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 8.2: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to `0x08080177`.

8.2.10 PCM Configuration

Configure the PCM by using the PS Keys PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristate of PCM_OUT.

8.3 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 8.5 lists these alternative functions. Figure 8.12 shows the timing diagram.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 8.5: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Configure the digital audio interface using PSKEY_DIGITAL_AUDIO_CONFIG, see *BlueCore Audio API Specification* and the PS Key file.

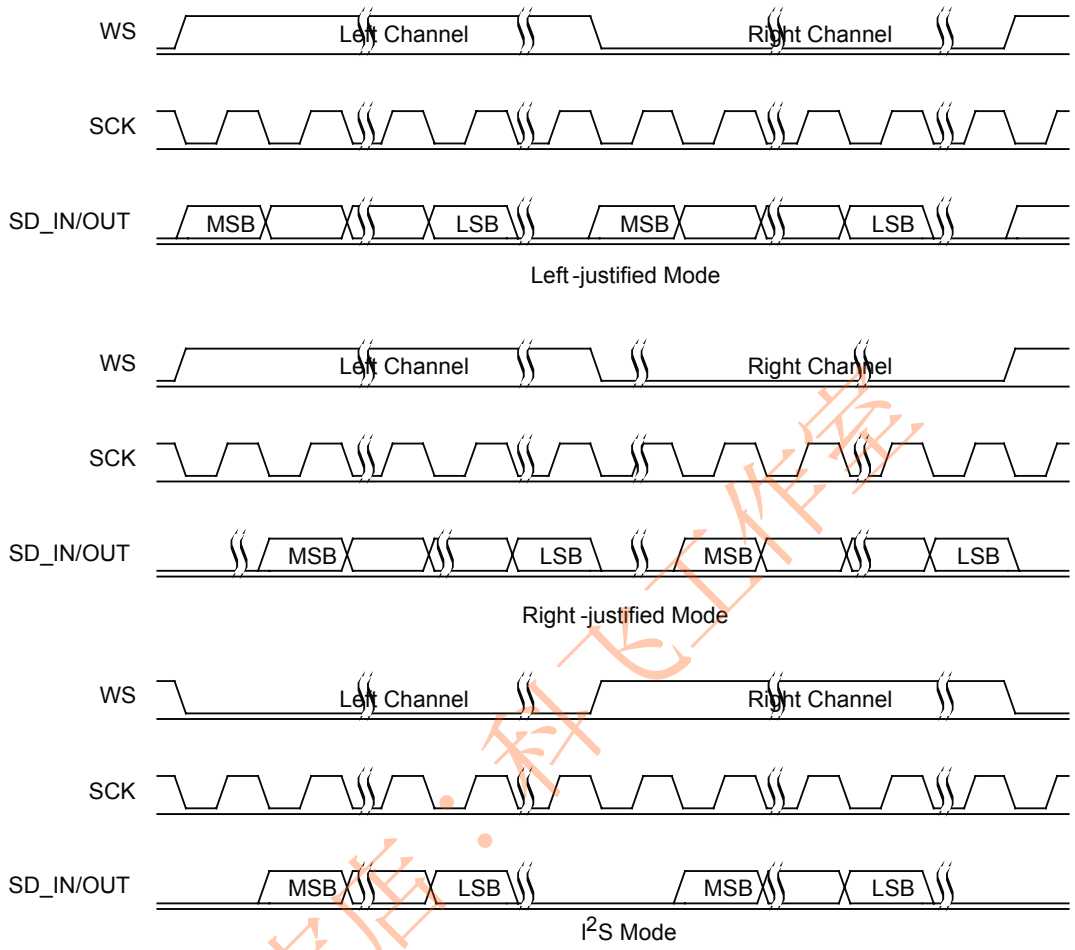


Figure 8.12: Digital Audio Interface Modes

The internal representation of audio samples within CSR8311 QFN is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns

Table 8.6: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{ssu}	WS valid to SCK high set-up time	20	-	-	ns
t_{sh}	SCK high to WS invalid hold time	2.5	-	-	ns
t_{opd}	SCK low to SD_OUT valid delay time	-	-	20	ns
t_{isu}	SD_IN valid to SCK high set-up time	20	-	-	ns
t_{ih}	SCK high to SD_IN invalid hold time	2.5	-	-	ns

Table 8.7: I²S Slave Mode Timing

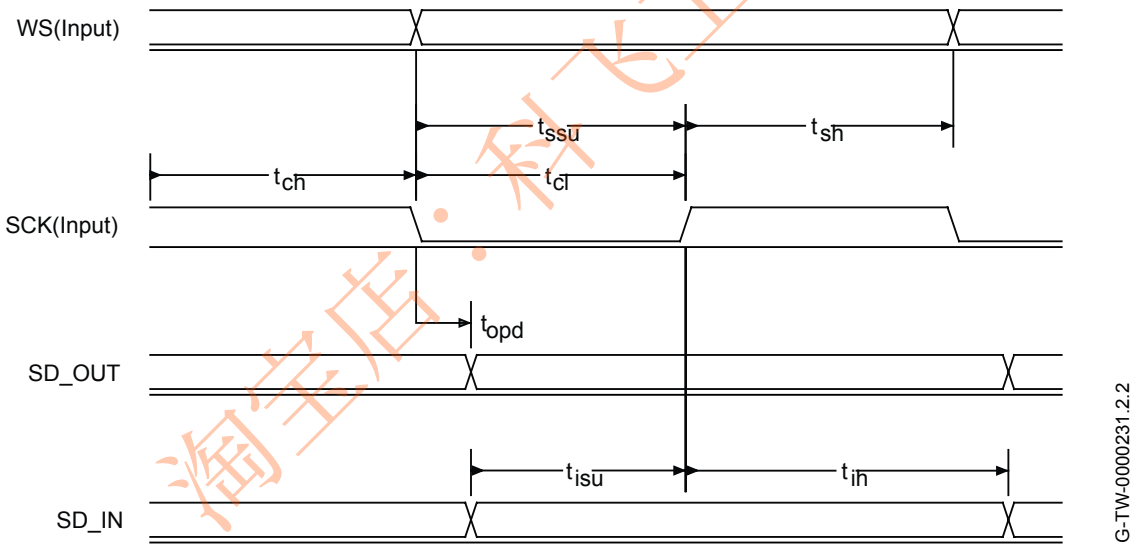


Figure 8.13: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz

Table 8.8: Digital Audio Interface Master Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{spd}	SCK low to WS valid delay time	-	-	39.27	ns
t_{opd}	SCK low to SD_OUT valid delay time	-	-	18.44	ns
t_{isu}	SD_IN valid to SCK high set-up time	18.44	-	-	ns
t_{ih}	SCK high to SD_IN invalid hold time	0	-	-	ns

Table 8.9: I²S Master Mode Timing Parameters, WS and SCK as Outputs

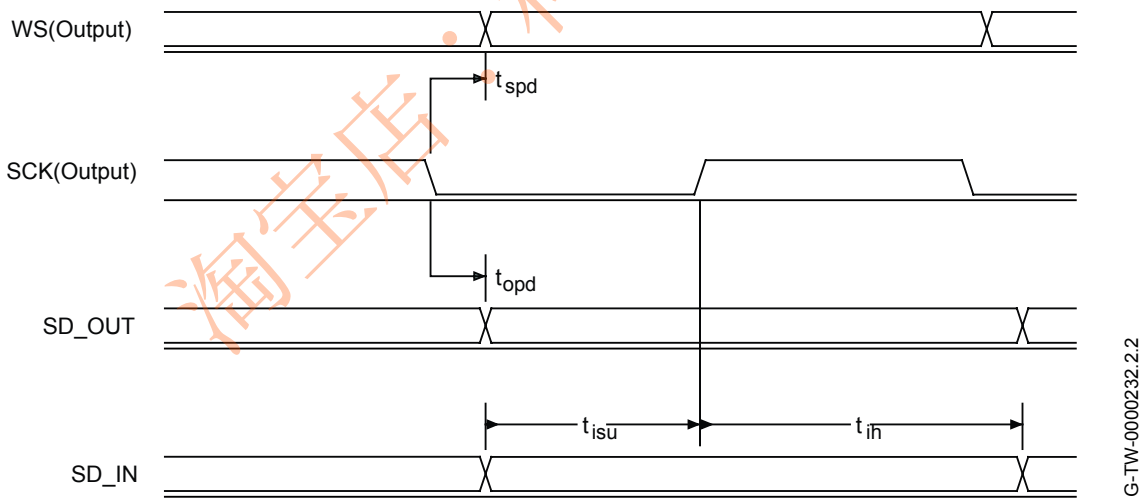


Figure 8.14: Digital Audio Interface Master Timing

9 Power Control and Regulation

Figure 9.1 shows the configuration of the regulators available on the CSR8311 QFN.

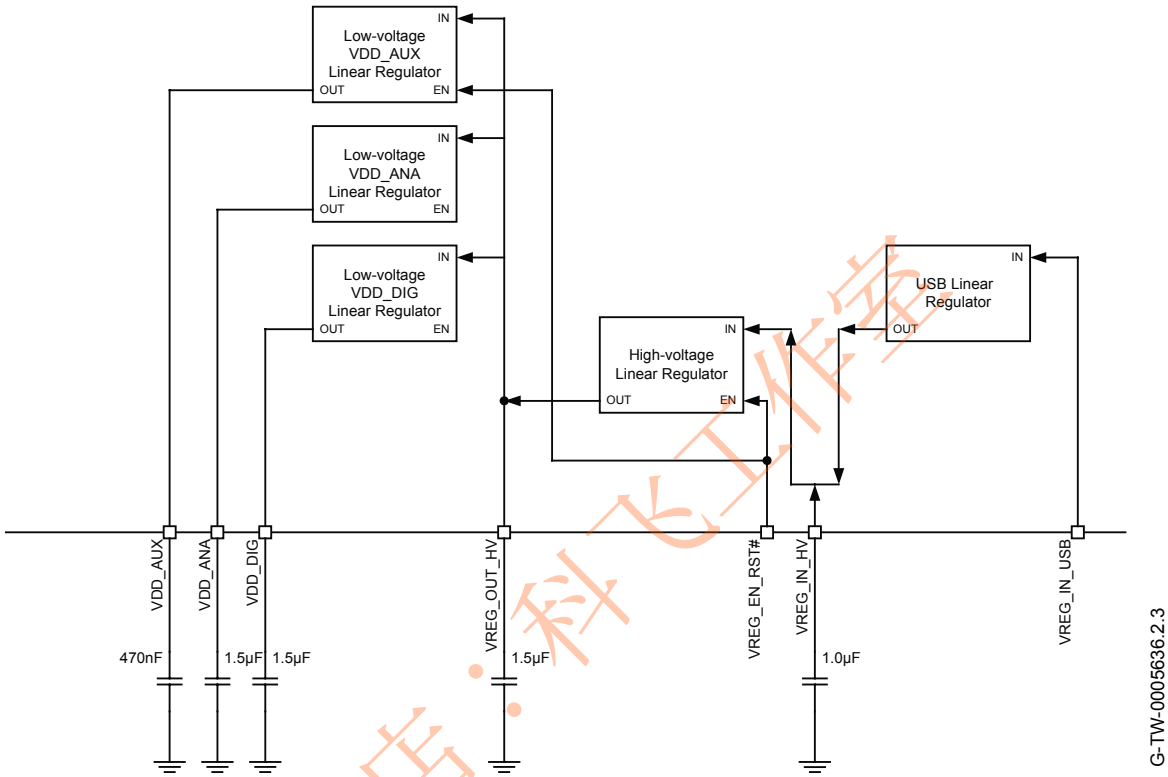


Figure 9.1: Power Control Configuration Diagram

9.1 USB Linear Regulator

The integrated USB LDO linear regulator is available as a 3.3V supply rail and is intended to supply the USB interface and the high-voltage linear regulator. The input voltage range is between 4.20V and 5.75V. The maximum current from this regulator is 150mA.

Externally decouple the output of this regulator using a low ESR MLC capacitor to the VREG_IN_HV pin. The regulator operates correctly with an output capacitor of 1µF to 4.7µF (±20%).

This regulator is enabled by default. If the USB linear regulator is not required leave its input (VREG_IN_USB) unconnected.

9.2 High-voltage Linear Regulator

The integrated high-voltage linear regulator is available to power the main 1.8V supply rail. The input voltage range is between 2.3V and 4.8V. The maximum current from this regulator is 100mA.

Externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 1.5µF to the VREG_OUT_HV pin.

Take VREG_EN high to enable this regulator.

Important Note:

CSR recommends that VREG_EN is not taken high before the supply on VREG_IN_HV is present.

If this regulator is not required then leave VREG_IN_HV unconnected or tied to VREG_OUT_HV.

9.3 Low-voltage VDD_DIG Linear Regulator

The integrated low-voltage VDD_DIG linear regulator is available to power a 0.90V to 1.25V supply rail which includes the digital circuits on CSR8311 QFN. The input voltage range is between 1.70V and 1.95V.

Externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 1.5µF to the VDD_DIG pin.

Software enables and controls the output voltage.

9.4 Low-voltage VDD_RADIO Linear Regulator

The integrated low-voltage VDD_RADIO linear regulator is available to power a 1.35V analogue supply rail which includes the radio circuits on CSR8311 QFN. The input voltage range is between 1.70V and 1.95V.

Externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 1.5µF to the VDD_RADIO pin.

Software enables and controls the output voltage. The regulator is disabled when CSR8311 QFN is in deep sleep or reset.

9.5 Low-voltage VDD_AUX Linear Regulator

The integrated low-voltage VDD_AUX linear regulator is available to power a 1.35V auxiliary supply rail which includes the VDD_AUX supply on CSR8311 QFN. The input voltage range is between 1.70V and 1.95V.

Externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 470nF to the VDD_AUX pin.

Take VREG_EN high to enable this regulator.

Important Note:

CSR recommends that VREG_EN is not taken high before the supply on VREG_IN_HV is present.

Software controls the output voltage.

9.6 Voltage Regulator Enable

All the regulators are enabled, except the USB linear regulator, by taking the VREG_EN pin above 1V. The regulators are also controlled by software.

The VREG_EN pin is tolerant of voltages up to the voltage on VREG_IN_HV. The VREG_EN pin is pulled down internally.

9.7 Power Sequencing

CSR recommends that the power supplies are all powered at the same time. The order of powering the supplies relative to the I/O supply, VDD_PADS to VDD_HOST, is not important. If the I/O supply is powered before VDD_DIG, all digital I/Os are weak pull-downs irrespective of the reset state.

9.8 Reset

The reset function is internally tied to the VREG_EN pin. CSR8311 QFN is reset from several sources:

- RST# pin
- Power-on reset
- Via a software-configured watchdog timer

The RST# pin is an active low reset. Assert the reset signal for a period >5ms to ensure a full reset. The RST# pin is pulled down internally until the VDD_DIG rail is turned on, then the pull switches to a strong pull up.

Important Note:

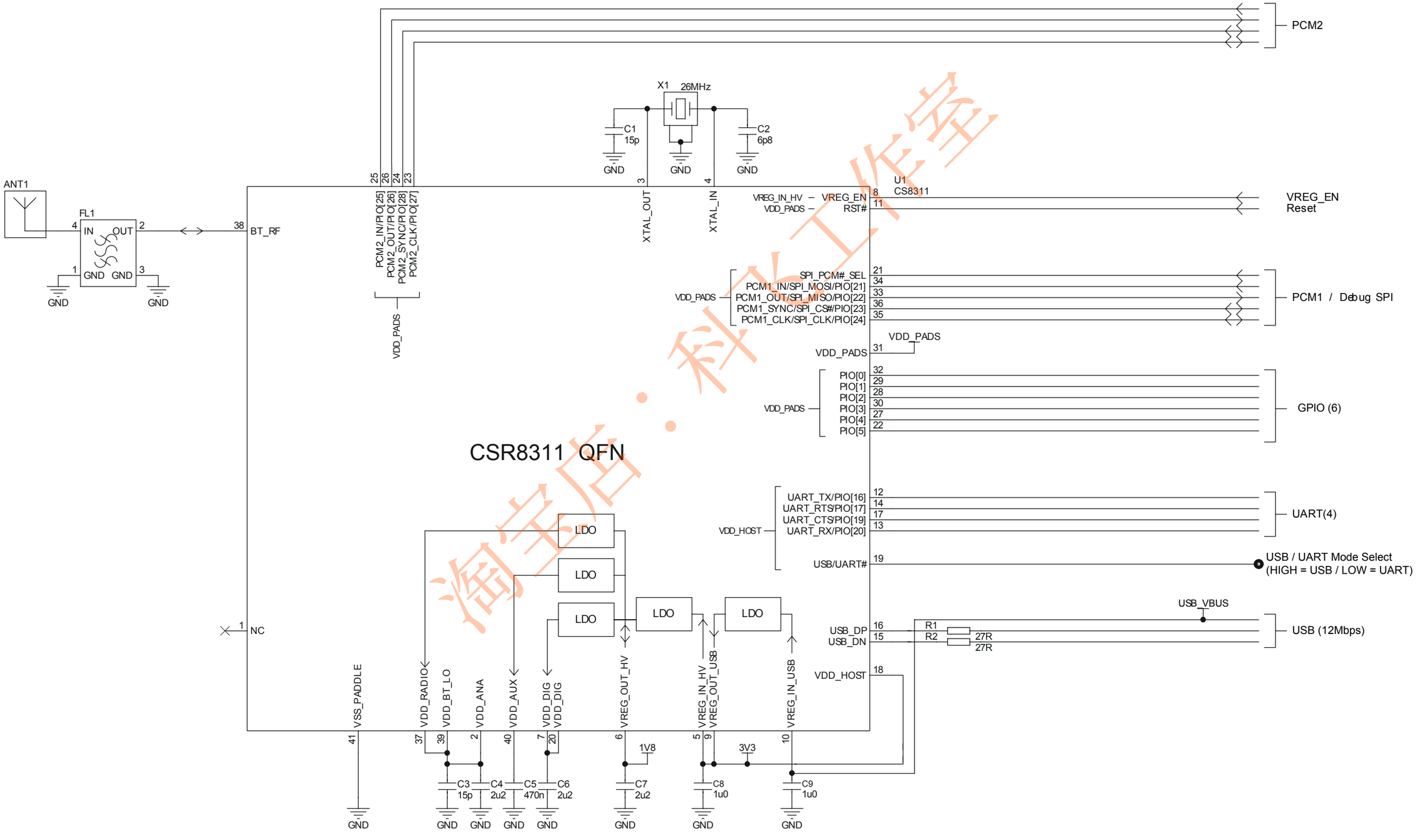
CSR does not recommend assertions of the reset of <5ms on the VREG_EN pin, as any glitches on this line can affect I/O integrity without triggering a reset.

A warm reset function is also available under software control. After a warm reset the RAM data remains available.

9.8.1 Digital Pin States on Reset

Pin Name/Group	I/O Type	No Core Supply Reset	Full Chip Reset
RST#	Digital input	Strong pull-down	N/A
SPI_CLK / PCM_CLK / PIO[24]	Digital bidirectional tristated	Weak pull-down	Weak pull-down
SPI_CS# / PCM_SYNC / PIO[23]	Digital bidirectional tristated	Weak pull-up (SPI) Weak pull-down (PCM)	Weak pull-up (SPI) Weak pull-down (PCM / PIO)
SPI_MISO / PCM_OUT / PIO[22]	Digital output tristated	Weak pull-down	Weak pull-down
SPI_MOSI / PCM_IN / PIO[21]	Digital input	Weak pull-down	Weak pull-down
PIO[5:0]	Digital bidirectional tristated	Weak pull-down	Weak pull-down

10 Example Application Schematic



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11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Rating	Min	Max	Unit
Storage temperature	-40	105	°C
VDD_HOST	3.1	3.6	V
VDD_PADS	1.2	3.6	V
Other terminal voltages	VSS - 0.4V	VDD + 0.4V	V

11.2 Recommended Operating Conditions

Rating	Min	Max	Unit
Operating temperature range	-40	85	°C
VDD_HOST	3.1	3.6	V
VDD_HOST (USB interface in use)	3.0	3.6	V
VDD_HOST (USB interface not in use)	1.2	3.6	V
VDD_PADS	1.2	3.6	V

11.3 Input/Output Terminal Characteristics

11.3.1 USB Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	4.20	5.0	5.75	V
Output voltage	-	3.3	-	V
Output current	-	-	150	mA

11.3.2 High-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	2.3	3.3	4.8	V
Output voltage	-	1.85	-	V
Temperature coefficient	-200	-	200	ppm/°C
Output noise (frequency range 100Hz to 100kHz)	-	-	0.4	mV rms
Settling time (settling to within 10% of final value)	-	-	5	µs
Output current	-	-	100	mA
Quiescent current (excluding load, I_{load} < 1mA)	-	40	-	µA
Low-power Mode				
Quiescent current (excluding load, I_{load} < 100µA)	-	18	-	µA

11.3.3 Low-voltage VDD_DIG Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Output voltage	0.90	-	1.25	V

11.3.4 Low-voltage VDD_AUX Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Output voltage	1.30	1.35	1.40	V

11.3.5 Low-voltage VDD_RADIO Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Output voltage	1.30	1.35	1.45	V

11.3.6 Digital

Digital Terminals	Min	Typ	Max	Unit
Input Voltage				
V_{IL} input logic level low	-0.4	-	0.4	V
V_{IH} input logic level high	0.7 x VDD	-	VDD + 0.4	V
Tr/Tf	-	-	25	ns
Output Voltage				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75 X VDD	-	-	V
Tr/Tf	-	-	5	ns
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	µA
Strong pull-down	10	40	150	µA
Weak pull-up	-5	-1.0	-0.33	µA
Weak pull-down	0.33	1.0	5.0	µA
C_I Input Capacitance	1.0	-	5.0	pF

11.3.7 Clock

Clock Source	Min	Typ	Max	Unit
External Clock				
XTAL_IN input resistance	30	-	-	kΩ
XTAL_IN input capacitance	-	-	4	pF

11.3.8 External Sleep Clock Specification

Sleep Clock			Min	Typ	Max	Units
Frequency[a]			30	32.768	35	kHz
Frequency tolerance[b]			-	-	250	±ppm
Duty cycle			30:70	50:50	70:30	%
Jitter Integrated rms jitter 10Hz to 20kHz		f_{ref} = 32.768kHz	-	-	20	ns rms
Phase noise	f_{ref} = 32.768kHz	1kHz offset	-	-	-100	dBc/Hz
		10kHz offset	-	-	-120	
Digital input, values as Section 11.3.6						

Table 11.1: Sleep Clock Specification

[a] Stability is most important as frequency is calibrated against the system clock.

[b] The frequency of the slow clock is periodically calibrated against the system clock, as a result the rate of change of the frequency is more important than the maximum deviation.

11.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 11.2 shows the ESD handling maximum ratings.

Condition	Class	Max Rating
Human Body Model AEC Q100-002	H1C	2kV (all pins)
Machine Model AEC Q100-003	M2	150V (I/O and Supply pins), 200V (BT_RF pin)
Charged Device Model AEC Q100-011	C3B	500V (all pins), 750V (corner pins)

Table 11.2: ESD Handling Ratings

12 Product Reliability Tests

The reliability tests in this section follow the tests outlined in the AEC-Q100 to Grade 3 requirements and were performed on CSR8311 QFN in QFN 40-lead 6 x 6 x 0.9mm 0.5mm pitch I/O. Samples are electrically tested at ambient, hot and cold temperature depending on the reliability test requirement.

This package qualification will (where moisture sensitivity preconditioning is required) use JEDEC J-STD-020, JESD22-A113, MSL3, using a Lead Free profile peaking at 260°C i.e. the finished product is allowed a maximum exposure to a 30°C/60% RH environment for 168 hours before mounting.

As part of CSR's automotive test program, customers will have access to the initial device reliability test report. They will also have access to a twice yearly reliability test report update for CSR products.

12.1 Automotive Die Test

Test	Test Conditions	Specification
ESD, Human Body Model	-	AEC Q100-002, Class H1C
ESD, Machine Model	-	AEC Q100-003, Class M2
ESD, Charged Device Model	-	AEC Q100-011, Class C3B
Latch-up	Ambient and T_{max}	AEC Q100-004
Early Life Failure Rate	125°C, VDD_{max}, 48 hours	AEC Q100-008
High Temperature Operating Life	125°C, VDD_{max}, 1000 hours	JEDEC JESD22-A108

12.2 Automotive Package Test

Test	Test Conditions	Specification
Moisture Sensitivity Preconditioning	30°C / 60% RH, 192 hours, 3 x reflow	JEDEC J-STD-020, JESD22-A113
Temperature Cycling	-65ºC to 150ºC, 500 cycles	JEDEC JESD22-A104
Autoclave	121ºC / 15psig, 96 hours	JEDEC JESD22-A102
Biased Highly Accelerated Stress Test (HAST)	130ºC / 85% RH, VDD_{MAX}, 96 hours	JEDEC JESD22-A110
High Temperature Storage Life	150ºC, 1000 hours	JEDEC JESD22-A103

13 Software

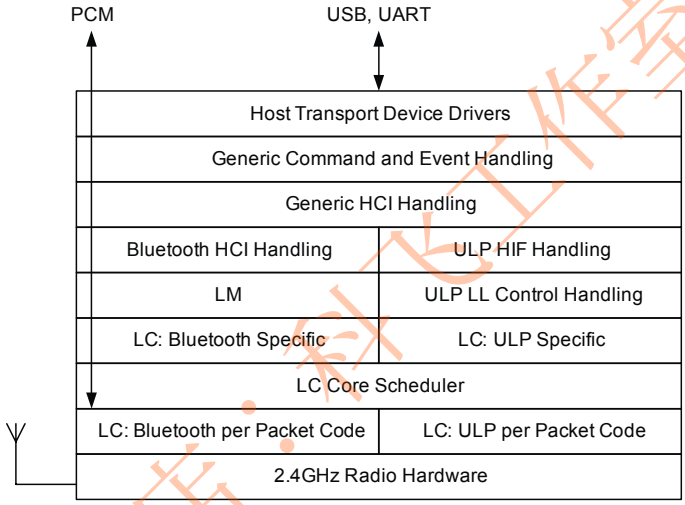
CSR8311 QFN:

- Is supplied with on-chip Bluetooth v4.0 specification qualified HCI stack firmware
- Can be shipped with CSR's off-chip software package, CSR Synergy, that runs on the host.

13.1 On-chip Software

13.1.1 BlueCore HCI Stack

Figure 13.1 shows an example implementation. An internal processor runs the Bluetooth stack up to the HCI. The host processor must provide all upper layers including the application.



G-TW-0005681.3.2

Figure 13.1: Example Firmware Architecture

13.1.1.1 Latest Features of the HCI Stack

CSR8311 QFN is qualified to Bluetooth v4.0 specification. This introduces the following features:

- Generic Alternate MAC/PHY (AMP)
- Generic Test Methodology for AMP
- 802.11 Protocol Adaptation Layer
- Enhanced Power Control
- Enhanced USB and SDIO HCI Transports
- HCI Read Encryption Key Size command
- Unicast Connectionless Data

For Bluetooth v3.0 + HS operation a separate 802.11 IC is used in conjunction with CSR8311 QFN.

13.2 Off-chip Software

13.2.1 CSR Synergy

CSR Synergy is a product from CSR that aids software development. It integrates all Host software for the wireless technologies into one package and can support Bluetooth, Bluetooth low energy, Wi-Fi, eGPS, FM TX/RX, NFC and UWB as Figure 13.2 shows.

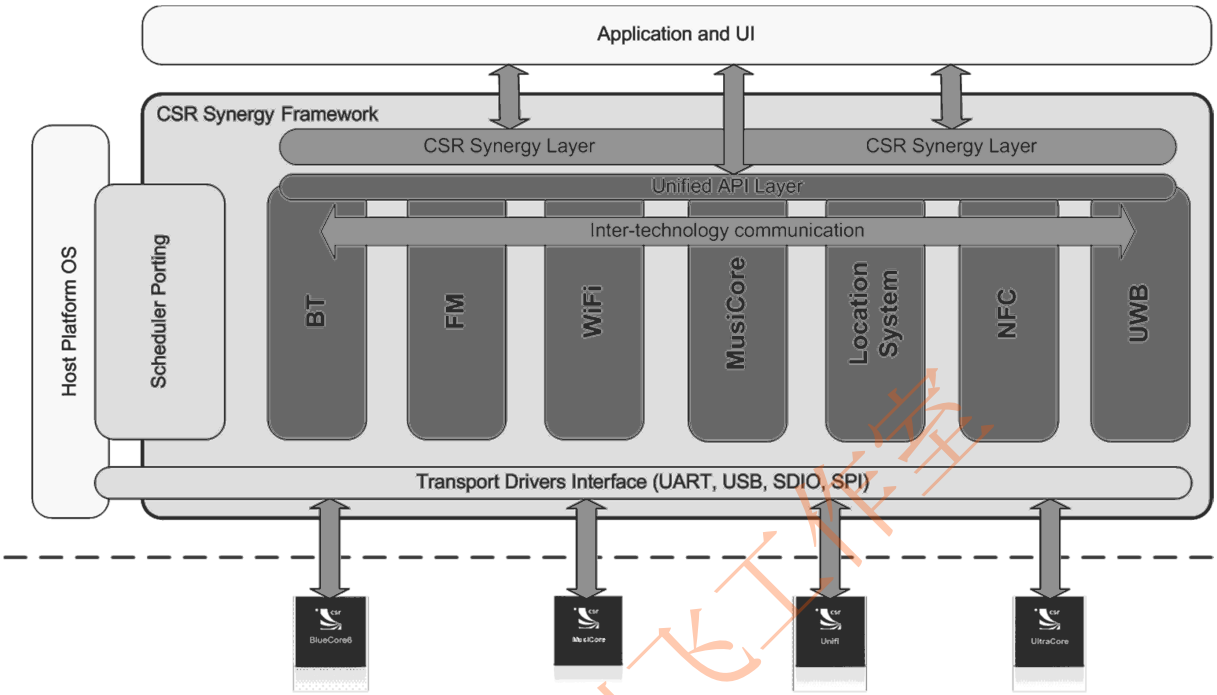


Figure 13.2: CSR Synergy Framework

Each technology in CSR Synergy is released as an individual component running in the common environment, the CSR Synergy Framework. This framework operates as a virtual OS for the components. Technologies can be removed and added easily to fit the hardware configuration, leaving no overhead in terms of MIPS and memory usage when a technology is not used.

See http://www.csr.com/products/19/csr-synergy for more information.

13.2.2 Enhanced Application Software for PC Environments

CSR8311 QFN contains CSR's Enhanced BlueCore VM Application software designed for PC environments:

- LED control:
  - Support for a configurable LED drive indicating Bluetooth radio operation
  - Configurable LED flash patterns for each radio state
- Hardware RF kill:
  - Typically for Flight Mode applications, this disables RF activity depending on a PIO state
- Software RF kill:
  - Typically for Flight Mode applications, this disables RF activity using HCI commands from the USB host
  - State is optionally maintained through reboot

For more information see *Enhanced BlueCore Application for PC Environments*.

14 CSR Green Semiconductor Products and RoHS Compliance

CSR confirms that CSR Green semiconductor products comply with the following regulatory requirements:

- Restriction on Hazardous Substances directive guidelines in the EU RoHS Directive 2002/95/EC. This includes compliance with the requirements for Deca BDE, as per removal of exemption, implementation date 01-Jul-08

  EU REACH, Regulation (EC) No 1907/2006:
  - List of substances subject to authorisation (Annex XIV)
  - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations and articles (Annex XVII). This Annex now includes requirements that were contained within EU Directive, 76/769/EEC. There are many substance restrictions within this Annex, including, but not limited to, the control of use of Perfluorooctane sulfonates (PFOS).
  - Substances identified on candidate list as Substances of Very High Concern (SVHC), 53 substances as per update published 20 June 2011.
- EU Commission Decision 2009/251/EC:
  - Products containing dimethylfumarate (DMF) are not placed or made available on the market.
- EU Packaging and Packaging Waste, Directive 94/62/EC
- Montreal Protocol on substances that deplete the ozone layer
- Global Automotive Declarable Substance List (GADSL)

Additionally, Table 14.1 shows that CSR Green semiconductor products are free from bromine, chlorine or antimony trioxide and other hazardous chemicals.

Material	Maximum Allowable Amount
Cadmium (Cd)	100ppm
Lead (Pb)	1000ppm (solder), 100ppm (plastic)
Mercury (Hg)	1000ppm
Hexavalent-Chromium (Cr VI)	1000ppm
Polybrominated biphenyls (PBB)	1000ppm
Polybrominated diphenyl ethers (PBDE)	1000ppm
Bromine, Chlorine	900ppm, <1500ppm combined
Antimony Trioxide (Sb_2O_3)	900ppm
Benzene	1000ppm
Beryllium and compounds (other than Beryllium Oxide (BeO)	1000ppm
Halogenated Diphenyl Methanes (Monomethyltetrachloro Diphenyl Methane (CAS# 76253-60-6), Monomethyldichloro Diphenyl Methane (CAS# 81161-70-8), Monomethyldibromo Diphenyl Methane (CAS# 99788-47-8)	1000ppm
Red phosphorous	1000ppm
1,1,1-trichloroethane	Banned

Material	Maximum Allowable Amount
Aliphatic CHCs (chlorohydrocarbons)	Banned
Benzotriazole (2-3',5'-Di-tert-butyl-2'-hydroxyphenyl)	Banned
Beryllium Oxide	Banned
Chlorinated paraffin (including short chain chlorinated paraffins – carbon chain length 10-13 and medium chain chlorinated paraffins – carbon chain length 14-17)	Banned
Formaldehyde (Banned in wooden, adhesive and plastic products)	Banned as described
Hydrofluorocarbon (HFC)	Banned
NPs (nonylphenols) and NPEs (nonylphenol ethoxylates) (Banned in textile, leather, metal, pulp and paper parts)	Banned as described
Organic tin compounds	Banned
Perfluorocarbon (PFC)	Banned
Polychlorinated napthalenes (PCN)	Banned
Polychlorinated terphenyls (PCT)	Banned
Polychlorinated biphenyls (PCB)	Banned
Polyvinyl Chloride (PVC)	Banned
Sulfur hexafluoride	Banned
Tetrachloromethane (CAS# 56-23-5)	Banned
Asbestos	Banned as intentionally introduced
Phthalates	Banned as intentionally introduced
Radioactive substances	Banned as intentionally introduced: reportable
Tributyl tin (TBT) / Triphenyl tin (TPT) / Tributyl Tin Oxide (TBTO) Dibutyl Tin (DBT) and Dioctyl Tin Compounds (DOT)	Banned as intentionally introduced

Table 14.1: Chemical Limits for Green Semiconductor Products

Products and shipment packaging are marked and labelled with applicable environmental marking symbols in accordance with relevant regulatory requirements.

CSR has defined this Green standard based on current regulatory and customer requirements. For more information contact product.compliance@csr.com.

15 Ordering Information

Device	Package			Order Number
	Type	Size	Shipment Method	
CSR8311A08	QFN 40-lead Green	6 x 6 x 0.9mm, 0.5mm pitch	Tape and Reel	CSR8311A08-AQQD-R

Note:

CSR8311 QFN is a ROM-based device where the product code has the form CSR8311Axx. xx is the specific ROM-variant.

Minimum order quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

To contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts.

16 Tape and Reel Information

For tape and reel packing and labeling see *IC Packing and Labelling Specification*.

16.1 Tape Orientation

The general orientation of the QFN in the tape is as shown in Figure 16.1.

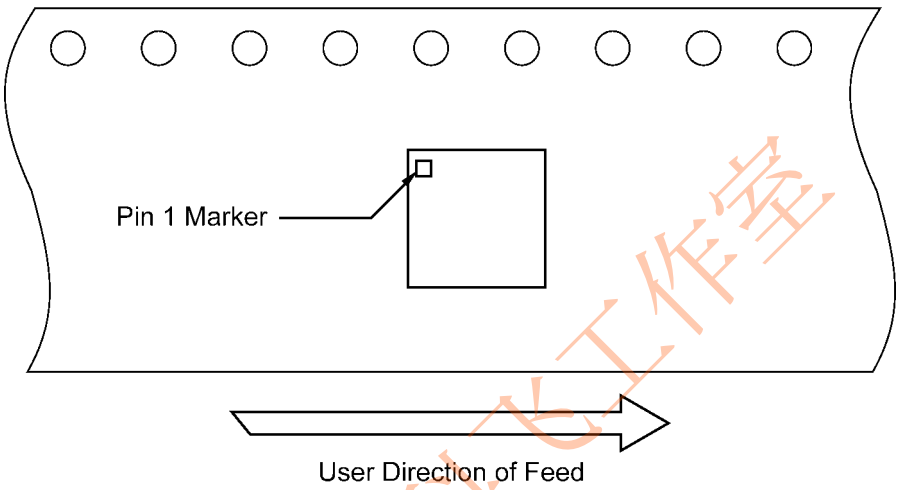


Figure 16.1: Tape and Reel Orientation

16.2 Tape Dimensions

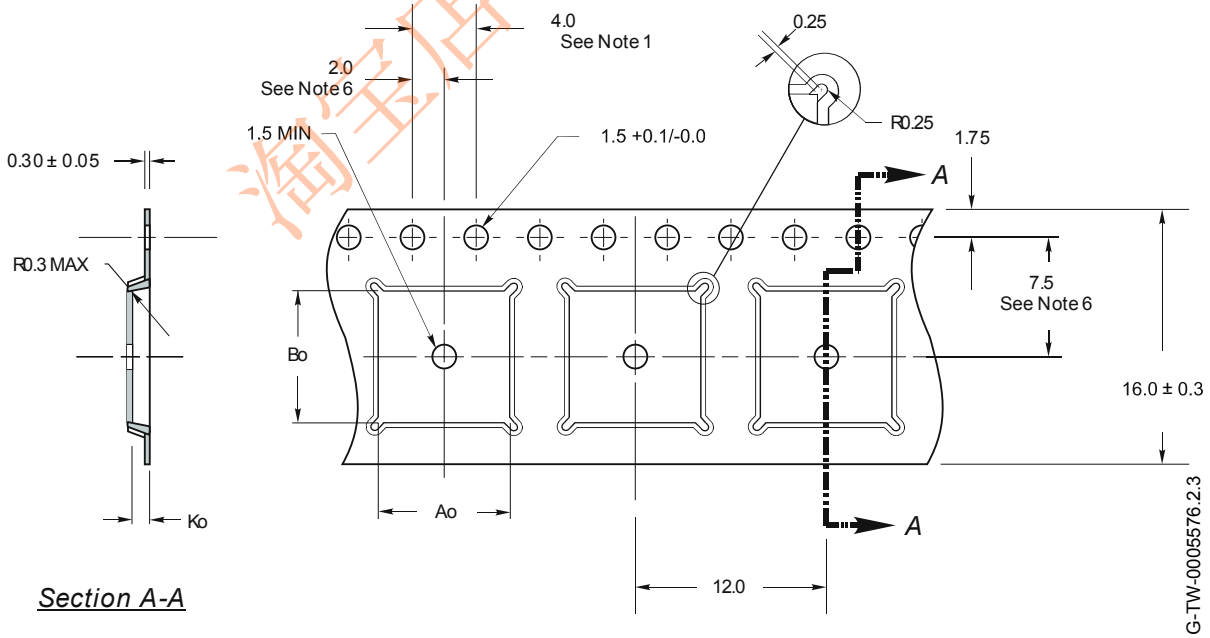


Figure 16.2: Tape Dimensions

A_0	B_0	K_0	Unit	Notes
6.3	6.3	1.1	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.02 2. Camber not to exceed 1mm in 100mm 3. Material: PS + C 4. A_0 and B_0 measured as indicated 5. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier 6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

16.3 Reel Information

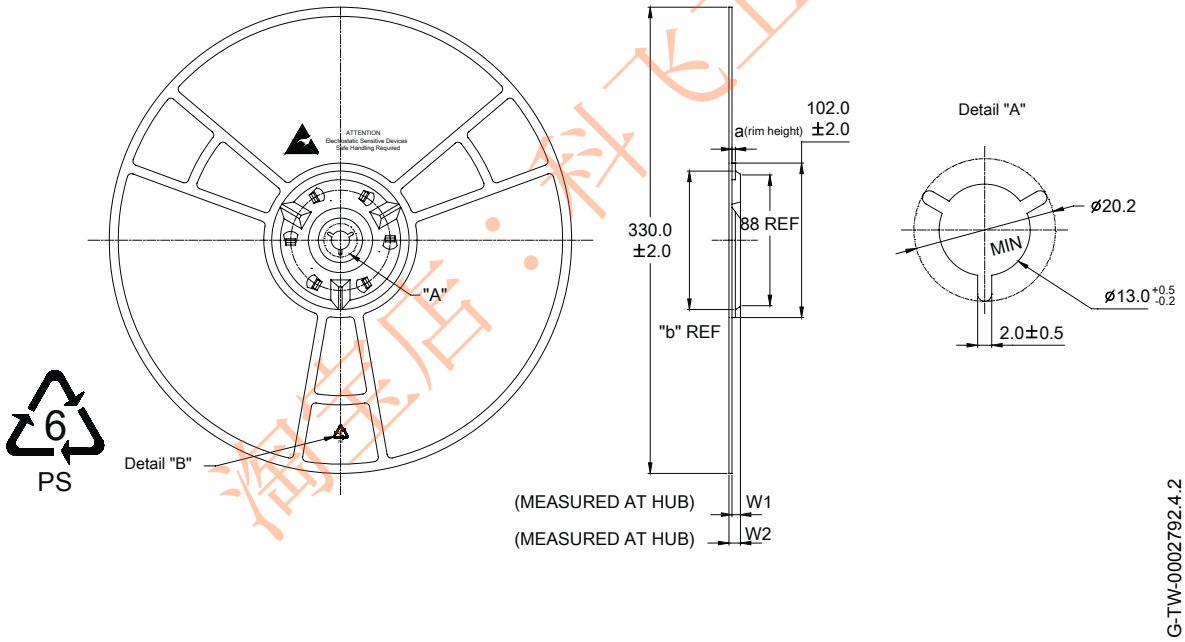


Figure 16.3: Reel Dimensions

Package Type	Nominal Hub Width (Tape Width)	a	b	W1	W2 Max	Units
6 x 6 x 0.9mm QFN	16mm	4.5	98.0	16.4 (3.0/-0.2)	19.1	mm

17 Document References

Document	Reference, Date
BCCMD Commands	CS-101482-SP (bcore-sp-005)
BlueCore Audio API Specification	CS-209064-DD
BlueCore Bluetooth/IEEE 802.11 Coexistence Application Note	CS-207808-AN
Bluetooth and USB Design Considerations	CS-101412-AN
CSR8311 Clock Application Note	CS-218819-AN
CSR8311 QFN Automotive Performance Specification	CS-219331-SP
Enhanced BlueCore Application for PC Environments	CS-200947-AN
Environmental Compliance Statement for CSR Green Semiconductor Products	CB-001036-ST, 27 September 2007
Global Automotive Declarable Substance List (GADSL)	GADSL Version 1.1, 2011
HQ Commands	CS-101677-SP (bcore-sp-003)
IC Packing and Labelling Specification	CS-112584-SP
Selection of I²C EEPROMS for Use with BlueCore	CS-101518-AN (bcore-an-008)
Specification of the Bluetooth System	v4.0, 17 December 2009
Stress Qualification For Integrated Circuits (base document only with no test methods) *Charged Device Model (CDM) Electrostatic Discharge Test* *Human Body Model (HBM) Electrostatic Discharge Test* *Machine Model (MM) Electrostatic Discharge Test*	AEC-Q100, Rev-G base AEC-Q100-011, Rev-B AEC-Q100-002, Rev-D AEC-Q100-003, Rev-E
Typical Solder Reflow Profile for Lead-free Devices	CS-116434-AN

Terms and Definitions

Term	Definition
3G	3rd Generation of mobile communications technology
802.11™	WLAN specification defined by a working group within the IEEE
µ-law	Audio companding standard (G.711)
A-law	Audio companding standard (G.711)
A2DP	Advanced Audio Distribution Profile
AC	Alternating Current
ADC	Analogue to Digital Converter
AES	Advanced Encryption Standard
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AMP	Alternate MAC/PHY
balun	balanced/unbalanced interface or device that changes a balanced output to an unbalanced input or vice versa
BCCMD	BlueCore Command
BCSP	BlueCore Serial Protocol
BIST	Built-In Self-Test
BlueCore®	Group term for CSR's range of Bluetooth wireless technology ICs
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
CDMA	Code Division Multiple Access
codec	Coder decoder
CRC	Cyclic Redundancy Check
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1 mW
DC	Direct Current
DDS	Direct Digital Synthesis

Term	Definition
e.g.	*exempli gratia*, for example
EBU	European Broadcasting Union
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
eGPS®	enhanced GPS
eSCO	Extended SCO
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
etc	*et cetera*, and the rest, and so forth
FM	Frequency Modulation
GCI	General Circuit Interface
GSM	Global System for Mobile communications
H4DS	H4 Deep Sleep
HCI	Host Controller Interface
I²C	Inter-Integrated Circuit Interface
I²S	Inter-Integrated Circuit Sound
i.e.	*Id est*, that is
I/O	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency
IPC	See www.ipc.org
IQ Modulation	In-Phase and Quadrature Modulation
ISDN	Integrated Services Digital Network
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
Kb	Kilobit
KB	Kilobyte
LC	An inductor (L) and capacitor (C) network
LDO	Low (voltage) Drop-Out
LED	Light-Emitting Diode
LM	Link Manager

Term	Definition
LNA	Low Noise Amplifier
LSB	Least Significant Bit (or Byte)
MAC	Medium Access Control
Mb	Megabit
MB	Megabyte
Mbps	Megabits per second
MCU	MicroController Unit
MIPS	Million Instructions Per Second
MLC	Multilayer Ceramic
MMU	Memory Management Unit
NC	Not Connect
NFC	Near Field Communication
NSMD	Non Solder Mask Defined
OS	Operating System
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PHY	Physical (layer)
PIO	Programmable Input/Output, also known as general purpose I/O
pk-pk	peak-to-peak
plc	Public Limited Company
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
PU	Pull-up
RAM	Random Access Memory
RF	Radio Frequency
RH	Relative Humidity
RISC	Reduced Instruction Set Computer

Term	Definition
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
RS-232	Recommended Standard-232, a TIA/EIA standard for serial transmission between computers and peripheral devices (modem, mouse, etc.)
RSSI	Received Signal Strength Indication
RTS	Request To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented
SDIO	Secure Digital Input/Output
SIG	(Bluetooth) Special Interest Group
SPDIF	Sony/Philips Digital InterFace (also IEC 958 type II, part of IEC-60958). An interface designed to transfer stereo digital audio signals between various devices and stereo components with minimal loss.
SPI	Serial Peripheral Interface
TCXO	Temperature Compensated crystal Oscillator
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
UWB	Ultra-wideband
VCO	Voltage Controlled Oscillator
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
Wi-Fi®	Wireless Fidelity (IEEE 802.11 wireless networking)