30V 3.5A 500KHz Synchronous Step-Down Regulator

## CST2335 Features

- Wide Input Voltage Range: 6V ~ 30V
- 3.5A output current capability
- Fixed 500KHz Switching Frequency
- Output Adjustable from 0.925V
- Internal Soft start
- Built-in Over Current Limit
- No Schottky Diode Required
- Under Voltage Protection
- Over Voltage Protection
- Over Current Protection
- Short Circuit Protection
- Over Thermal Protection
- Available in ESOP8 Package
- -40°C to +85°C Temperature Range

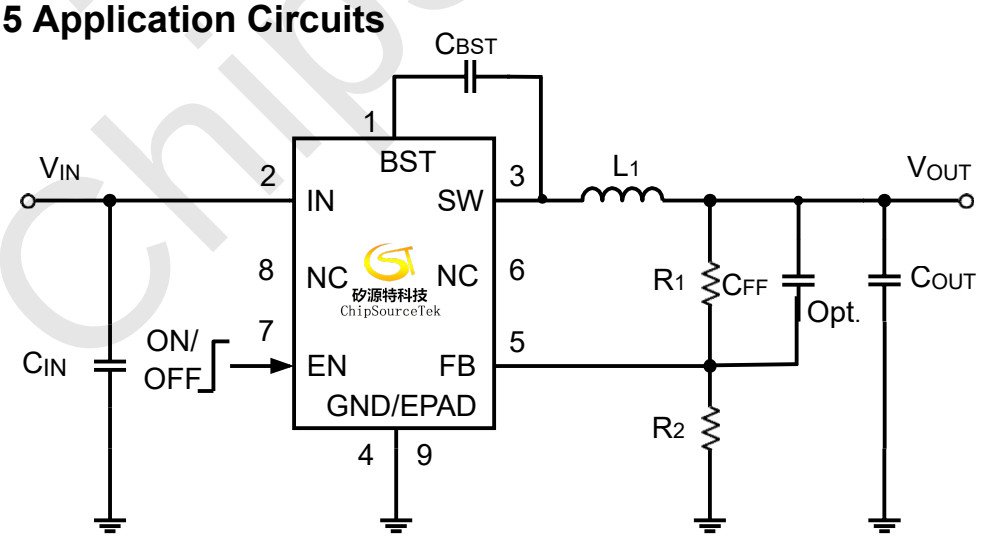
## CST2335 Application

- Automotive Systems
- Security Monitoring Camera
- Network Terminal Equipment
- Industrial Power Systems

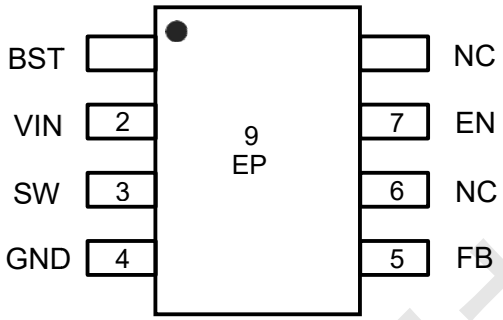
## CST2335 Description

The CST2335 is synchronous converters with an input-voltage range of 6V to 30V. It has an integrated low-side switching FET that eliminates the need for an external diode which reduces component count. Efficiency is maximized through the integrated 85-mΩ and 60-mΩ MOSFETs, low IQ and pulse skipping at light loads. Using the enable pin, the shutdown supply current is reduced to 2 μA. This step-down (buck) converter provides accurate regulation for a variety of loads with a well regulated voltage reference that is 1.5% over temperature.Cycle-by-cycle current limiting on the high-side MOSFET protects the CST2335 in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. A low-side sinking current-limit turns off the low-side MOSFET to prevent excessive reverse current.Hiccup protection is triggered if the overcurrent condition continues for longer than the preset time. Thermal shutdown disables the device when the die temperature exceeds the threshold and enables the device again after the built-in thermal hiccup time.

## CST2335 Application Circuits



## CST2335 Pin Configuration




## CST2335 Pin Description

| Pin | Name | Function |
|---|---|---|
| 1 | BST | Boot-Strap Pin. Supply high side gate driver. Decouple this pin to SW pin with10nF ceramic cap. |
| 2 | VIN | Power Supply Pin |
| 3 | SW | Switch Output Pin. Connect using a wide PCB trace. |
| 4 / 9 | GND / EP | System Ground. |
| 5 | FB | Output Feedback Pin. Connect this pin to the center point of the output resistor divider to program the output voltage |
| 6 | NC | NC |
| 7 | EN | Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode. |
| 8 | NC | NC |

## CST2335 Order Information

| Model | Marking | Description | Package | T/R Qty |
|---|---|---|---|---|
| CST2335 | **** | ST2335 Synchronous Step-Down Regulator; 30V,3.5A,500KHz, $V_{FB}$ 0.925V | ESOP-8 | 3,000 PCS |

**Note** :For marking information,contact our sales representative directly

**All AISIS parts are Pb-Free and adhere to the RoHS directive.**

## CST2335 Absolute Maximum Ratings(1)(2)

| Item | Min | Max | Unit |
|---|---|---|---|
| Supply Input Voltage | -0.3 | 38 | V |
| SW,EN Voltage | -0.3 | $V_{IN}$+0.3 | V |
| FB, BS-SW Voltage | -0.3 | 4 | V |
| Operating junction temperature .$T_J$ | -40 | 150 | °C |
| Power dissipation | Internally Limited | | |
| Lead Temperature (Soldering, 10 sec.) | 300 | | °C |
| Storage Temperature Range. Tstg | -65 | 150 | °C |
| Dynamic SW Voltage in 10ns Duration | GND-5V | VIN+3V | V |
| Package Thermal Resistance $\theta_{JA}$ | 40 | | °C/W |
| Package Thermal Resistance $\theta_{JC}$ | 50 | | °C/W |

Note1: Exceeding these ratings may damage the device.

Note2: The device is not guaranteed to function outside of its operating conditions.

## CST2335 ESD Ratings

| Item | Description | Value | Unit |
|---|---|---|---|
| $V_{(ESD-HBM)}$ | Human Body Model (HBM)<br>ANSI/ESDA/JEDEC JS-001-2014<br>Classification, Class: 2 | ±2000 | V |
| $V_{(ESD-CDM)}$ | Charged Device Model (CDM)<br>ANSI/ESDA/JEDEC JS-002-2014<br>Classification, Class: C0b | ±200 | V |
| $I_{LATCH-UP}$ | JEDEC STANDARD NO.78E<br>APRIL 2016Temperature Classification,<br>Class: I | ±150 | mA |

## CST2335 Recommended Operating Conditions(1)

| Item | Min | Max | Unit |
|---|---|---|---|
| Input Voltage | 6 | 30 | V |
| Output current | 0 | 3.5 | A |
| Operating junction temperature | –40 | 125 | °C |
| Operating Temperature Range | -40 | 85 | °C |

Note (1): All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

## CST2335 Electrical Characteristics

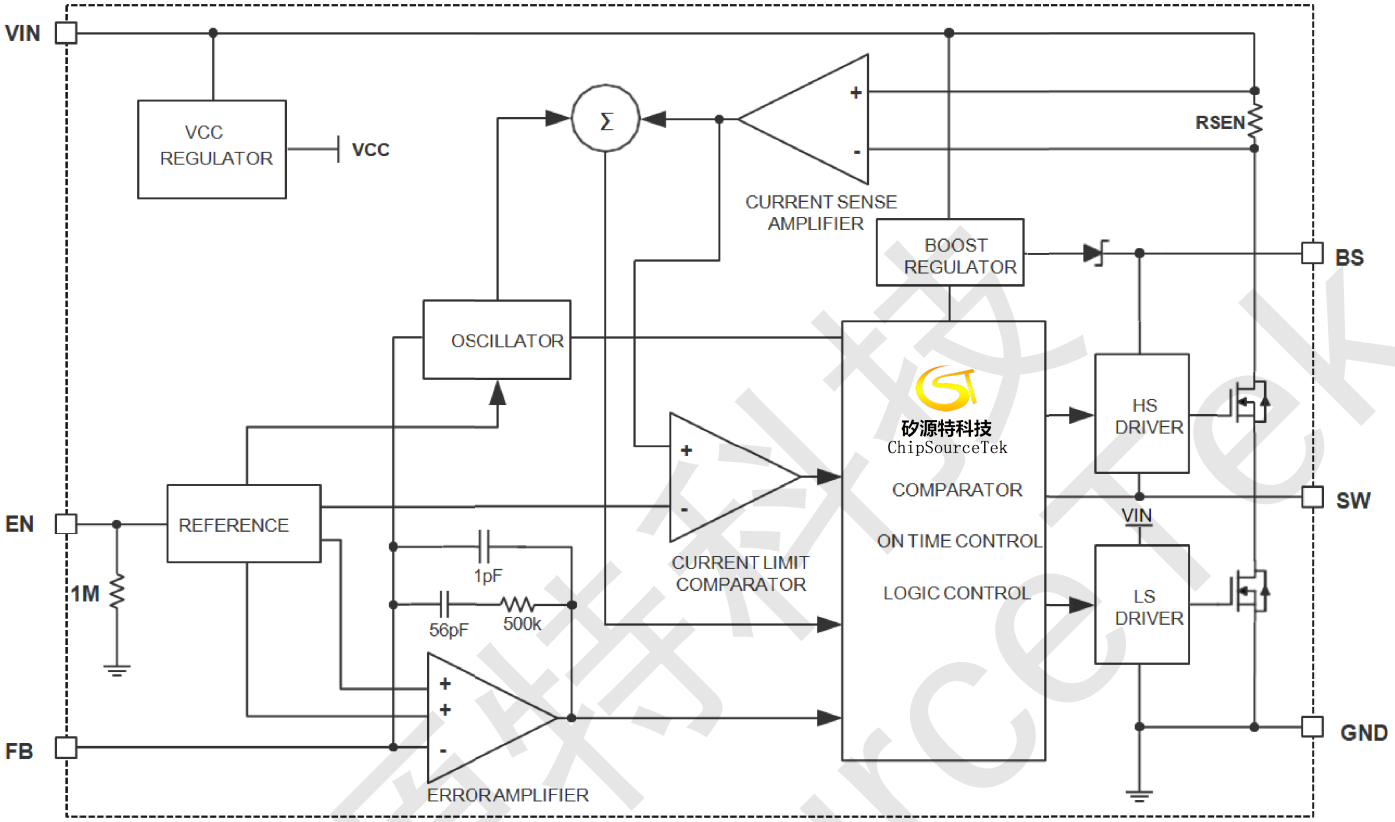
($V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 10μH, $C_{OUT}$ = 44μF, TA = 25°C, $I_{OUT}$ = 1A unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | 6 | | 30 | V |
| Input OVP Threshold | $V_{OVP}$ | | | | 38 | V |
| Input OVP Hysteresis | $V_{HYS}$ | | | 4 | | V |
| Input UVP Threshold | $V_{UVP}$ | | | | 5.3 | V |
| Input UVP Hysteresis | $V_{HYS}$ | | | 0.6 | | V |
| Standby Supply Current | $I_Q$ | $I_{OUT}$=0,$V_{FB}$=$V_{REF}$×105% | | 110 | | μA |
| Shutdown Supply Current | $I_{SHDN}$ | $V_{EN}$ = 0 | | 2 | | μA |
| EN Rising Threshold | $V_{EN\_R}$ | | | 1.2 | | V |
| EN Falling Threshold | $V_{EN\_F}$ | | | 1 | | V |
| Feedback Voltage | $V_{REF}$ | | | 0.925 | | V |
| FB Input Current | $I_{FB}$ | | -50 | | 50 | nA |
| Top FET RON | $R_{DSON}$ | | | 90 | | mΩ |
| Bottom FET RON | $R_{DSON}$ | | | 65 | | mΩ |
| Maximum Duty Cycle | $D_{MAX}$ | $V_{FB}$=0.925 | | | 93 | % |
| Min ON Time | $T_{ON\_MIN}$ | | | 50 | | ns |
| Min OFF Time | $T_{OFF\_MIN}$ | | | 100 | | ns |
| Turn On Delay | $T_{ON\_DLY}$ | From EN high to SW | | 180 | | μs |
| Soft-start Time | $T_{SS}$ | $V_{OUT}$ from 0 to 100% | | 1.5 | | ms |
| Switching Frequency | $F_{SW}$ | $V_{OUT}$=3.3V, CCM | | 500 | | kHz |
| Top FET Current Limit | $I_{LIM\_TOP}$ | | | 4.5 | | A |
| Bottom FET Current Limit | $I_{LIM\_BOT}$ | | | 4.5 | | A |
| Thermal Shutdown | $T_{SD}$ | | | 150 | | °C |
| Thermal Shutdown | $T_{HYS}$ | Duty = 30% | | 15 | | °C |

Note1: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note2: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

## CST2335 Function Block Diagram




## CST2335 FUNCTIONAL DESCRIPTION

CST2335 is a high efficiency, 500kHz synchronous step-down DC/DC regulator, which is capable of delivering up to 3.5A load current. It can operate over a wide input voltage range from 6V to 30V and integrate main switch and synchronous switch with very low RDS(ON) to minimize the conduction loss. CST2335 provides protection functions such as cycle by cycle current limiting and thermal shutdown protection.

### Internal Soft Start

CST2335 has an internal soft-start circuit that limits the in-rush current during startup. This allows the converters to gradually reach the steady-state operating point, thus reducing startup stresses and surges. During startup, the switch current limit is increased in steps.

The typical soft-start time is 1.5ms.

### OCP and SCP

If the high side power FET current gets higher than peak current limit threshold, the high side power FET will turn off and the low side power FET will turn on. If the low side FET current gets higher than valley current limit threshold, the low side FET will keep turning on until low side FET current decreases below the valley current limit threshold. So both peak and valley current are limited. If the load current continues to increase in these conditions, the output voltage will drop. When

the output voltage falls below 33% of the regulation level, the output short is detected and the IC will operate in hic-cup mode. The hic-cup on time is 2.5ms and hic-cup off time is 9ms. If the hard short is removed, the IC will return to normal operation.

### Enable and Adjusting UVLO

The EN pin has accurate rising and falling threshold, it provides programmable ON/OFF control by connecting an external resistor divider. Once the EN pin voltage exceeds the rising threshold, the device will start operation. If the EN pin voltage is pulled below the falling threshold, the regulator will stop switching and enter shutdown stat.

## CST2335Applications Information

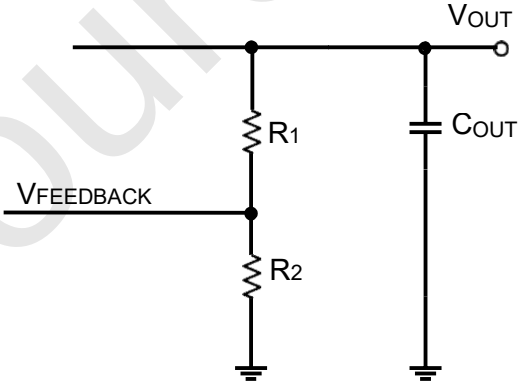
### Adjusting the Output Voltage

CST2335 require an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. CST2335 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider. A resistor divider from the output node to the feedback pin sets the output voltage. Recommend using 1% tolerance or better divider resistors. Start with fixed value for the R1 resistor and use Equation to calculate R2. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the feedback input current are noticeable.

$$V_{OUT} = V_{FEEDBACK} \times \frac{R1+R2}{R2}$$

Select R1 value then:

$$R2 = R1 \times \frac{V_{FEEDBACK}}{V_{OUT}-V_{FEEDBACK}}$$




### Inductor Selection

Use a inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, select an inductor with a DC resistance less than 15mΩ. For most designs, derive the inductance value from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_S}$$

Where ΔIL is the inductor ripple current. Choose aninductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use alarger inductor to improve efficiency.

## Input Capacitor Selection

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to both supply the AC current to the step-down converter and maintain the DC input voltage. For the best performance, use low ESR capacitors, such as ceramic capacitors with X5R or X7R dielectrics and small temperature coefficients. A 10μF capacitor is sufficient for most applications. The input capacitor requires an adequate ripple current rating because it absorbs the input switching. Estimate the RMS current in the input capacitor with:

$$I_{CIN} = I_{LOAD} \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

The worst-case condition occurs at $V_{IN} = 2\ V_{OUT}$, where:

$$I_{CIN} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. Place a small, high-quality, ceramic capacitor (0.1μF) as close to the IC as possible when using electrolytic or tantalum capacitors. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive input voltage ripple. Estimate the input voltage ripple caused by the capacitance with:

$$\Delta V_{IN} = \frac{I_{LOAD}}{F_S \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

## Output Capacitor Selection

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_S \times C_{OUT}}\right)$$

Where L is the inductor value and RESR is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_S^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The CST2335 can be optimized for a wide range of capacitance and ESR values.For the best performance, it is recommended to use X5R or a better grade ceramic capacitor with 16V rating and more than 44μF capacitance.

### Bootstrap Capacitor Selection

Connect a 100nF ceramic capacitor between the SW and BS pins for proper operation. Recommend using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 6.3V or higher voltage rating.

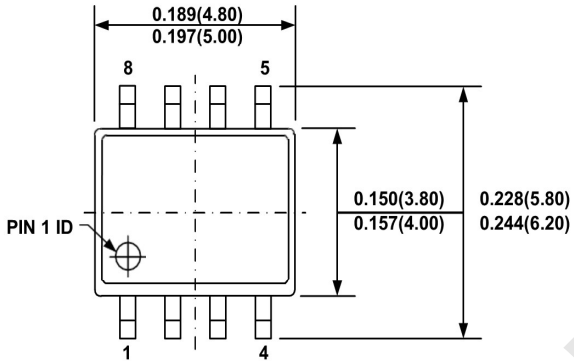
### PC Board Layout Consideration

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

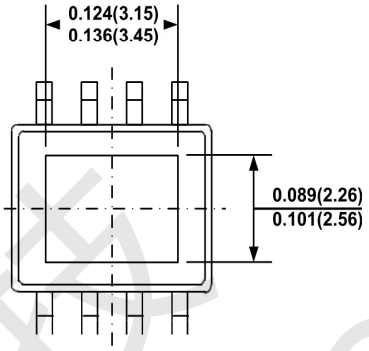
- Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the CIN input capacitor, to the regulator VIN terminal, to the regulator SW terminal, to the inductor then out to the output capacitor COUT and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to COUT and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of asmall localized top side plane that connects to GND.The inductor should be placed as close as possible to the SW pin and output capacitor.
- Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
- Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
- Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise

- Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

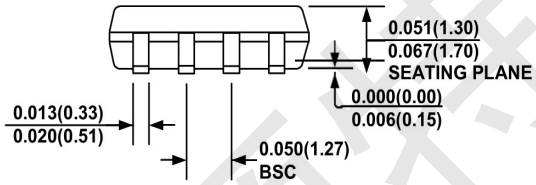
# PACKAGE OUTLINE DRAWING FOR 8-SOIC w/ EXPOSED PAD



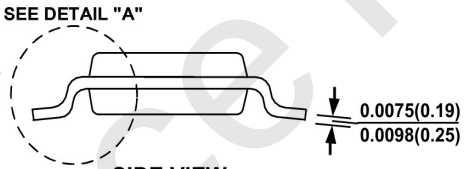

TOP VIEW



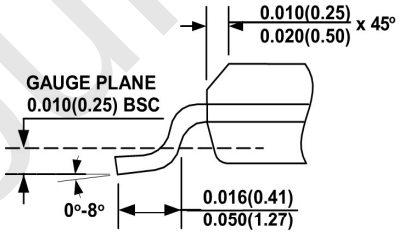

BOTTOM VIEW



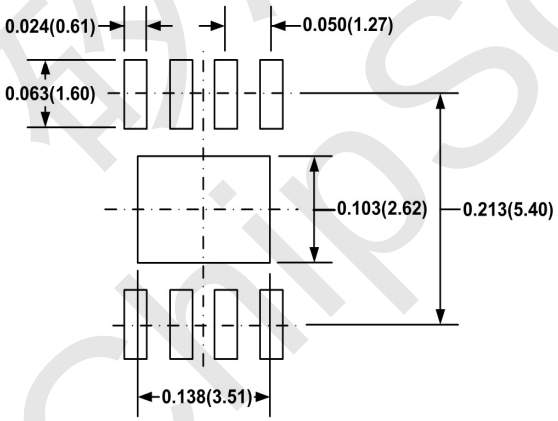

FRONT VIEW




SIDE VIEW




DETAIL "A"




RECOMMENDED LAND PATTERN

**NOTE:**

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.