



DATASHEET

CST510K5

Self-capacitive touch key controller



GENERAL DESCRIPTION

CST510K5 is a high-performance self-capacitor touch key controller that supports various self-capacitor key patterns and has excellent signal-to-noise ratio to achieve high reliability while maintaining ultra-low power consumption.

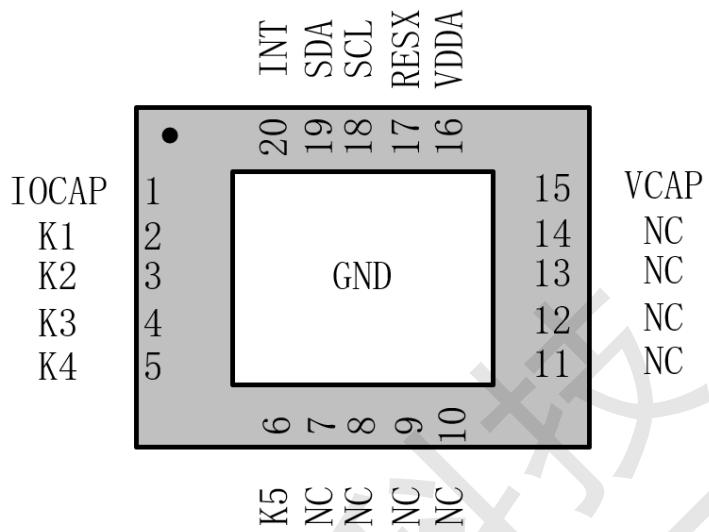
1 CST510K5 Features

1.1 Key features

- ◆ Highly sensitive self-capacitance detection technology
- ◆ Supported key number up to 5
- ◆ Support three work modes: Normal mode, Idle mode, Sleep mode
- ◆ The sleep mode power consumption is as low as 5uA, the Idle mode consumption is as low as 100uA, and the normal mode power consumption is as low as 1.2mA
- ◆ Auto calibration
- ◆ Supports I2C interfaces
- ◆ Support online programming
- ◆ Single power supply 2.7V to 5.5V
- ◆ Package: QFN20 3x3x0.55mm
- ◆ The CST510K5 typical applications are listed as follows:
 - Digital products
 - Household appliances, small appliances
 - Intelligent electronic toy
 - Instead of a switch



1.2 Pin layout



PIN Name	Description	Note
K1~K5	Touch key channels	
SCL/SDA	IIC	I2C clock input /I2C data input and output
RESX	Reset input	active low
INT	Interrupt output	External interrupt to the host
IOCAP	Connect 1uF capacitor	
VCAP	Connect 1uF capacitor	
VDDA	Power supply	2.7~5.5V, Connect 1-10uF capacitor



2 CST510KD Function Overview

2.1 Block diagram

The overall system block diagram of the CST510K5 is shown as Figure below.

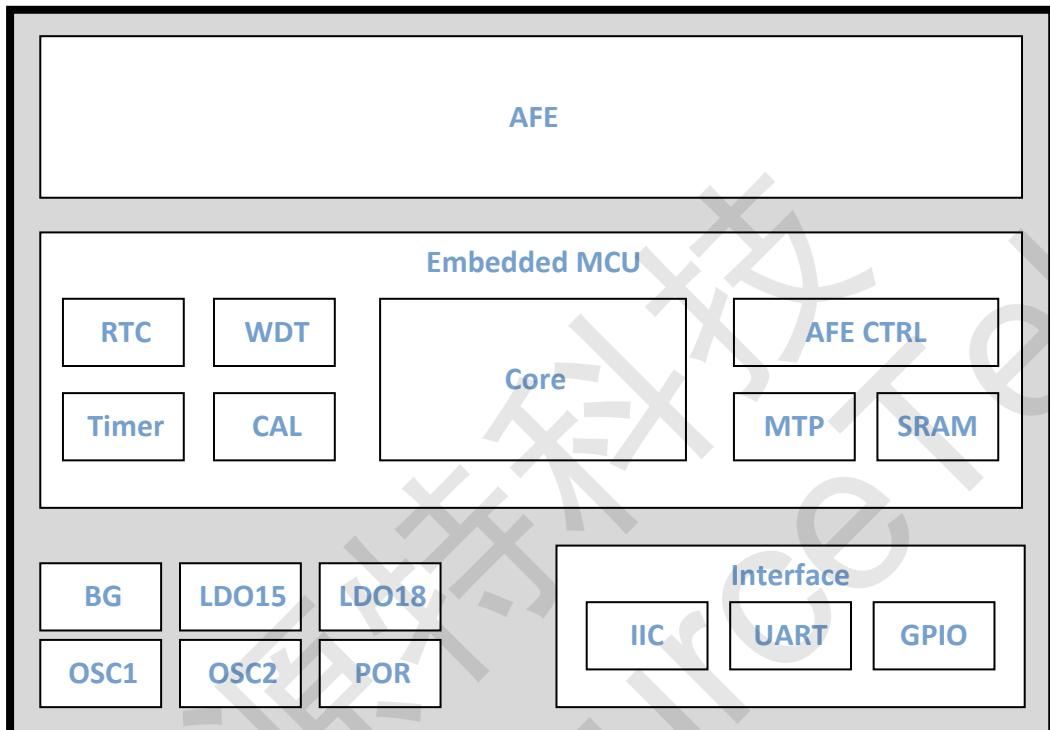


Figure: block diagram

2.1.1 AFE

AFE channels connect with key patterns, scan by sending AC signals to the patterns and process the received signals, which finally be converted by ADC and sent to MCU.

2.1.2 Interface

IIC is main communication interface which support slave mode only and support up to 400KHz transfer speed. Detail of IIC communication please refer to Chapter 3.

UART is normally used as debug function. It supports up to 1MHz baud rate.

GPIO (pins: “INT”, “SDA”, “SCL”) high level voltage can be configurated to 1.8V or VDDA by setting internal register. “INT” signal is used to inform HOST to get newest key states or just wakeup HOST.



2.1.3 Embedded MCU

Embedded MCU bases on a high efficiency core.

MTP is used to store firmware and run.

SRAM is for system use.

AFE CTRL module is the interface between MCU and AFE. User can configurate AFE CTRL registers to generate control signals to AFE. AFE also inform MCU current state through AFE CTRL module.

RTC works with OSC2. It is used to support low-power scan mode, in which OSC1 can be shut down and AFE scan is triggered automatically.

CAL module is designed for speeding up data process.

Timer can be used to generate a precise latency.

WDT is used to ensure the stability of chip when in operation.

Signal processing algorithms are implemented by MCU to detect the key states reliably and efficiently. Communication protocol is also implemented by MCU to exchange key states or control information with HOST.

2.2 Work modes

There are three work modes available:

- Normal mode
- Idle mode
- Sleep mode

Work modes switching conditions are shown as below:

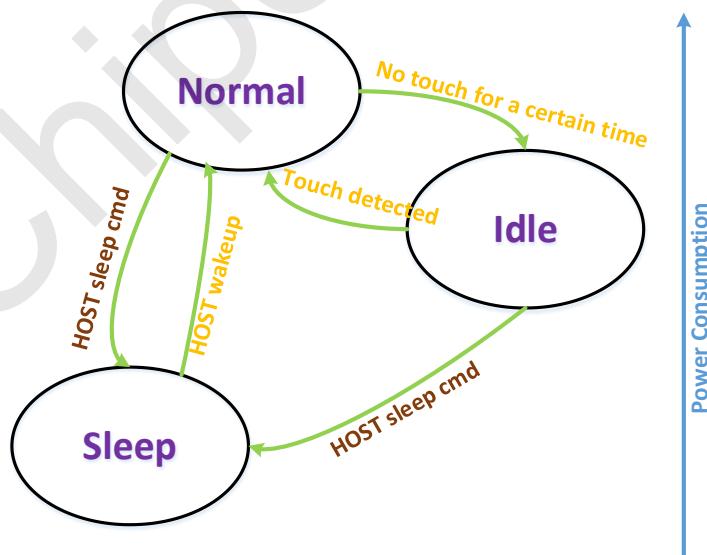


Figure: Work modes



2.2.1 Normal mode

In normal mode, AFE scans the key patterns in a configurable scan-rate, MCU will detect touch states of each key and report.

2.2.2 Idle mode

When there is no touch on any key for a configurable interval, MCU automatically switch into idle mode. In idle mode, AFE scans the key patterns with a relatively lower scan-rate (also configurable) to reduce power consumption. Majority of the algorithms will be canceled, and only simple detection algorithms is retained to detect if there is a touch. Once a touch on any key is detected, MCU will immediately switch back to normal mode.

2.2.3 Sleep mode

In sleep mode, MCU enters ultra low-power mode and can be wakeup by IIC. The power consumption in this mode is extremely small, can greatly extend the standby time of portable devices.



3 Communication Interface

The connection from host to CST510K5 is shown as below:

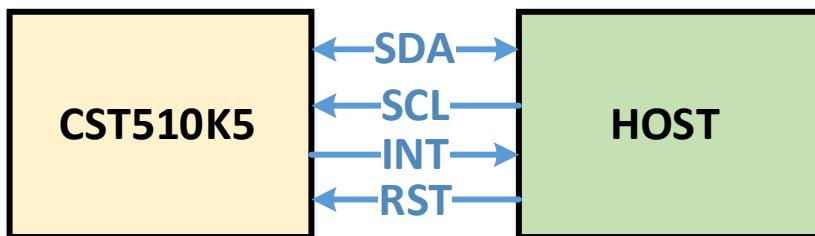


Figure: interface

INT signal is used to inform HOST that there are key states changed and states information is ready. INT signal idle level can be configurated as low or high. When there are key states changed, INT signal is set to active level until HOST read the states information. If HOST haven't read the states information, INT signal would retain active level until next key states update. So, HOST can use either level or edge trigger-mode interrupt to respond INT signal.

RST signal is used to reset CST510K5 by setting low level for a while then setting back to high level.

IIC interface is used to transfer data between CST510K5 and HOST. Write/Read protocols are shown as below:



Figure: IIC write/Read operation



Figure: Host write CST510K5 register

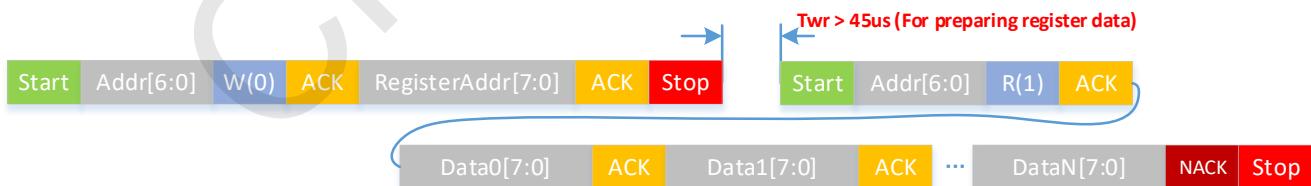


Figure: Host read CST510K5 register



4 CST510K5 Electrical Specifications

4.1 Absolute maximum ratings

Table: Absolute Maximum Ratings

Characteristics	Sym.	Min.	Max	Unit	Test Condition
Supply Voltage	VDDA	-0.3	5.5	V	
Storage temperature Range	T _{Str}	-55	150	°C	

4.2 Recommended operating condition

Table: Recommended operation condition

Item	Sym.	Min	Typ.	Max	Unit	Condition
Power-supply voltage	VDDA	2.7	3.3	5.5	V	
Operating Temperature Range	T _{Opr}	-40		85	°C	

4.3 AC characteristics

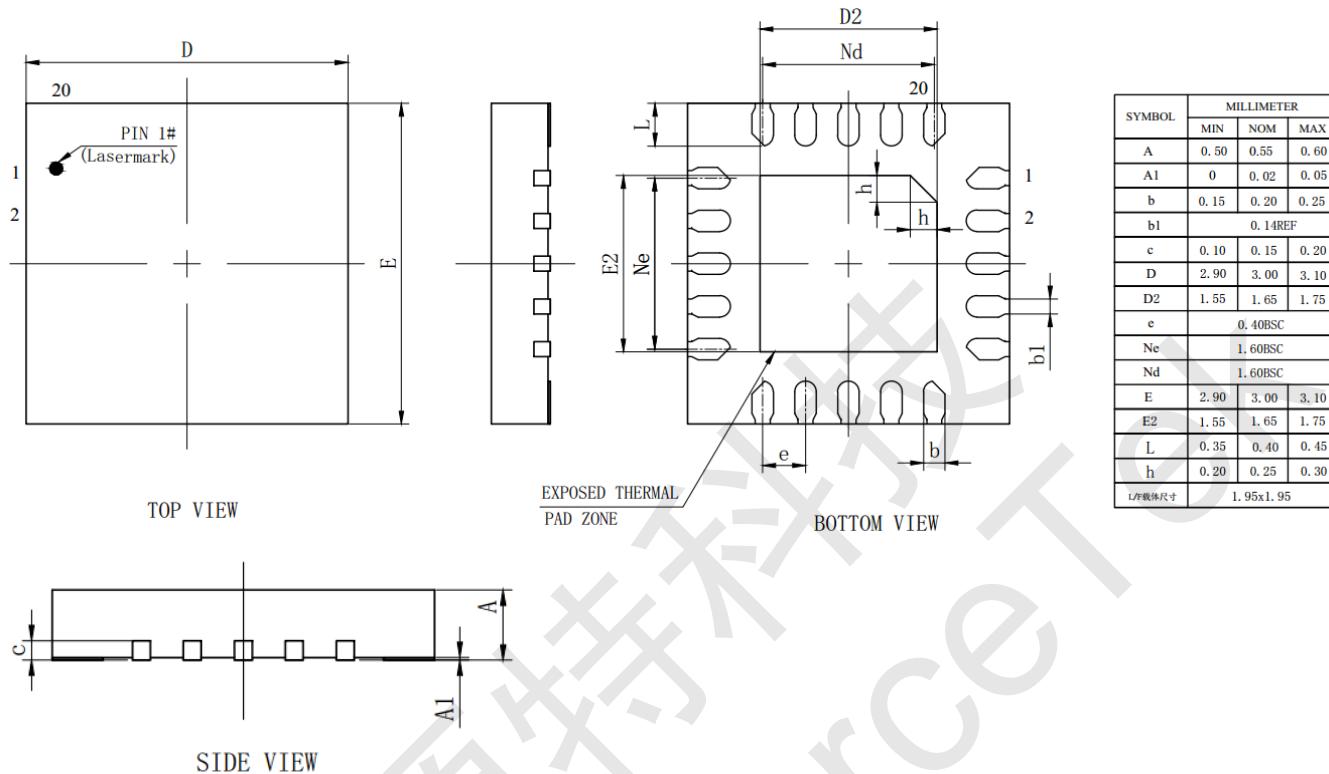
Table: AC Characteristics

Parameter	Sym.	Min	Typ.	Max	Unit	Condition
Digital inputs/outputs						
Input high voltage	VIH	0.7 × IOVCC		IOVCC	V	
Input low voltage	VIL	GND		0.3 × IOVCC	V	
Output high voltage	VOH	0.7 × IOVCC		IOVCC	V	
Output low voltage	VOL	GND		0.3 × IOVCC	V	

NOTE: IOVCC=VDDA or 1.8V



5 CST510K5 Package



6 Ordering information

Product Series	Package Type	Packing Method	Ordering Number	Minimum Order Quantity
CST510K5	20-pin 3x3x0.55mm QFN	TR	CST510K5	5000



7 CST510K5 DISCLAIMER

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