CT1496-2
MIL-STD-1397 Type E 10MHz
Low Level Serial Manchester 32 Bit Encoder

Features

- **Implements Type E protocol**
- **Operates with a single +5V supply**
- **Single clock input (40MHz)**
- **Selectable 4, 34, 35 bit operation**
- **Selectable Parity**
- **Includes parallel to serial converter**
- **Self-test outputs for BITE applications**
- **External encoder inhibit**
- **Bipolar Construction**
- **Use with CT1469-2 (transceiver) & CT1508-2 (4 bit decoder) to provide a complete low level serial interface**

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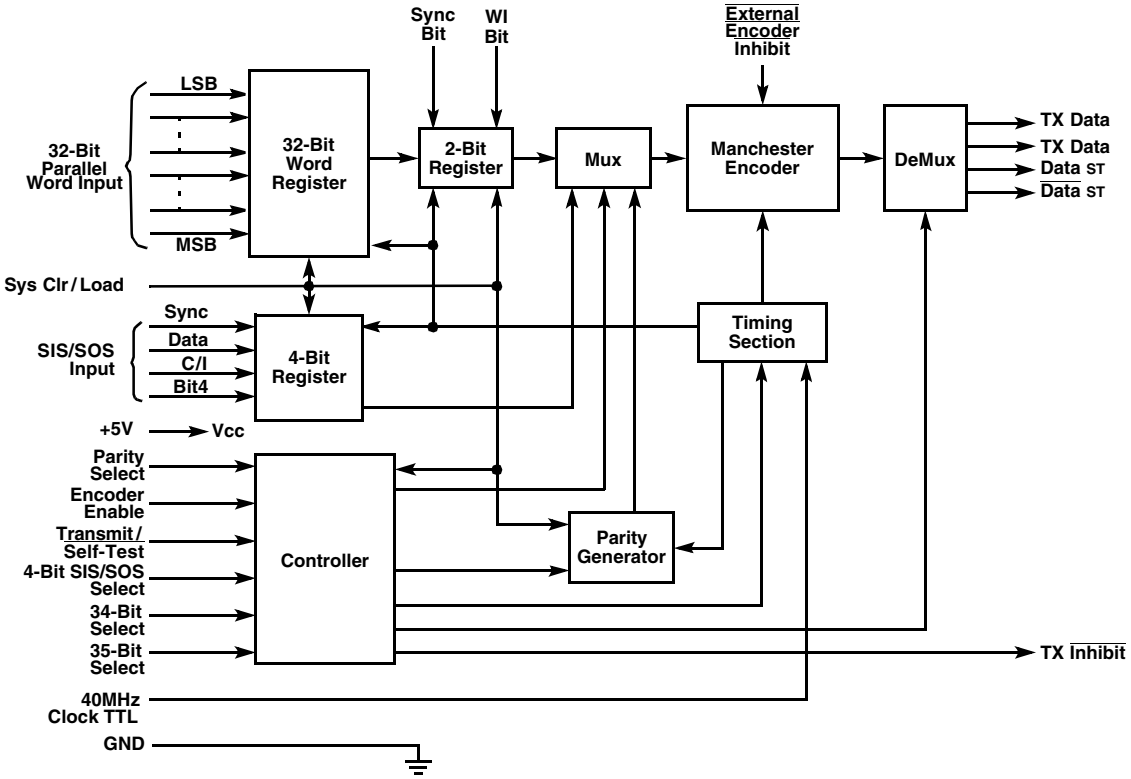
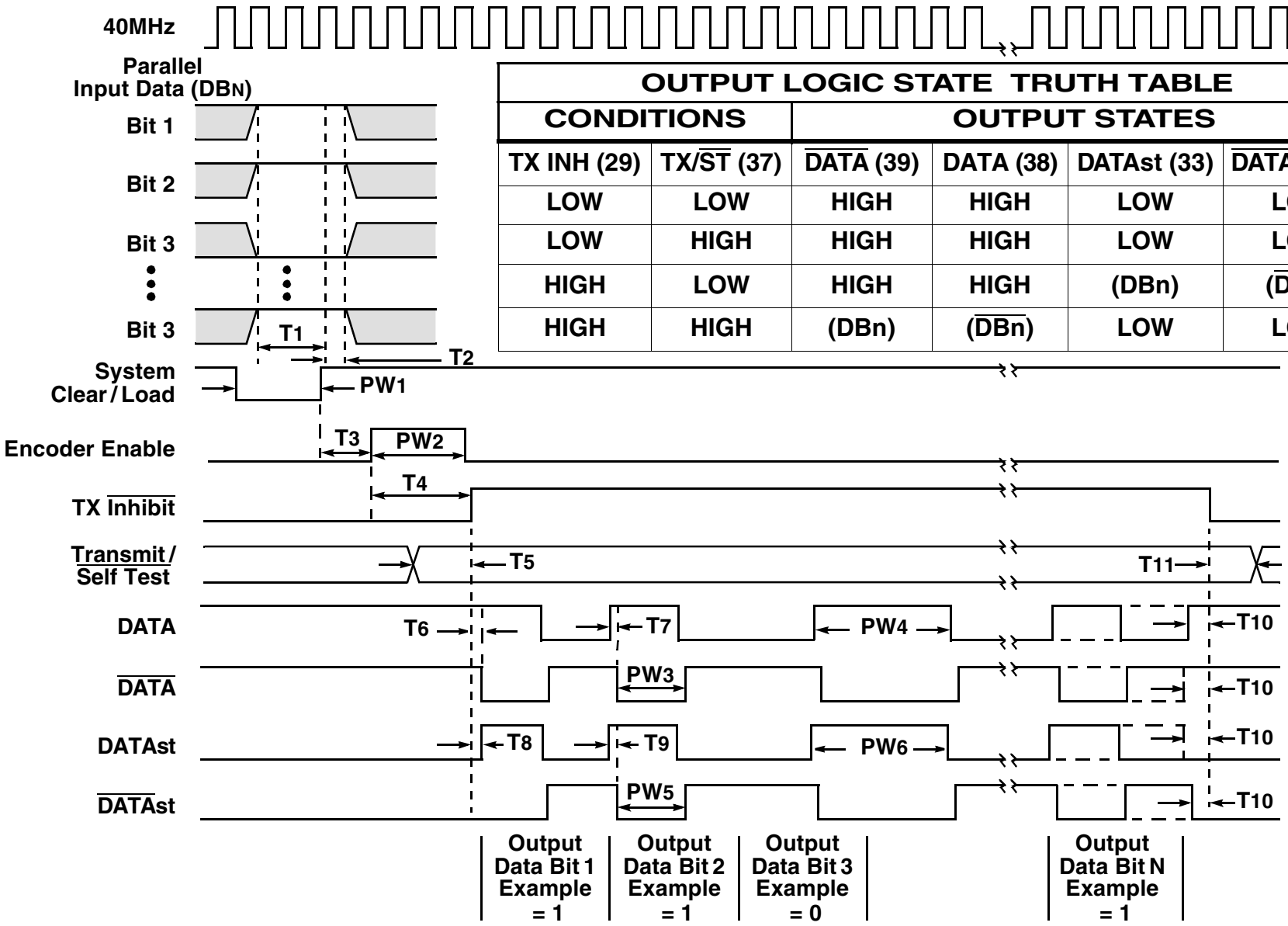
General Description

CT1496-2 is a hybrid microcircuit which incorporates a low level serial Manchester encoder in a single package. The encoder accepts 32 bit parallel data and outputs a 35 bit Manchester encoded TTL NRZ serial stream (34 bit transmission if parity option is not selected). Preceding the 32 data bits are a synchronization and word identifier bit and a parity bit trails the data (parity is optional and may be disabled). A self-test feature is implementd allowing the user to verify transmit patterns. Aeroflex Circuit Technology is a 80,000 square foot MIL-PRF-38534 certified facility in Plainview, N.Y.



Block Diagram



OUTPUT LOGIC STATE TRUTH TABLE

CONDITIONS		OUTPUT STATES			
TX INH (29)	TX/$\overline{ST}$ (37)	$\overline{DATA}$ (39)	DATA (38)	DATAst (33)	$\overline{DATA}$st (32)
LOW	LOW	HIGH	HIGH	LOW	LOW
LOW	HIGH	HIGH	HIGH	LOW	LOW
HIGH	LOW	HIGH	HIGH	(DBn)	($\overline{DBn}$)
HIGH	HIGH	(DBn)	($\overline{DBn}$)	LOW	LOW

Figure 1 – Encoder Timing Waveforms

Absolute Maximum Ratings

Parameter	Rating	Units
Supply Voltage 1/	+7.0	V
Logic Input Voltage	-1.2 to +5.5	V
Logic Input Current	-10 (low logic)	mA
Power Dissipation 2/	3.25	W
Storage Temperature Range	-65 to +125	°C
Operating Case Temperature Range	-55 to +100	°C

1/ Power sequencing shall not be required.

2/ For Logic output short circuits, line to ground logic outputs shall withstand currents not exceeding 100mA for one second for one output at a time.

DC Electrical Characteristics

(V_{DD} = 5V ±10%, T_C = -55 °C to +100°C, unless otherwise specified)

SYMBOL	PARAMETER	LIMIT
DATA 1/, $\overline{\text{DATA}}$ 1/, DATAst 2/ & $\overline{\text{DATA}}$st 2/		
V_{OH}	Logic High Output Voltage 3/, 4/	2.5V min @ I_{OH} = -50µA
V_{OL}	Logic Low Output Voltage 4/	0.5V max @ I_{OL} = 2mA
TX $\overline{\text{INHIBIT}}$		
V_{OH}	Logic High Output Voltage 3/, 4/	2.5V min @ I_{OH} = -150µA
V_{OL}	Logic Low Output Voltage 4/	0.5V max @ I_{OL} = 5mA
40MHz, Encoder Enable & $\overline{\text{External}}$ $\overline{\text{Encoder}}$ $\overline{\text{Inhibit}}$		
I_{IH}	Logic High Input Current	100µA max @ V_{IH} = 2.5V
I_{IL}	Logic Low Input Current 3/	-4mA max @ V_{IL} = 0.5V
Parity Select, 34 Bit Select, 35 Bit Select & Sys Clear / Load		
I_{IH}	Logic High Input Current	50µA max @ V_{IH} = 2.5V
I_{IL}	Logic Low Input Current 3/	-2mA max @ V_{IL} = 0.5V
Transmit / $\overline{\text{Self Test}}$ & 4 Bit SIS / SOS Select		
I_{IH}	Logic High Input Current	150µA max @ V_{IH} = 2.5V
I_{IL}	Logic Low Input Current 3/	-6mA max @ V_{IL} = 0.5V

DC Electrical Characteristics (con't)

(V_{DD} = 5V ±10%, T_C = -55 °C to +100°C, unless otherwise specified)

SYMBOL	PARAMETER	LIMIT
Sync Bit, WI Bit, 4 Bit SIS/SOS Input & 32 Bit Parallel Word Input		
I_{IH}	Logic High Input Current	20µA max @ V_{IH} = 2.5V
I_{IL}	Logic Low Input Current 3/	-400µA max @ V_{IL} = 0.5V
DC Supply Currents		
I_{CC}	V_{CC} = +5.5V (pin 31), all other pins at GND	590mA max

Notes:
1/ and 2/ The total loads on these outputpairs (1 & 2) must be matched to within 15pF in order to maintain signal skews between the lines of ≤ 5nSec maximum.
3/ Current out of a terminal is given as a negative value.
4/ Maximum total capacitance loads allowable on these pins are:

DATA, $\overline{\text{DATA}}$	40 pF max
TX $\overline{\text{INHIBIT}}$	45 pF max
DATAst & $\overline{\text{DATA}}$st	50 pF max

AC Electrical Characteristics

(V_{CC} = 5V ±10%, T_C = -55 °C to +100°C, See Figure 1, unless otherwise specified)

Symbol	Parameter / Condition	Min	Max	Unit
T1	Stable input data setup time prior to Sys Clr / Load rising edge	40	-	ns
T2	Stable input data hold time after Sys Clr / Load rising edge	20	-	ns
PW1	Sys Clr / Load pulsewidth	50	-	ns
T3	Sys Clr / Load disable to Encoder Enable pulse	40	-	ns
PW2	Encoder Enable pulsewidth	100	400	ns
T4	Encoder Enable rising edge to TX $\overline{\text{Inhibit}}$ disable (thruput delay)	30	140	ns
T5	Transmit / $\overline{\text{Self Test}}$ selection to TX $\overline{\text{Inhibit}}$ disable set-up time	50	-	ns
T6	TX $\overline{\text{Inhibit}}$ disable to output data delay (Transmit / $\overline{\text{Self Test}}$ = high)	-	10	ns
T7	DATA Output to $\overline{\text{DATA}}$ output delay {Z_{LOAD} (DATA) = Z_{LOAD} ($\overline{\text{DATA}}$), C_{LOAD} ≤ 40pF}	-	5	ns
PW3	DATA and $\overline{\text{DATA}}$ output half-bit pulsewidth	47	53	ns
PW4	DATA and $\overline{\text{DATA}}$ output bit pulsewidth	97	103	ns
T8	TX $\overline{\text{Inhibit}}$ disable to output DATAST delay	-	10	ns
T9	DATAST output $\overline{\text{DATA}}$ST output delay {Z_{LOAD} (DATAST) = Z_{LOAD} ($\overline{\text{DATA}}$ST), C_{LOAD} ≤ 50pF}	-	5	ns
PW5	DATAST and $\overline{\text{DATA}}$ST output half-bit pulsewidth	47	53	ns
PW6	DATAST and $\overline{\text{DATA}}$ST output bit pulsewidth	97	103	ns
T10	End of output DATA, $\overline{\text{DATA}}$, DATAst or $\overline{\text{DATA}}$st to TX $\overline{\text{Inhibit}}$ enable	-	10	ns
T11	TX $\overline{\text{Inhibit}}$ enable to next Transmit / $\overline{\text{Self Test}}$ selection	50	-	ns

Input Capacitance Table

Pin #	Pin Name	Maximum Input Capacitance
41	40 MHz	30 pF
40	Encoder Enable	30 pF
34	External Encoder Inhibit	30 pF
20	Parity Select	15 pF
22	34 Bit Select	15 pF
21	35 Bit Select	15 pF
42	Sys Clr / Load	15 pF
37	Transmit / $\overline{\text{Self Test}}$	45 pF
36	4 Bit SIS / SOS Select	45 pF
15	WI Bit	15 pF
16	Sync Bit	15 pF
24 - 27	4 Bit SIS / SOS Input	15 pF
43 - 60, 1 - 14	32 Bit Parallel Word Input	15 pF

Word Selection Truth Table

4 Bit Select	34 Bit Select	35 Bit Select	Word Length
High	X	X	4 Bit
Low	High	X	34 Bit
Low	Low	High	35 Bit
Low	Low	Low	Illegal

Functional Description and Pinout

Pin #	Pin Name	Function
31	VCC	+5V ± 10%
39	DATA 1/	Manchester Encoder Serial DATA Output (Max Load 40 pF).
38	$\overline{\text{DATA}}$ 1/	Manchester Encoded Serial $\overline{\text{DATA}}$ Output (Max Load 40 pF).
29	T_X $\overline{\text{Inhibit}}$	Transmit Inhibit Output (Max load 45 pF).
33	DATAST 1/	Manchester Encoded Serial DATA Output for purpose of self-testing. Connected to decoder self-test input. Controlled by Transmit / $\overline{\text{Self-Test}}$ function (max load 50 pF).
32	$\overline{\text{DATA}}$ST 1/	Manchester Encoded Serial $\overline{\text{DATA}}$ Output for Purpose Of Self-Testing. Connected to Decoder Self-test Input. Controlled By Transmit / $\overline{\text{Self-Test}}$ Function. (Max Load 50 pF).
41	40 MHz	40 MHz ± 0.1% TTL input to encoder. Symmetry 35% min. Rise and fall times 5nSec max.
20	Parity Select	Low Level Input for even parity, high level input for odd parity. Parity determined on 34 Bit word (Sync, W1, 32 Data Bits).
40	Encoder Enable	Asynchronous enable input pulse. Enables transmission when a high level signal is input.
37	Transmit / $\overline{\text{Self-Test}}$	High level input enables transmission of data thru data and data outputs: Disables DATA_{st} and $\overline{\text{DATA}}_{st}$ outputs; Which both go to low logic state. Low level input enables transmission of DATA thru DATA_{st} and $\overline{\text{DATA}}_{st}$ outputs; Disables DATA and $\overline{\text{DATA}}$ outputs, which both go to high logic state.
36	4 Bit SIS / SOS Select	High level selects 4 Bit SIS/SOS transmission. This will enable 4 Bit inputs to be loaded into the 4 Bit SIS / SOS register
22	34 Bit Select	High level selects 34 Bit transmission (32 Data Bits, W1 Bit and Sync Bit).
21	35 Bit Select	High level selects 35 Bit transmission (32 data Bits, W1 Bit, Sync Bit and Parity Bit).
42	Sys Clr / Load	A low level allows data at input pins to be loaded, clears the parity generator and initializes the internal controller. A positive going edge latches input data present at that time into the data registers.

Functional Description and Pinout (con't)

Pin #	Pin Name	Function
43-60 1-14	32 Bit Parallel Word Input (Pin 43 MSB) (Pin 14 LBS)	32 Bit Parallel Input for Data Word. This data is latched into the 32 Bit register on a Sys Clr / Load positive going edge.
16	Sync Bit	Input for Sync Bit which is latched into the 2 Bit Register on a Sys Clr/Load positive going edge (Sync Bit always logic high).
15	WI Bit	Input for Word Identifier Bit Which is latched into the 2 Bit register on a Sys Clr / Load positive going edge.
24 25 26 27	4 Bit SIS / SOS Input: Bit 4 (MSB) C/I Data Sync (LSB)	4 Bit Parallel Input for SIS / SOS which is latched into the 4 Bit SIS/SOS Register on a Sys Clr / Load positive going edge.
34	$\overline{\text{External}}$ $\overline{\text{Encoder}}$ $\overline{\text{Inhibit}}$	Asynchronous inhibit. A low forces DATA and $\overline{\text{DATA}}$ to a common high state and DATAST and $\overline{\text{DATA}}_{st}$ to a common low state.
17 18 19 23 28 30 35		Grounds. All ground pins are common and connected to hybrid case.

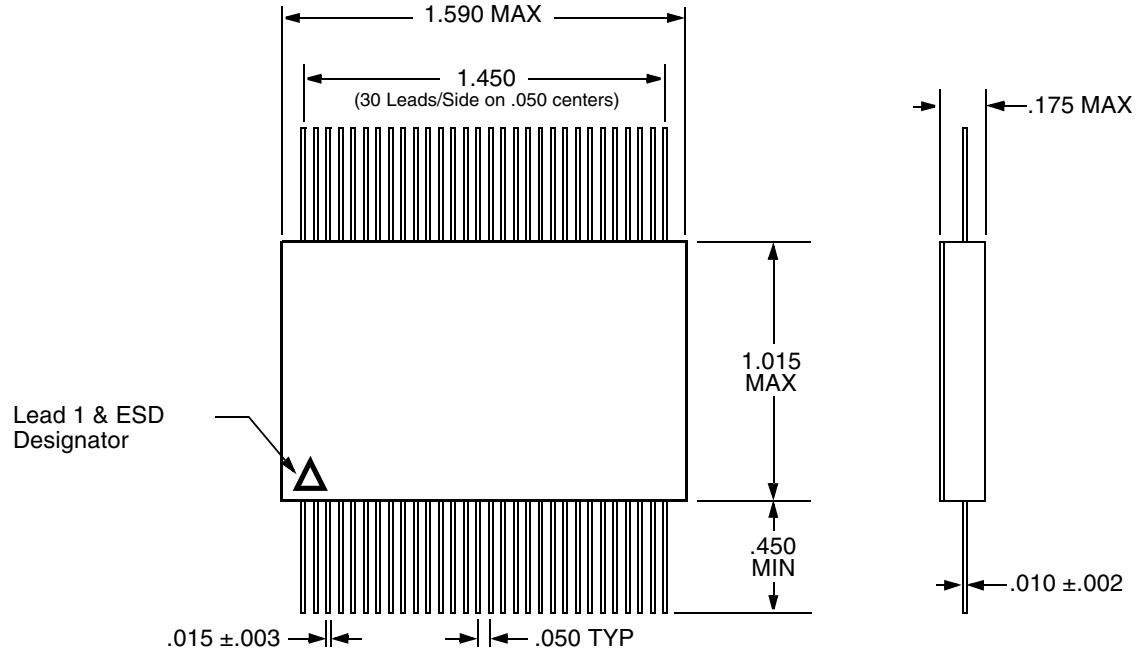
1/ Equal loads must be applied to these output pairs.

Pin #'s	Functions	Pin #'s	Functions
1	(BIT 14)	31	Vcc (+5V)
2	(BIT 13)	32	$\overline{\text{DATA}}$ ST
3	(BIT 12)	33	DATA ST
4	(BIT 11)	34	EXTERNAL ENCODER INHIBIT
5	(BIT 10)	35	GND
6	(BIT 9)	36	4 BIT SIS/SOS SELECT
7	(BIT 8)	37	TX/$\overline{\text{SELF TEST}}$
8	(BIT 7)	38	SERIAL $\overline{\text{DATA}}$
9	(BIT 6)	39	SERIAL DATA
10	(BIT 5)	40	ENCODER ENABLE
11	(BIT 4)	41	40MHz IN
12	(BIT 3)	42	SYS CLR/LOAD
13	(BIT 2)	43	(BIT 32) MSB
14	(BIT 1) LSB	44	(BIT 31)
15	W.I. BIT	45	(BIT 30)
16	SYNC BIT	46	(BIT 29)
17	GND	47	(BIT 28)
18	GND	48	(BIT 27)
19	GND	49	(BIT 26)
20	PARITY SELECT	50	(BIT 25)
21	35 BIT SELECT	51	(BIT 24)
22	34 BIT SELECT	52	(BIT 23)
23	GND	53	(BIT 22)
24	BIT 4 (MSB)	54	(BIT 21)
25	CLEAR/LOAD	55	(BIT 20)
26	DATA	56	(BIT 19)
27	SYNC (LSB)	57	(BIT 18)
28	GND	58	(BIT 17)
29	TX $\overline{\text{INHIBIT}}$	59	(BIT 16)
30	GND	60	(BIT 15)

Ordering Information

Model Number	Package
CT1496-2	Flat Package

Flat Package Outline



Specifications subject to change without notice.

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