CT212

DVB Decoder Chip

Specification

Rev. 0.9

Table of Contents

1. General Description

The CT212 is a high integration single-chip DIGITAL TV STB backend processor. It integrates MPEG A/V decoder, MPEG transport de-multiplex processor, micro-controller, and TV encoder onto a chip, facilitating a cost-effective solution for DIGITAL TV STB receivers.

The CT212 performs real-time PID filtering, decompression of MPEG1, MPEG2 video, MPEG and LPCM audio. Also, it supports EPG and VBI functions such as teletext, WSS/CGMS and closed caption.

In A/V presentation, the CT212 supports stereo and multi-channel audio output with a variety of sound effect. It also supports digital audio output through S/PDIF port. The embedded TV encoder supports CVBS, S-video, component YCbCr, RGB and progressive YPbPr formats.

The micro-controller is fully compliant to standard Turbo 8032 core. This provides easy development of system firmware and user interface.

2. Features

System operation

- ISO/IEC 13818 transport stream decoding
- EPG for digital TV and set top box applications
- Teletext with VBI (Vertical Blanking Insertion) or OSD

Transport de-multiplexing and NIM interface

- 32 PID filters
- Accept both 188 and 204 byte packet formats
- CRC-32 accelerator
- PCR clock recovery and PWM generator
- Parallel/serial interface with NIM (Network Interface Module)
- Maximal input clock rate: 13MHz for parallel and 104MHz for serial
- 2-wire serial interface with NIM control

Audio decoding and processing

- Decode *MPEG2 and MPEG1* Audio at sampling frequency of 16K, 22.05K, 24K, 32K, 44.1K, and 48KHz
- Decode *Linear PCM* at sampling frequency of 44.1 KHz, 48KHz and 96 KHz
- Output serial PCM audio data with 16, 18, 20 and 24 bits resolution and sampling rate at 16K, 22.05K, 24K, 32K, 44.1K, 48K and 96 KHz
- Support 3D surround sound
- Support key-shift
- S/PDIF output meet *IEC958* spec, supporting compressed AC-3 and stereo digital PCM
- Digital mute control and volume adjustment

Video decoding and processing

- Decode MPEG2 Main Profile Main Level and MPEG1 video streams, up to 720 × 480 at 30 Hz and 720 × 576 at 25 Hz resolution
- Support 16:9 and 4:3 TV aspect ratios, by Pan & Scan and Letter Box conversion

- Support frame rate conversion for different video formats
- Support flexible horizontal and vertical scaling of x 16 ~ x 1/16
- BrightView to brighten the details of dark area in a picture: Normal/Bright/Soft
- Fade in/out control
- Support background picture
- Support 16 color 32x32 cursor
- Four rectangle strip planes.

OSD (On Screen Display)

- 2 bits, 4 bits and 8 bits per pixel, up to 256 color palettes
  - One line to full screen OSD
  - Region-based alpha-blending
  - Scroll display capability
- Highlight processing
- Seamlessly link adjacent OSD regions
- 64 mix-weighting level for blending OSD and video
- Bitmap OSD
  - Support horizontal pixel duplication to enlarge bitmap automatically.
  - Support sub-region redraw to facilitate bitmap display.
- Font OSD:
  - Support 2 bits/pixel encoding font OSD.
  - Support eight kinds of font size for each region
  - Maximum 256 characters in one font table
  - Eight choices of font size to build font table: 4 pixels to 32 pixels in 4 pixels step
  - Support horizontal pixel duplication to enlarge character automatically.
  - Maximum 44 characters display and maximum 8 different font colors for each region
  - Support color-change option to enrich font color.

TV encoder

- NTSC-M, PAL-B, D, G, H, I, N_C, M encoding
- Support interlace and progressive scan

- Programmable Y/C delay relationship
- Four 10-bit DACs run at 2X pixel rate, provide CVBS/S-video, RGB, YCbCr and progressive scan YPbPr output formats
- Teletext, WSS/CGMS and closed captioning

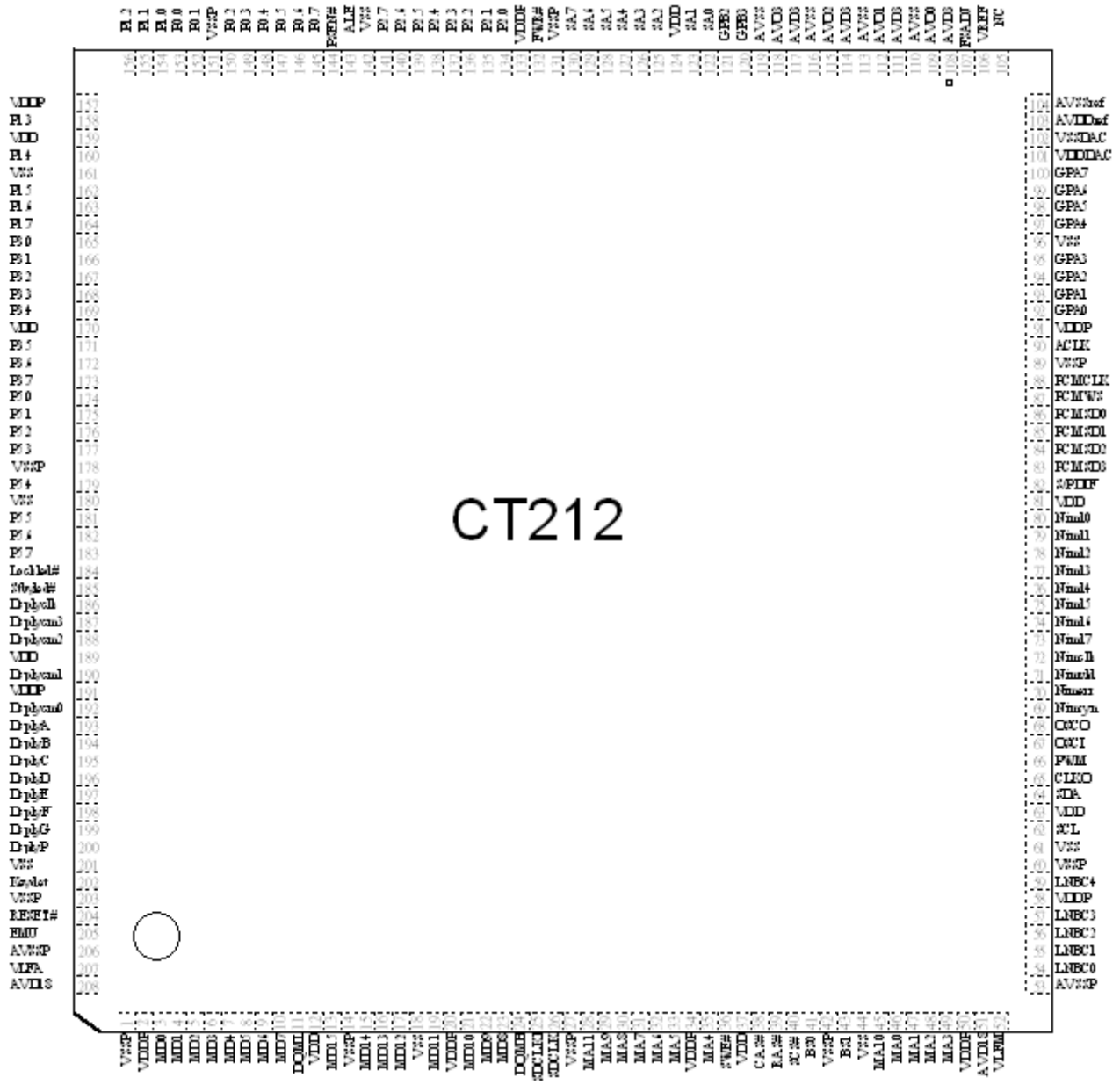
Embedded micro-controller

- 8-bit micro-controller compatible to Turbo 8032
- Up to 50MHz operating frequency
- 256-byte Scratchpad RAM
- Embedded 32K-byte data memory
- 64K-byte address space for external Program memory
- 32K-byte address space for external Data Memory
- Three 16-bit timer/counters
- Five 8-bit bi-directional ports
- Six interrupt channels
- One programmable watch-dog timer
- Two programmable full duplex serial port

Electrical and physical characteristics

- Build-in PLL
- Single 27 MHz clock input crystal with PCR control
- Support 16M, 32M and 64M SDRAM operating at up to 133MHz
- 1.8V and 3.3V dual power supply
- 208 pin PQFP

3. Pin Configuration



4. Pin Description

4.1 System Signals and Power/Ground

Pin name	Type	Description
OSCI	I	Clock input. It can be oscillator or crystal input. Frequency is 27MHz.
OSCO	O	Output terminal for crystal connection. This signal also emulates as VCLK for digital video pixel clock output
CLKO	O	Clock output, frequency programmable, see reg. CLKO definition
RESET#	I	System reset, active LOW
EMU	I	Emulation mode select EMU =0, normal operation, enable internal micro-controller, =1, select emulation mode, disable internal micro-controller.
GPA[7:0]/PD[7:0]	I/O	General purpose IO bus A bits[7:0], initial in input state/digital pixel data bus bits[7:0]
PWM	O	Clock control PWM output for PCR recovery
VLFM	AI	Loop filter, connected to a capacitor
VLFA	AI	Loop filter, connected to a capacitor
AVD18	AP	1.8V analog power supply
AVSSP	AG	Analog ground
VDDP	DP	3.3V digital power supply for IO driving buffer
VSSP	DG	Digital ground for IO driving buffer
VDD	DP	1.8V digital power supply for core
VSS	DG	Digital ground for core

4.2 Micro-controller Interface Signals

Pin name	Type	Internal uC mode (EMU=0)	External uC mode (EMU=1)
ALE	I/O	Address latch enable output. It is used to latch the address low byte expressed on port0.	ALE: Address latch enable input.
PSEN#	I/O	Program strobe enable output. It is used to strobe code of the external program memory.	LATS: Low byte address conveying type select input. LATS=0, mux with SAD[7:0]; LATS=1, conveyed on SA[7:0]

PORT0 [7:0]	I/O	Port0 is an 8-bit bi-directional I/O port. In accesses to external memory, port0 outputs the low byte of the external memory address, time-multiplexed with the data byte being written or read.	SAD[7:0]: low byte address and data bus, bi-directional.
SA[7:0]/GPA[15:8]	I/O	SA[7:0]: lower address byte for external program and data memories, latched by ALE from Port0 address phase, output. This is the default. Alternately these pins can be used as general purpose IO signals. GPA[15:8]: general purpose IO bus A bits[15:8], bi-directional.	LATS=1, SA[7:0]: low byte address bus, input. LATS=0, SA[7:0] output or GPA[15:8] selected by register
PORT2 [7:0]	I/O	Port2 is an 8-bit bi-directional I/O port with internal pull-up. Port2 also serves as memory address bus. In accesses to external memory, port2 outputs the high byte of the external memory address.	SA[15:8]: high byte address bus, input.
PORT1 [7:0]	I/O	Port1 is an 8-bit bi-directional I/O port with internal pull-up. P1.0 and p1.1 also serve the T2 and T2EX functions, respectively. P1.2 and P1.3 also serve the RXD2 and TXD2, respectively. P1.4: GPB0, general purpose IO bus B bit 0, initial in input state P1.5, P1.6 and P1.7 also serve external interrupt inputs	P1.4: INTTS#, output P1.5: CS#, input

PORT3 [7:0]	I/O	Port3 is an 8-bit bi-directional I/O port with internal pull-up. Port3 also serve following special functions: P3.0 RXD1 (serial input port) P3.1 TXD1 (serial output port) P3.2 IR input P3.3: GPB1, general purpose IO bus B bit 1, initial in input state P3.4 T0 (timer 0 external input) P3.5 T1 (timer 1 external input) P3.6 WR# (external data memory write) P3.7 RD# (external data memory read)	P3.3: INTM#, output P3.6: WR#, input P3.7: RD#, input
PORT5 [7:0]	I/O	Port5 is an 8-bit bi-directional I/O port, default in input state.	
FWR#	O	Flash write enable output	

4.2.1 External Micro-controller Mode

Pin name	Type	Description
ALE	I	Address latch enable. It is used to latch the low byte address of SAD[7:0] as LATS=0.
LATS	I	Low byte address conveying type select, input only. LATS=0, mux with SAD[7:0]; LATS=1, conveyed on SA[7:0].
SAD[7:0]	I/O	When ALE is active (ALE=1), it is the low byte of the address. And it is time-multiplexed with the data byte being written(WR# active) or read(RD# active).

SA[7:0]/GPA[15:8]	I/O	When LATS=1, SA[7:0] input is specified, representing the low byte address bus, input. When LATS=0, two options: one is SA[7:0] output of the low byte address latched from SAD[7:0] input by ALE; the other is GPA[15:8], general purpose IO bus A bits[15:8], bi-directional; SA[7:0] output is default.
SA[15:8]	I	The high byte of the address bus.
CS#	I	Chip select input, active low
INTTS#	O	Interrupt request of on-chip transport de-multiplex processor, active low.
INTM#	O	Interrupt request of on-chip AV decoder, active low.
WR#	I	Write enable, active low.
RD#	I	Read enable, active low.

4.3 SDRAM Interface Signals

Pin name	Type	Description (64M type)	Alternative (2x16M type)
MA[11:0]	O	SDRAM Address bus output	MA[11]: no use MA[10:0]: Address bus output
BS[1:0]	O	SDRAM Bank Select output	BS[0]: BA, Bank address output BS[1]: SCS1#, Chip select output of 2nd SDRAM, active low
MD[15:0]	I/O	SDRAM Data bus keeps as input state except for WRITE operation	MD[15:0]
SDCLK	O	SDRAM Clock Output	SDCLK
SDCLKI	I	SDRAM Clock Input	SDCLKI
SCS#	O	SDRAM Chip Select output, active Low	SCS0#, Chip select output of 1st SDRAM, active low
RAS#	O	Row Address Strobe output, active Low	RAS#

CAS#	O	Column Address Strobe output, active Low	CAS#
SWE#	O	Write Enable output, active Low	SWE#
DQML	O	Low byte data mask, active High	DQML
DQMH	O	High byte data mask, active High	DQMH

4.4 Video Interface Signals

Pin name	Type	Description
AVO0	AO	Four kinds of analog video output supoorted: CVBS(composite)/S-video(Y/C), YCbCr(component), RGB(component) and YPbPr Progressive scan. Mode 1: CVBS + S-video(Y/C) Mode 2: CVBS+YCbCr Mode 3: CVBS+RGB Mode 4: YPbPr This pin is: In mode 1: (CVBS) analog composite signal output. 2: (Y) analog luminance signal output. 3: (G) analog Green signal output. 4: (Y) analog progressive luminance signal output.
AVO1	AO	This pin is: In mode 1: (Y) analog luminance signal output, 2: (Cb) analog chrominance signal output. 3: (B) analog blue signal output. 4: (Pb) analog progressive chrominance signal output.
AVO2	AO	This pin is: In mode 1: (C) analog chrominance signal output, 2: (Cr) analog chrominance signal output. 3: (R) analog red signal output. 4: (Pr) analog progressive chrominance signal output.

AVO3	AO	This pin is: In mode 1: (CVBS) analog composite signal output. 2: (CVBS) analog composite signal output. 3: (CVBS) analog composite signal output. 4: (Y) analog progressive luminance signal output.
FSADJ	AO	Full-scale adjust control pin. The full-scale current of DAC is controlled by connecting a resister (R_{SET}) between this pin and AVSSref. The full-scale current I_{OUT} = K * VREF / R_{SET} (mA), K = 2765 for 3.3V VDD.
VREF	AO	Voltage reference output. Typical value is 0.9V. A 0.1uF ceramic capacitor decouples this pin to AVSSref
AVD33	AP	3.3v analog power supply of video DAC
AVSS	AG	Analog ground of video DAC
AVDDref	AP	3.3v analog reference voltage supply of video DAC
AVSSref	AG	Analog reference ground of video DAC
VDDDAC	DP	3.3V digital power supply of video DAC
VSSDAC	DG	Digital ground of video DAC
GPB2/Hsync	I/O	General purpose IO bus B bit 2, initial in input state/Horizontal sync output; GPB2 by default
GPB3/Vsync	I/O	General purpose IO bus B bit 3, initial in input state/Vertical sync output; GPB3 by default

4.5 Audio Interface Signals

Pin name	Type	Description
ACLK	I/O	Clock for audio sampling rate. Its frequency can be 256fs or 384fs. (fs is audio sampling rate.) The default is in output state and 384fs.
PCMCLK	O	Audio PCM clock output
PCMSD0	O	PCM Serial Data output for left/right channel or stereo L/R channel
PCMSD1	O	PCM Serial Data output for left surround/right surround channel
PCMSD2	O	PCM Serial Data output for center/LFE channel

PCMSD3	O	PCM Serial Data output for down-mixed L/R channel
PCMWS	O	PCM channel word select output
S/PDIF	O	IEC-958 self-clocking digital serial output

4.6 NIM Interface Signals

Pin name	Type	Description
Nimerr	I	Error of parallel/serial input
Nimsyn	I	Sync of parallel/serial input
Nimvld	I	Valid of parallel/serial input
Nimclk	I	Clock of parallel/serial input
Nimd[7]/NimdA	I	Parallel data input bit[7]/serial data input A
Nimd[6:1]	I	Parallel data input bits[6:1]
Nimd[0]/NimdB	I	Parallel data input bits[0]/serial data input B
SCL	I/O	Serial control clock
SDA	I/O	Serial control data
LNBC[4:0]	O	LNB control output bits[4:0], reflecting the setting of corresponding bits in reg. LNB control

4.7 Panel Control Signals

Pin name	Type	Description
Stbyled#	O	Standby LED indicator, active low
Lockled#	O	NIM lock LED indicator, active low
Keydet	I	Front panel key pressed detection
Dsplycm[3:0]	O	Front panel 7-seg display common port[3:0]

DsplyA	O	A segment of 7-seg display, active high
DsplyB	O	B segment of 7-seg display, active high
DsplyC	O	C segment of 7-seg display, active high
DsplyD	O	D segment of 7-seg display, active high
DsplyE	O	E segment of 7-seg display, active high
DsplyF	O	F segment of 7-seg display, active high
DsplyG	O	G segment of 7-seg display, active high
DsplyP	O	Dot of 7-seg display, active high
Dsplyclk	O	Clock for 7-seg display and key-pad scanning

4.8 Pin Map

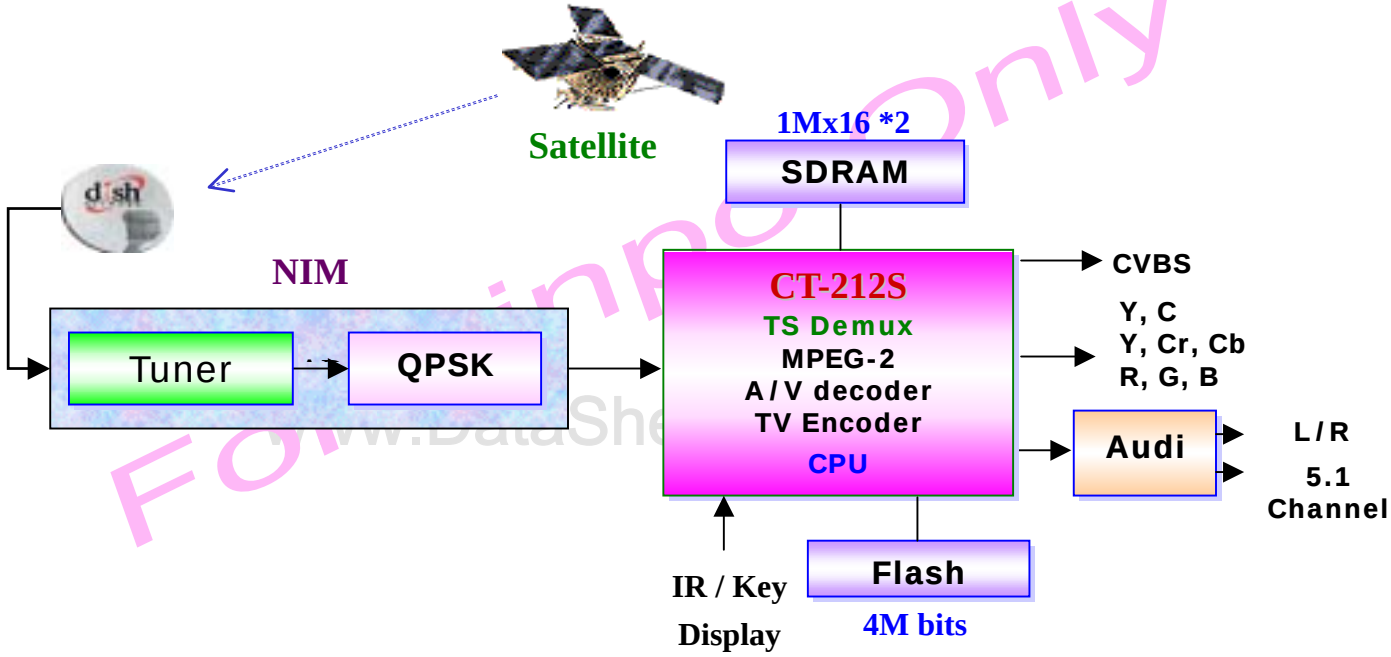
Pin no.	Signal Name	Pin no.	Signal Name	Pin no.	Signal Name	Pin no.	Signal Name
1	VSSP	53	AVSSP	105	NC	157	VDDP
2	VDDP	54	LNBC0	106	VREF	158	P1.3
3	MD0	55	LNBC1	107	FSADJ	159	VDD
4	MD1	56	LNBC2	108	AVD33	160	GPB0/INTTS#
5	MD2	57	LNBC3	109	AVO0	161	VSS
6	MD3	58	VDDP	110	AVSS	162	P1.5/CS#
7	MD4	59	LNBC4	111	AVD33	163	P1.6
8	MD5	60	VSSP	112	AVO1	164	P1.7
9	MD6	61	VSS	113	AVSS	165	P3.0
10	MD7	62	SCL	114	AVD33	166	P3.1
11	DQML	63	VDD	115	AVO2	167	P3.2
12	VDD	64	SDA	116	AVSS	168	GPB1/INTM#
13	MD15	65	CLKO	117	AVD33	169	P3.4
14	VSSP	66	PWM	118	AVO3	170	VDD
15	MD14	67	OSCI	119	AVSS	171	P3.5
16	MD13	68	OSCO	120	GPB3/Vsync	172	P3.6/WR#
17	MD12	69	Nimsyn	121	GPB2/Hsync	173	P3.7/RD#

18	VSS	70	Nimerr	122	SA0/GPA8	174	P5.0
19	MD11	71	Nimvld	123	SA1/GPA9	175	P5.1
20	VDDP	72	Nimclk	124	VDD	176	P5.2
21	MD10	73	Nimd7/NimdA	125	SA2/GPA10	177	P5.3
22	MD9	74	Nimd6	126	SA3/GPA11	178	VSSP
23	MD8	75	Nimd5	127	SA4/GPA12	179	P5.4
24	DQMH	76	Nimd4	128	SA5/GPA13	180	VSS
25	SDCLKI	77	Nimd3	129	SA6/GPA14	181	P5.5
26	SDCLK	78	Nimd2	130	SA7/GPA15	182	P5.6
27	VSSP	79	Nimd1	131	VSSP	183	P5.7
28	MA11	80	Nimd0/NimdB	132	FWR#	184	Lockled#
29	MA9	81	VDD	133	VDDP	185	Stbyled#
30	MA8	82	S/PDIF	134	P2.0/SA8	186	Dsplyclk
31	MA7	83	PCMSD3	135	P2.1/SA9	187	Dsplycm3
32	MA6	84	PCMSD2	136	P2.2/SA10	188	Dsplycm2
33	MA5	85	PCMSD1	137	P2.3/SA11	189	VDD
34	VDDP	86	PCMSD0	138	P2.4/SA12	190	Dsplycm1
35	MA4	87	PCMWS	139	P2.5/SA13	191	VDDP
36	SWE#	88	PCMCLK	140	P2.6/SA14	192	Dsplycm0
37	VDD	89	VSSP	141	P2.7/SA15	193	DsplyA
38	CAS#	90	ACLK	142	VSS	194	DsplyB
39	RAS#	91	VDDP	143	ALE	195	DsplyC
40	SCS#/SCS0#	92	GPA0/PD0	144	PSEN#/LATS	196	DsplyD
41	BS0/BA	93	GPA1/PD1	145	P0.7/SAD7	197	DsplyE
42	VSSP	94	GPA2/PD2	146	P0.6/SAD6	198	DsplyF
43	BS1/SCS1#	95	GPA3/PD3	147	P0.5/SAD5	199	DsplyG
44	VSS	96	VSS	148	P0.4/SAD4	200	DsplyP
45	MA10	97	GPA4/PD4	149	P0.3/SAD3	201	VSS
46	MA0	98	GPA5/PD5	150	P0.2/SAD2	202	Keydet
47	MA1	99	GPA6/PD6	151	VSSP	203	VSSP
48	MA2	100	GPA7/PD7	152	P0.1/SAD1	204	RESET#
49	MA3	101	VDDDAC	153	P0.0/SAD0	205	EMU
50	VDDP	102	VSSDAC	154	P1.0	206	AVSSP

51	AVD18V	103	AVDDref	155	P1.1	207	VLFA
52	VLFM	104	AVSSref	156	P1.2	208	AVD18

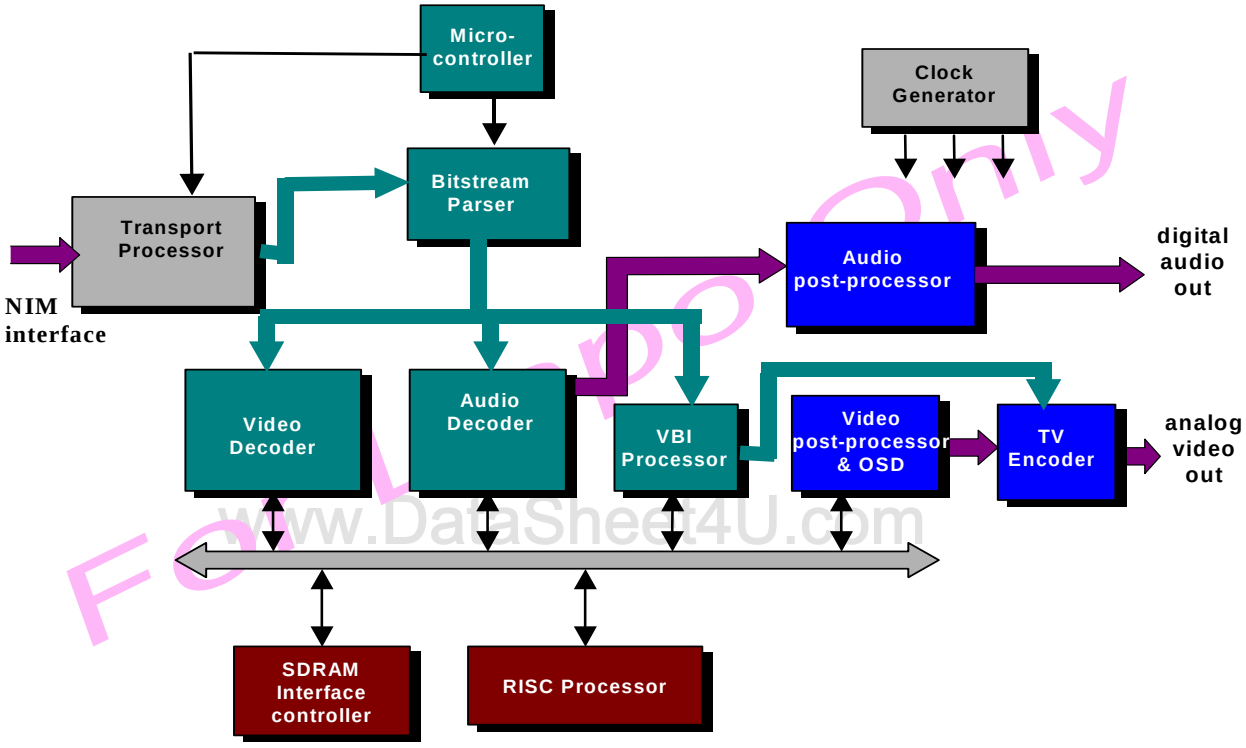
5. System Diagram

The following diagram shows an example of CT212 application in a satellite DIGITAL TV STB receiver. In this example, CT212 operates with the NIM, SDRAM and audio DAC to achieve the purpose of low cost and simple system configuration. The Flash memory stores system firmware and command the system operation.

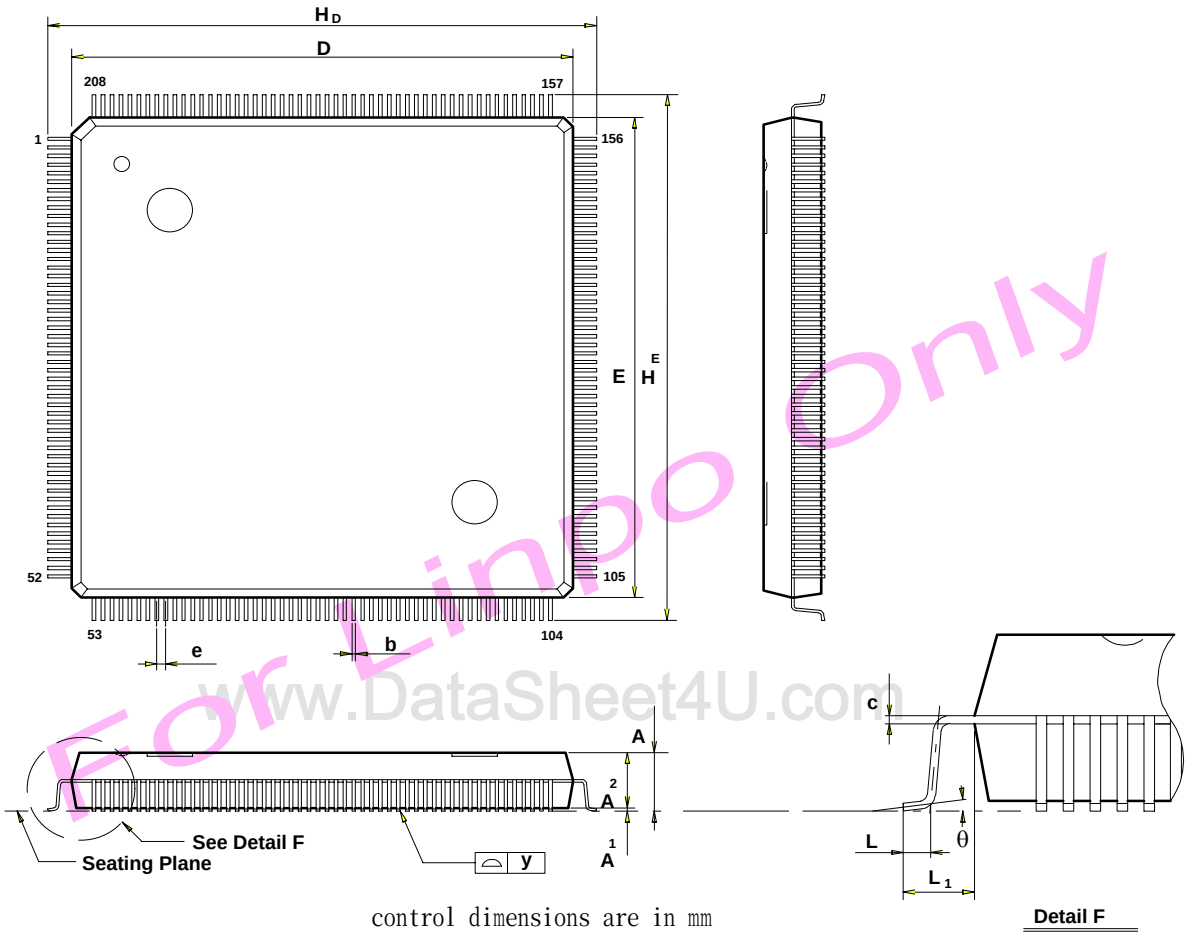


6. Block Diagram

Following diagram shows the functional blocks of CT212.



7. Package Specification



control dimensions are in mm

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.145	—	—	3.68
A_1	0.004	—	—	0.10	—	—
A_2	0.122	0.127	0.132	3.10	3.23	3.35
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.010	0.10	0.15	0.25
D	1.097	1.102	1.107	27.87	28.00	28.13
E	1.097	1.102	1.107	27.87	28.00	28.13
e	0.016	0.020	0.024	0.40	0.50	0.60
H_D	1.193	1.205	1.217	30.30	30.60	30.90
H_E	1.193	1.205	1.217	30.30	30.60	30.90
L	0.012	0.020	0.028	0.30	0.50	0.70
L_1	0.043	0.051	0.059	1.10	1.30	1.50
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Cheertek's Locations

Corporate Headquarter

5F-2, No.2-1, Li Hsin Rd. Science-Based Industrial Park

Hsinchu, Taiwan, R.O.C.

Tel: 886-3-666-7777

Fax: 886-3-611-2216, 886-3-666-7999

Cheertek (ShangHai) Ltd.

27F, 2299 Yan An Road (west),

Shanghai, China

Tel: 86-21-62361579; 86-21-6236599

Fax: 86-21-62361562

Shenzhen Office, Cheertek (ShangHai) Ltd.

Rm. 26C, Oriental Building,

No.1072, Jian She Lu, Shenzhen , China

Tel: 86-755-83643001

Fax: 86-755-83643186