MCTC

CT2522

Single LOW POWER +5 VOLT ONLY TRANSCEIVER FOR MIL-STD-1553B

GENERAL DESCRIPTION

The CT2522 +5V only transceiver is a third generation hybrid device utilizing custom monolithic drivers and receivers. This allows the device to be operated from a single +5V supply. This design results in lower power and 100% duty cycle is permissible at 125C° case temperature. Each driver dissipates less than 1.0 watt at 25% duty cycle.

Marconi Circuit Technology Corporation is a MIL-STD-1772 Certified Manufacturer.

FEATURES

- 24 pin double dip package or flat pack
- Monolithic +5V Only Drivers
- AC interstage coupling prevents static burnout
- Receiver filtered to improve S/N ratio of system
- 20mV typical output offset
- TTL compatible

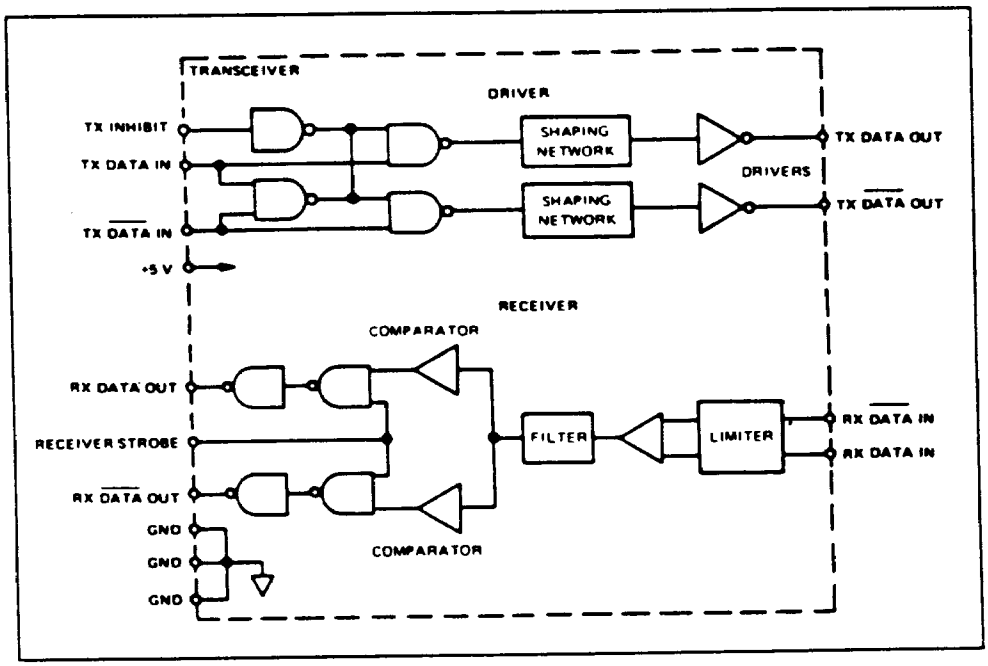


FIGURE 1. FUNCTIONAL DIAGRAM

ELECTRICAL CHARACTERISTICS, RECEIVER SECTION

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Differential input impedance DC to 1 MHz		Z_{In}	9K			ohms
Differential voltage range		V_{idr}	±20V			V_{peak}
Input common mode voltage range		V_{icr}	±10V			V_{peak}
Common mode rejection ratio (from point A)		CMRR	40			dB
STROBE characteristics						
(Logic "0" inhibits output)						
"0" input current (V_s = 0.4 V)		I_{il}			-1	ma
"1" input current (V_s = 2.7 V)		I_{ih}			40	μA
"0" input voltage		V_{il}			0.7	V
"1" input voltage		V_{ih}	2			V
Threshold characteristics (sine wave at 1 MHz)		V_{th1}	0.8	1.0	1.1	V_{p-p}
NOTE: Threshold voltages refer to point A.						
Filter characteristics	2 MHz	V_{th2}	1.5		8	V_{p-p}
(sine wave input)	3 MHz	V_{th3}	5			V_{p-p}
OUTPUT CHARACTERISTICS						
"1" state (I_{source} = 400μA)		V_{oh}	2.5	3.4		V
"0" state (I_{sink} = 4mA)		V_{ol}			0.5	V
NOTE: With receiver input below threshold both RX DATA OUT and RX $\overline{\text{DATA}}$ OUT remain in "0" state.						
Delay (average) from differential input zero crossings to RX DATA OUT and RX $\overline{\text{DATA}}$ OUT output to 50% points		t_{DRX}		340	450	ns

ELECTRICAL CHARACTERISTICS, DRIVER SECTION

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
"0" input current (V_{in} = 0.4 V)	I_{il}			-1	ma
"1" input current (V_{in} = 2.7 V)	I_{ih}			100	μA
"0" input voltage	V_{il}			0.7	V
"1" input voltage	V_{ih}	2			V
Delay from TX INHIBIT (0 ⟶ 1) to inhibited output impedance	t_{DXOFF}		150	225	ns
Delay from TX INHIBIT (1 ⟶ 0) to active output impedance	t_{DXON}		100	150	ns
Differential output nosie	V_{noi}			10	mV_{p-p}
Differential output impendance (inhibited at 1 MHz	Z_{oi}	5K			ohms
OUTPUT CHARACTERISTICS					
Differential output level at point B, (145-ohm load)	V_o	24	27	35	V_{p-p}
Rise and fall times (10% - 90% of p-p output)	t_r	100	160	300	ns
Output offset at point A (35-ohm load) 2.5 μs after mid-bit crossing of parity bit of last word of a 600 μs message	V_{os}		±20	±75	mV peak
Delay from 50% point of TX DATA IN or TX $\overline{\text{DATA}}$ IN to zero crossing differential output	t_{DTX}		100	150	ns

POWER AND THERMAL DATA, TOTAL HYBRID (DRIVER AND RECEIVER)

PARAMETER/CONDITION		SYMBOL	CT2522 MIN	CT2522 TYP	CT2522 MAX	UNIT
Power Supply voltages		V_{cc}	4.5	5.0	5.5	V
Power dissipation of most critical (hottest) device in hybrid during continuous transmission (100%) duty cycle)		P_c	Note 1	0.20	0.25	W
Thermal resistance, most critical device		$Ø_{jc}$			60	°C/W
Junction to case tempetature rise of most critical device at 100% duty cycle transmission		T_{jc}			15	°C
Total supply current "standby" mode, or transmitting at less than 1% duty cycle (e.g. 20 µs of transmission every 2 ms or longer interval)		I_{cc}		110	120	mA
Total supply current transmitting at 1 MHz into a 35-ohm load at point A	*DUTY CYCLE					
	25%	$1_{cc}25$	Note 2	225	240	mA
	100%	$1_{cc}100$	Note 2	535	610	mA

*Dual unit (one unit transmitting)

NOTE 1: Decreases linearly to zero at zero duty cycle.

NOTE 2: Decreases linearly to applicable "standby by" value at zero duty cycle.

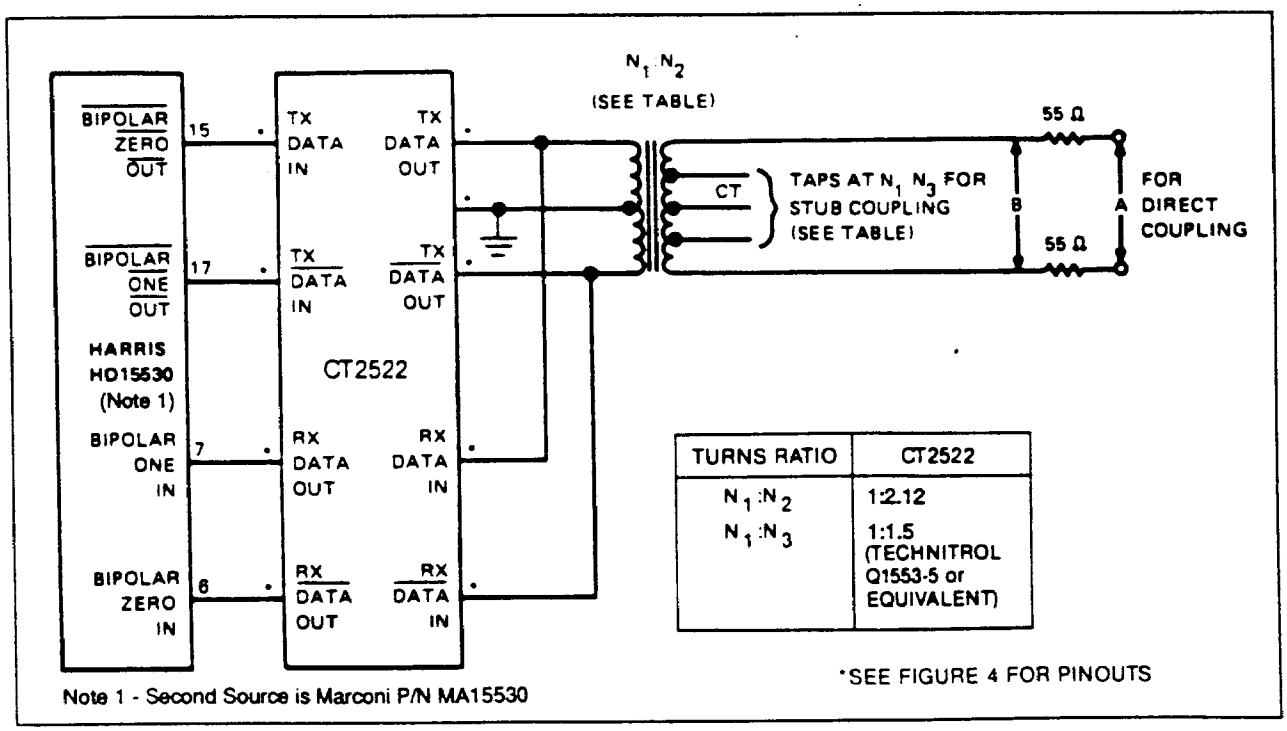


FIGURE 2. TYPICAL INPUT/OUTPUT CONNECTIONS

Absolute Maximum Ratings

Power Supply voltage (V_{CCL})	–0.3 to + 7.0V
Logic Input Voltage	–0.3 to +5.5V
Receiver Differential Input (RX DATA IN, RX $\overline{\text{DATA}}$ IN)	±20V (40Vp-p)
Receiver Input Voltage (RX DATA IN or RX $\overline{\text{DATA}}$ IN)	±15V
Driver Output Current (TX DATA OUT or TD $\overline{\text{DATA}}$ OUT)	800mA
Transmission Duty Cycle @Tc = 125°C	100%
Operating Case Temperature Range (Te)	–55°C to +125°C

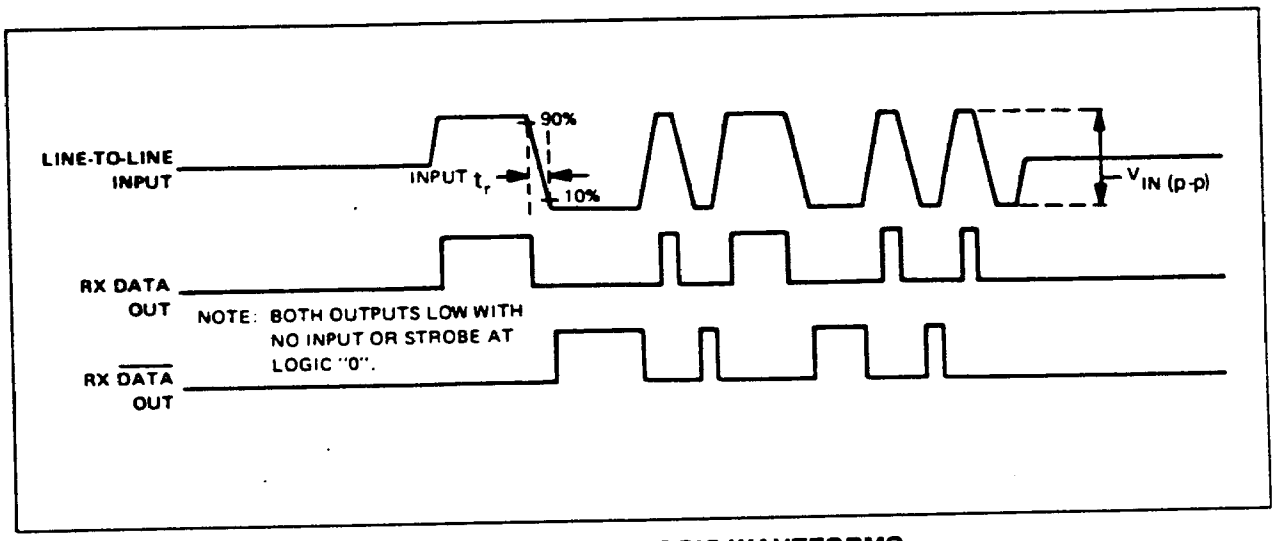


FIGURE 3. RECEIVER LOGIC WAVEFORMS
(FOR INVERTED DATA OUTPUT, ORDER CT2522I)

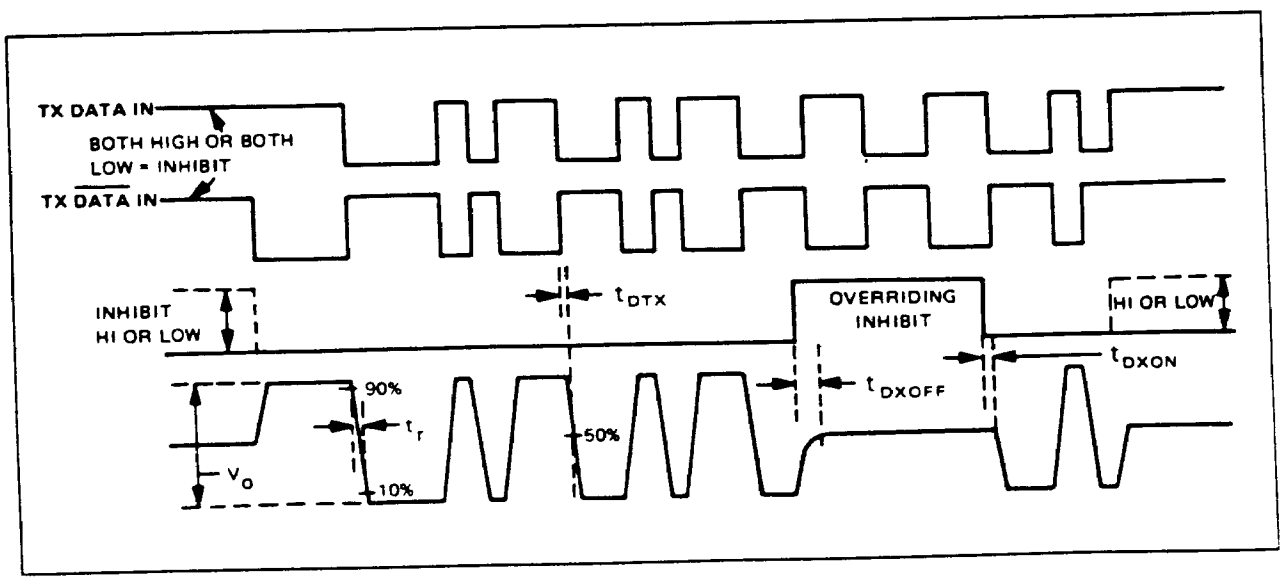
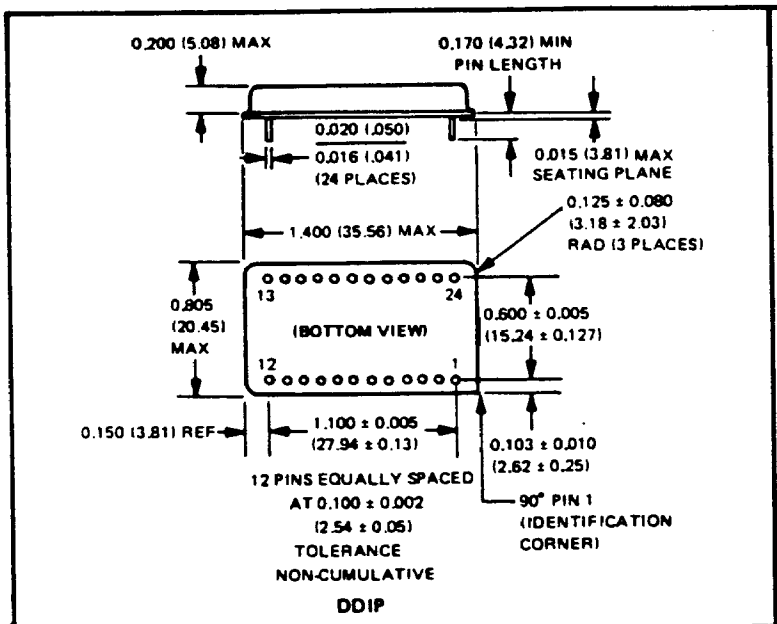
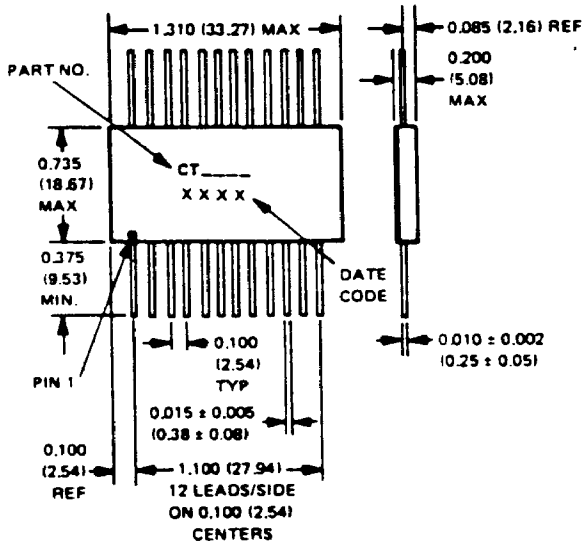


FIGURE 4. DRIVER LOGIC WAVEFORMS



SINGLE UNIT (DDIP AND FLAT PACK)			
PIN	FUNCTION	PIN	FUNCTION
1	TX DATA OUT	13	N.C.
2	TX DATA OUT	14	N.C.
3	GND	15	RX DATA IN
4	N.C.	16	RX DATA IN
5	N.C.	17	N.C.
6	N.C.	18	GND
7	RX DATA OUT	19	N.C.
8	STROBE	20	+5 V
9	GND	21	TX INHIBIT
10	RX DATA OUT	22	TX DATA IN
11	N.C.	23	TX DATA IN
12	N.C.	24	N.C.



NOTES:
1. DIMENSIONS SHOWN ARE IN INCHES (MILLIMETERS IN PARENTHESES).
2. LEAD IDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.
3. LEAD CLUSTER SHALL BE CENTERED WITHIN ±0.10 (2.54) OF OUTLINE DIMENSIONS. LEAD SPACING DIMENSIONS APPLY ONLY AT SEATING PLANE.
4. PIN MATERIAL MEETS SOLDERABILITY REQUIREMENTS OF MIL-STD-202E. METHOD 208C.

NOTES:
1. GDN PINS OF EACH SECTION SHOULD ALL BE CONNECTED EXTERNALLY.
2. DIMENSIONS SHOWN ARE IN INCHES (MILLIMETERS IN PARENTHESES).
3. LEAD INDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.
4. LEAD CLUSTER SHALL BE CENTERED WITHIN ±0.10 (2.54) OF OUTLINE DIMENSIONS. LEAD SPACING DIMENSIONS APPLY ONLY AT SEATING PLANE.
5. PIN MATERIAL MEETS SOLDERABILITY REQUIREMENTS MIL-STD-883, METHOD 2003.

**LOWER PROFILE PACKAGES AVAILABLE, PLEASE CONTACT FACTORY.*

FIGURE 5. MECHANICAL OUTLINE AND PINOUTS

RECOMMENDED DESIGN PRACTICES

(a) DECOUPLING

Decouple V_{CC} to ground, close to the hybrid with a >10μF tantalum capacitor in parallel with a 100nF ceramic bypass capacitor.

Note: Peak transmission current drawn from V_{CC} is 650mA.

(b) PCB LAYOUT

- Full PCB ground-planing is recommended.
- It is good practice to ensure connections from encoder/decoder to 'TXLOGICIN', '$\overline{\text{TXLOGICIN}}$' and 'TXINHIBIT' are as short as possible and of balanced length, shape and area. Optimum results are obtained when these signals have minimum rise/fall times and minimum differential delays.
- Connections between '$\overline{\text{TXDATAOUT}}$' and the center tapped transformer should be designed to:
  - (i) Withstand peak transmission currents at required operating duty cycles
  - (ii) Minimize added series inductance
  - (iii) Ensure system capacitance in conjunction with transceiver and transformer impedances does not reduce ouverall input impedance below the value stated in MIL-STD-1553B.

  These connections should also be balanced in terms of length, shape and area.

Marconi Circuit Technology Corporation
160 Smith Street, Farmingdale, New York 11735
(516) 293-8636/FAX: (516) 293-0061