CT2N7002E-R3

N-Channel Enhancement MOSFET

Features

- Drain-Source Breakdown Voltage V_{DSS} 60 V
- Drain-Source On-Resistance

  $R_{DS(ON)}$ 4.15Ω, at V_{GS}= 10V, I_{DS}= 500mA

  $R_{DS(ON)}$ 4.7Ω, at V_{GS}= 5.0V, I_{DS}= 500mA
- Continuous Drain Current at T_A=25˚C,I_D = 500mA
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free
- ESD protection

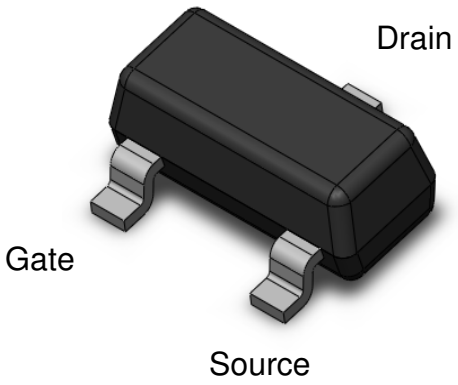
Description

The CT2N7002E-R3 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

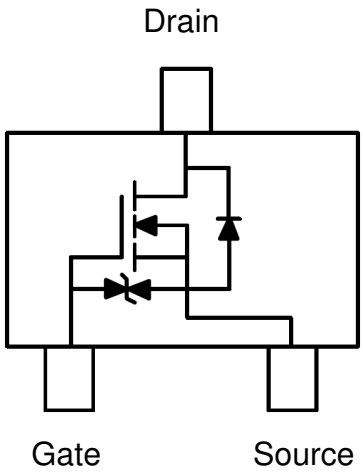
Applications

- Cellular phone
- Notebook
- Power management

Package Outline



Schematic



Absolute Maximum Rating at 25ºC

Symbol	*Parameters*	*Ratings*	*Units*	*Notes*
V_{DS}	Drain-Source Voltage	60	V	
V_{GS}	Gate-Source Voltage	±20	V	
I_D	Continuous Drain Current @T_A=25˚C	500	mA	1
I_{DM}	Pulsed Drain Current	1200	mA	1
P_D	Total Power Dissipation @T_A=25˚C	0.35	W	2
T_{STG}	Storage Temperature Range	-55 to 150	ºC	
T_J	Operating Junction Temperature Range	-55 to 150	ºC	

Thermal Characteristics

Symbol	*Parameters*	*Test Conditions*	*Min*	*Typ*	*Max*	*Units*	*Notes*
$R_{\Theta JA}$	Thermal Resistance Junction-Ambient (t=10s)		-	360	-	ºC /W	1,4

Electrical Characteristics T_A = 25℃ (unless otherwise specified)

Static Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= 250μA	60	-	-	V	
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 60V, V_{GS} = 0V	-	-	1	μA	
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±16V, V_{DS} = 0V	-	-	10	μA	

On Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS} = 10V, I_D = 500mA	-	4.15	7.5	Ω	3
		V_{GS} = 5.0V, I_D = 500mA	-	4.7	7.5	Ω	
$V_{GS(TH)}$	Gate-Source Threshold Voltage	V_{GS} = V_{DS}, I_D =250μA	1.0	2.0	3.0	V	3

Dynamic Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
C_{ISS}	Input Capacitance	V_{DS} = 25V ,	-	17	-	pF	
C_{OSS}	Output Capacitance	V_{GS} = 0V,	-	6	-		
C_{RSS}	Reverse Transfer Capacitance	f=1MHz	-	10	-		

Switching Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$T_{D(ON)}$	Turn-On Delay Time	V_{DS} = 15V , V_{GS} = 10V, R_G = 25Ω, I_D =500mA	-	1.4	-	ns	
T_R	Rise Time		-	16.3	-		
$T_{D(OFF)}$	Turn-Off Delay Time		-	4.4	-		
T_F	Fall Time		-	10			
Q_G	Total Gate Charge	V_{DS} = 15V , V_{GS} = 5V, I_D = 500mA	-	0.06	-	nC	
Q_{GS}	Gate-Source Charge		-	0.43	-		
Q_{GD}	Gate-Drain (Miller) Charge		-	0.12	-		

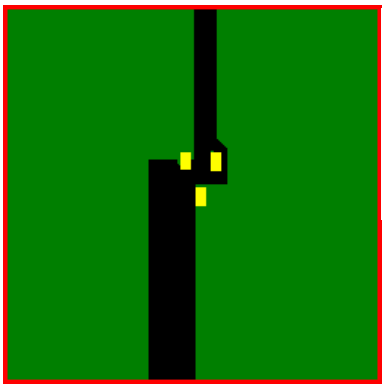
Drain-Source Diode Characteristics

Symbol	*Parameters*	*Test Conditions*	*Min*	*Typ*	*Max*	*Units*	*Notes*
V_{SD}	Body Diode Forward Voltage	V_{GS} = 0V, I_D = 500mA		0.96	1.2	V	
I_{SD}	Body Diode Continuous Current				500	mA	1

Note:

1. The power dissipation is limited by 150℃ junction temperature.

2. Device mounted on a glass-epoxy board



FR-4

25.4 × 25.4 mm .

2 Oz Copper

Actual Size

3. The data tested by pulsed , pulse width ≦ 300μs , duty cycle ≦ 2%

4. Thermal Resistance follow JESD51-3.

Typical Characteristic Curves

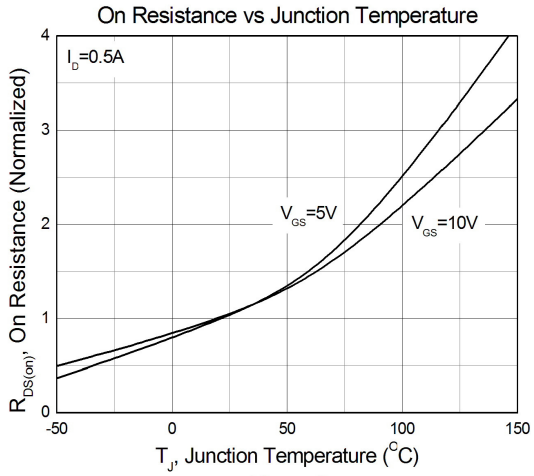


Figure 1

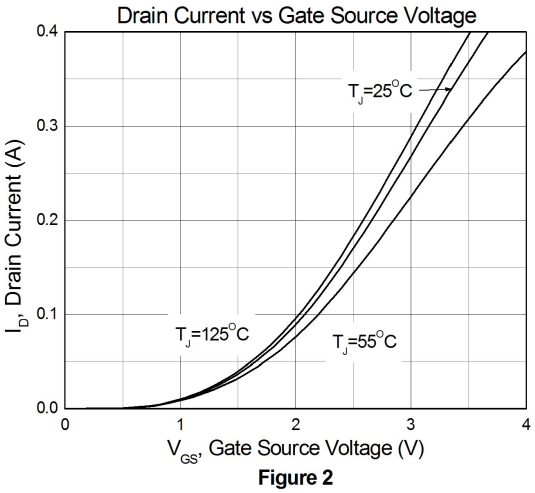


Figure 2

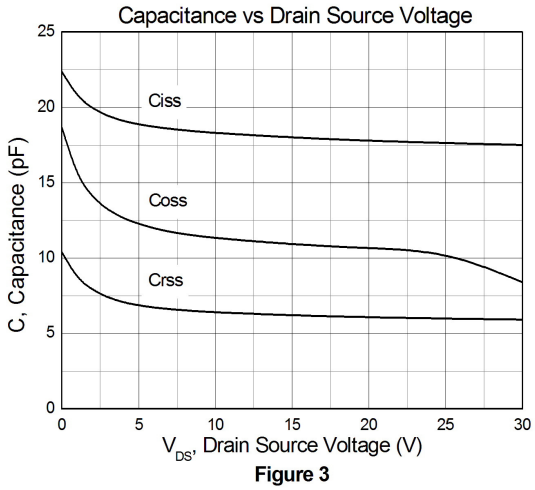


Figure 3

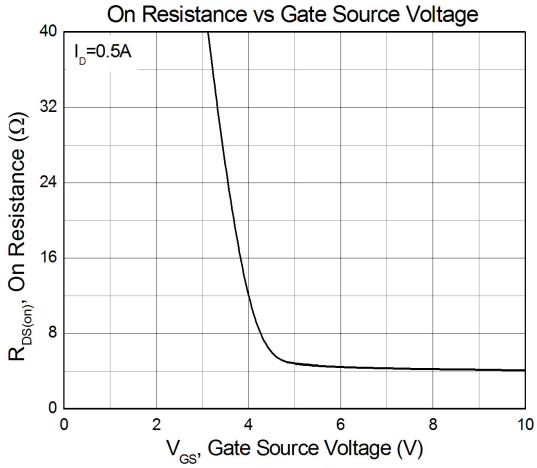


Figure 4

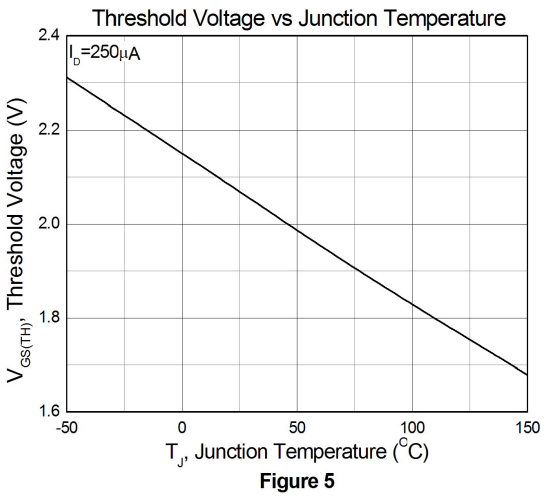


Figure 5

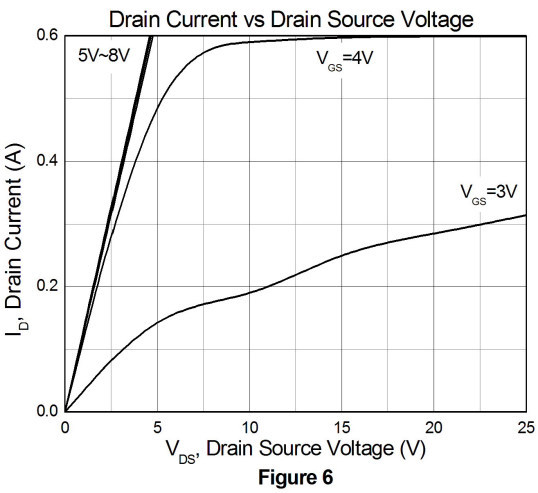


Figure 6

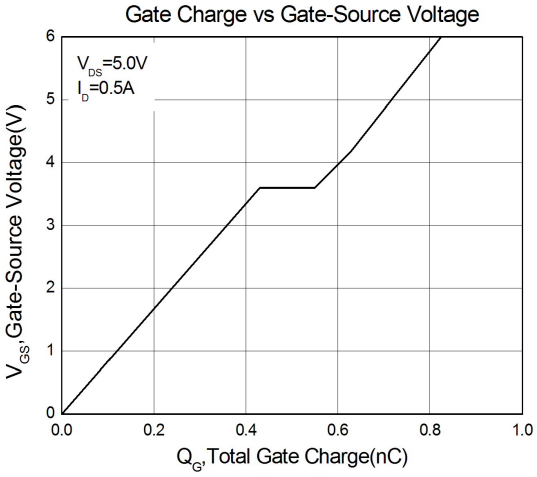


Figure 7

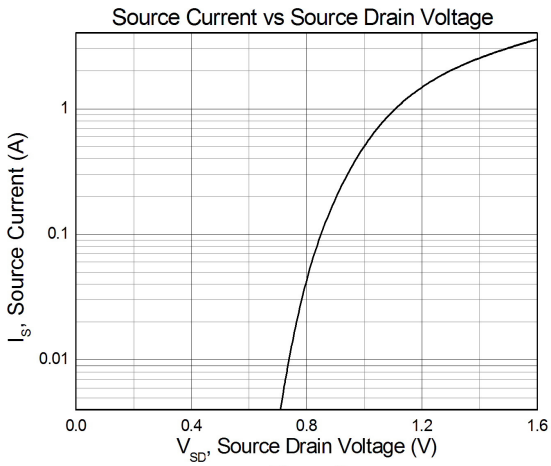


Figure 8

Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

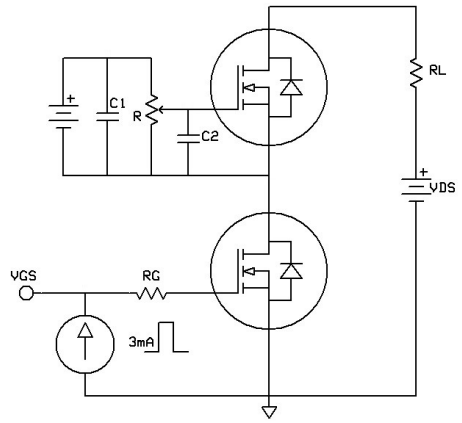


Figure 10: Gate Charge Waveform

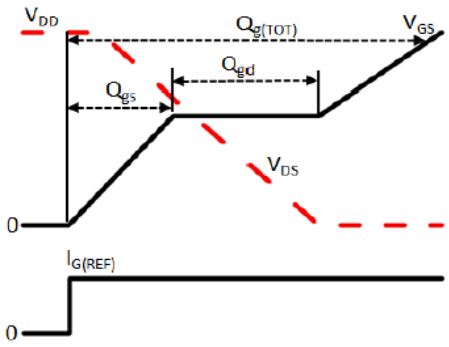


Figure 11: Switching Time Test Circuit

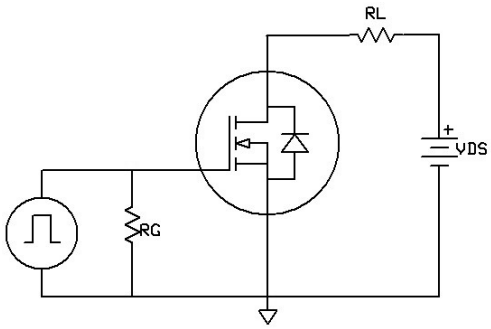
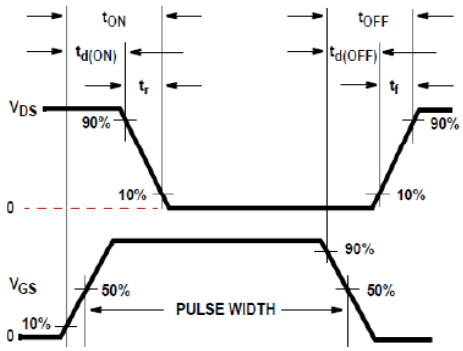
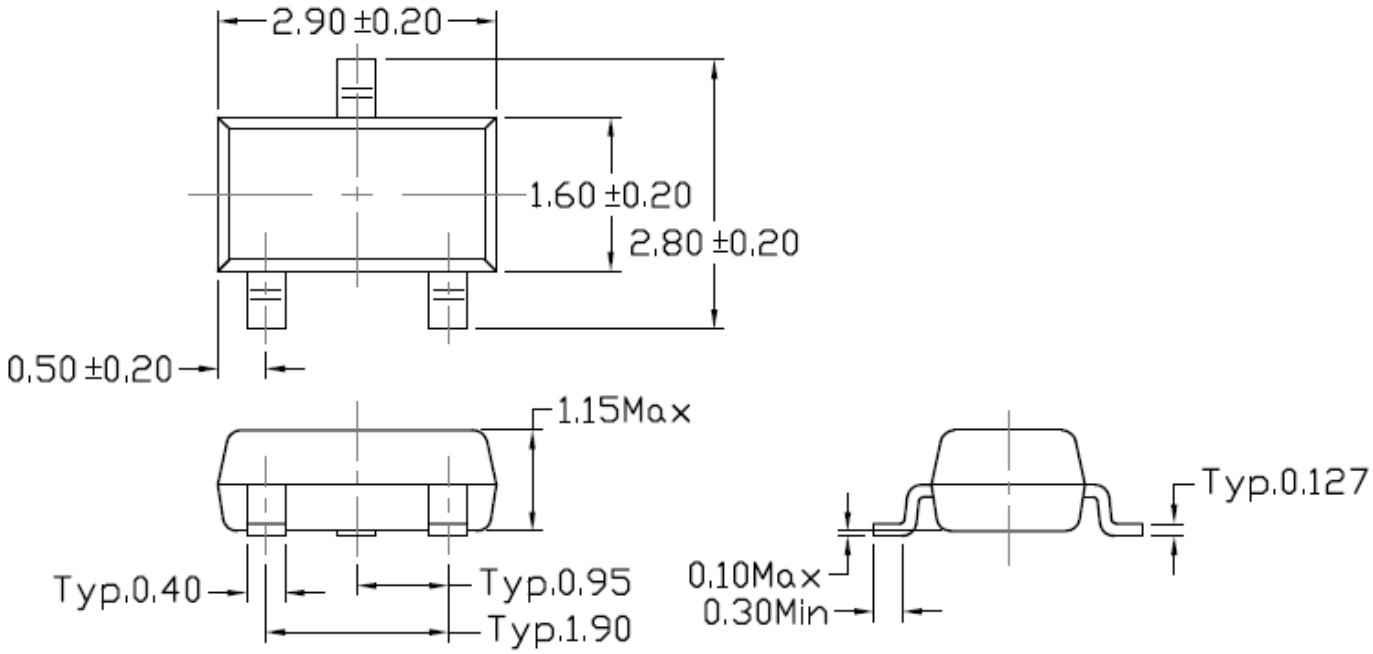


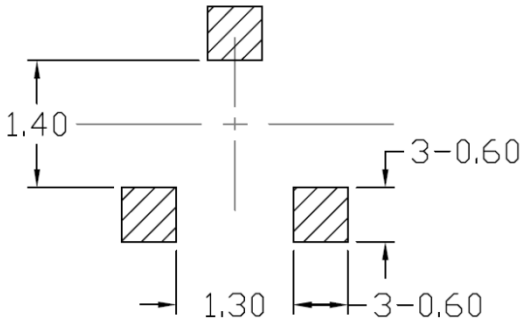
Figure 12: Switching Time Waveform



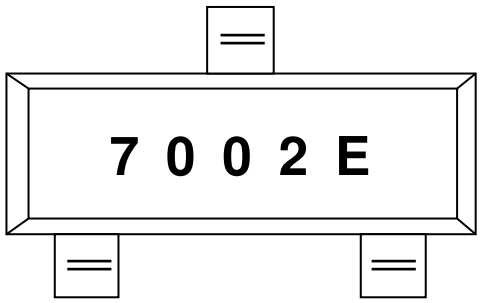
Package Dimension(SC-59)



Recommended pad layout for surface mount leadform



Marking Information

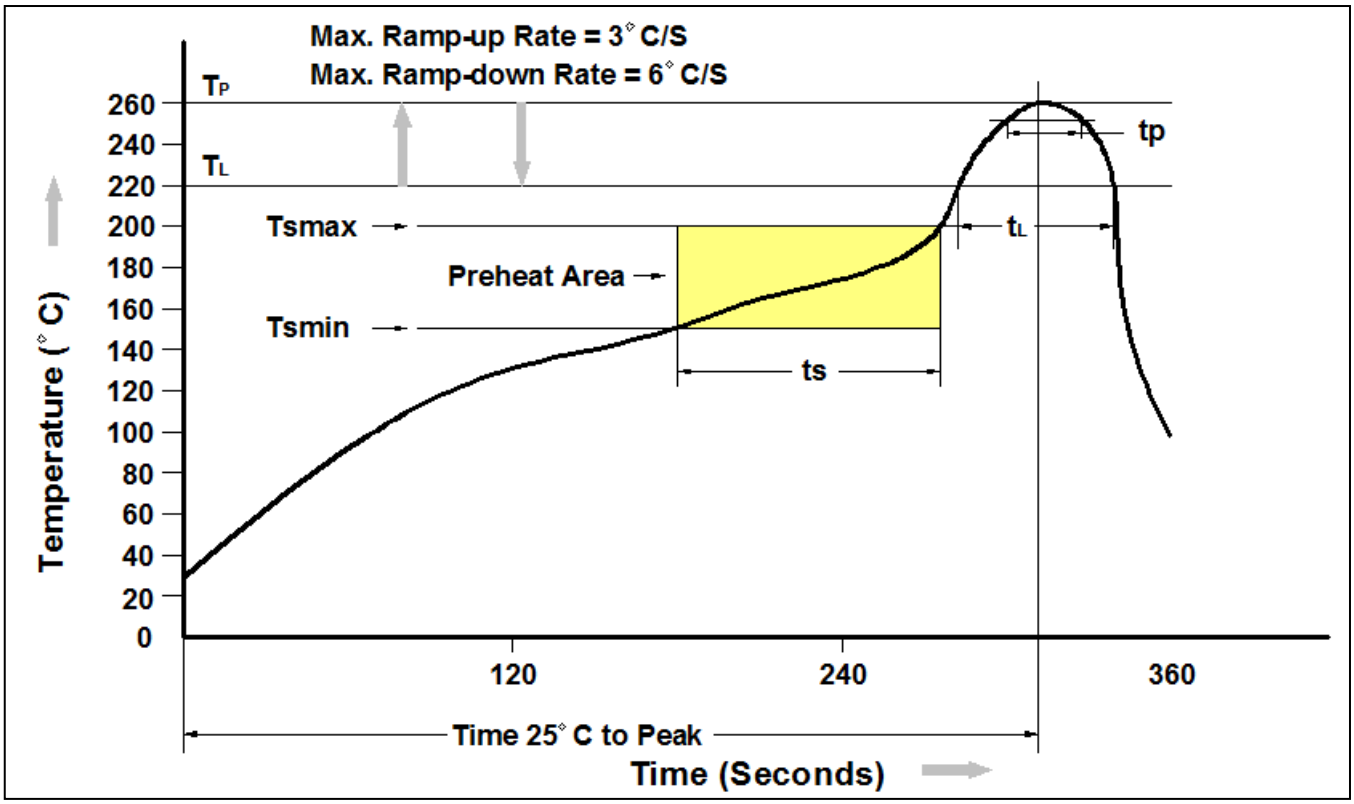


7002E : Device Number

Ordering Information

Part Number	*Description*	*Quantity*
CT2N7002E-R3	SC-59 Reel	3000 pcs

Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150℃
Temperature Max. (Tsmax)	200℃
Time (ts) from (Tsmin to Tsmax)	60-120 seconds
Ramp-up Rate (t_L to t_P)	3℃/second max.
Liquidous Temperature (T_L)	217℃
Time (t_L) Maintained Above (T_L)	60 – 150 seconds
Peak Body Package Temperature	260℃ +0℃ / -5℃
Time (t_P) within 5℃ of 260℃	30 seconds
Ramp-down Rate (T_P to T_L)	6℃/second max
Time 25℃ to Peak Temperature	8 minutes max.

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