CT453

XtremeSense™ TMR Coreless, Differential, and Contactless Current Sensor with Programmable Gain

FEATURES AND BENEFITS

- User-programmable field range:
  - □ 6 to 24 mT
- Preset magnetic field ranges:
  - □ 0 to 6 mT
  - □ ±6 mT
- Linear analog output voltage
- Common mode field rejection: –50 dB
- 1 MHz bandwidth
- Response time: <300 ns
- Reference voltage output for unipolar/bipolar field measurements
- Supply voltage: 3.0 to 3.6 V
- Low noise performance
- Filter pin to reduce noise on output
- Package options:
  - □ 8-lead SOIC
  - □ 8-lead TSSOP

APPLICATIONS

- Solar/power inverters
- Battery management systems
- Industrial equipment
- PFC systems
- Power utility meters
- Power conditioner
- DC/DC converters/power supplies

DESCRIPTION

The CT453 is a high-bandwidth and low-noise integrated zero-loss contactless current sensor that uses Allegro patented XtremeSense TMR technology to enable high-accuracy current measurements for many consumer, enterprise, and industrial applications. It supports two field ranges where the CT453 senses and translates the magnetic field into a linear analog output voltage. It achieves a total error output of less than ±1.0% over voltage and temperature.

This coreless current sensor is not only small in size and simple to design, but it also provides effective common mode field rejection of more than –50 dB. This enables the CT453 to have greater than 90% immunity to stray magnetic fields, thus having almost no impact on the accuracy of the current measurement.

The device has less than 300 ns output response time while the current consumption is about 6.0 mA. The CT453 is equipped with a filter function to reduce the noise on the output pin.

The CT453 is assembled in an 8-lead SOIC package and a low-profile, industry-standard 8-lead TSSOP package that are both green and RoHS compliant.

PACKAGES:

8-lead SOIC 8-lead TSSOP

Not to scale

FUNCTIONAL BLOCK DIAGRAMS

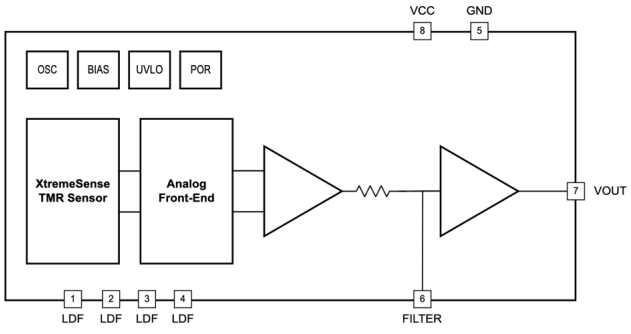

Figure 1: CT453 Functional Block Diagram for SOIC-8

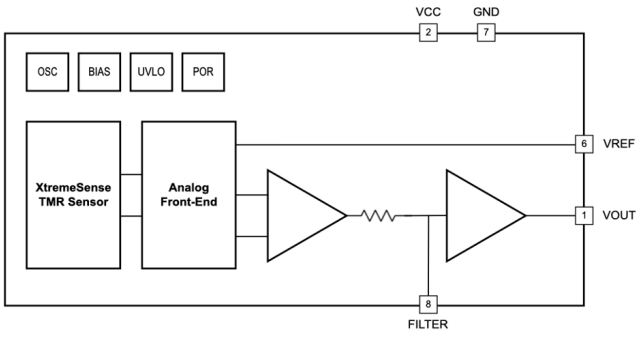

Figure 2: CT453 Functional Block Diagram for TSSOP-8

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SELECTION GUIDE

Part Number	Automotive Grade	Range (mT)	Operating Temperature Range (°C)	Package	Packing
BIPOLAR SENSITIVITY					
CT453-H06MRSN08	–	±6	–40 to 125	8-lead SOIC 4.89 mm × 6.00 mm × 1.62 mm	Tape and Reel
CT453-H06MRTS08	–	±6	–40 to 125	8-lead TSSOP 3.00 mm × 6.40 mm × 1.10 mm	Tape and Reel
UNIPOLAR SENSITIVITY					
CT453-H06DRSN08	–	6	–40 to 125	8-lead SOIC 4.89 mm × 6.00 mm × 1.62 mm	Tape and Reel
CT453-H06DRTS08	–	6	–40 to 125	8-lead TSSOP 3.00 mm × 6.40 mm × 1.10 mm	Tape and Reel
PROGRAMMABLE SENSITIVITY					
CT453-H00MRSN08	–	±6 to ±24	–40 to 125	8-lead SOIC 4.89 mm × 6.00 mm × 1.62 mm	Tape and Reel
CT453-H00DRSN08	–	6 to 24			
CT453-H00MRTS08	–	±6 to ±24	–40 to 125	8-lead TSSOP 3.00 mm × 6.40 mm × 1.10 mm	Tape and Reel
CT453-H00DRTS08	–	6 to 24			

EVALUATION BOARD SELECTION GUIDE

Part Number	Magnetic Field Range (mT)	Current Carrying Conductor	Operating Temperature Range (°C)	Package
CTD453-BB-06U	0 to 6	Busbar	–40 to 125	8-lead SOIC 4.89 mm × 6.00 mm × 1.62 mm
CTD453-BB-06B	±6			
CTD453-PT-06U	0 to 6	PCB Trace		
CTD453-PT-06B	±6			

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ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage Strength	V_{CC}		–0.3 to 6.0	V
Analog Input/Output Pins Maximum Voltage	$V_{I/O}$		–0.3 to V_{CC} + 0.3 [2]	V
Electrostatic Discharge Protection Level	ESD	Human Body Model (HBM) per JESD22-A114	±2.0 (min)	kV
		Charged Device Model (CDM) per JESD22-C101	±0.5 (min)	kV
Junction Temperature	T_J		–40 to 150	°C
Storage Temperature	T_{STG}		–65 to 155	°C
Lead Soldering Temperature	T_L	10 seconds	260	°C

[1] Stresses exceeding the absolute maximum ratings may damage the CT453 and may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.
[2] The lower of V_{CC} + 0.3 V or 6.0 V.

RECOMMENDED OPERATING CONDITIONS [1]

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Supply Voltage Range	V_{CC}		3.0	3.3	3.6	V
Output Voltage Range	V_{OUT}		0	–	V_{CC}	V
Output Current	I_{OUT}		–	–	±1.0	mA
Operating Ambient Temperature	T_A		–40	25	125	°C

[1] The Recommended Operating Conditions table defines the conditions for actual operation of the CT453. Recommended operating conditions are specified to ensure optimal performance to the specifications. Allegro does not recommend exceeding them or designing to absolute maximum ratings.

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APPLICATION DIAGRAMS

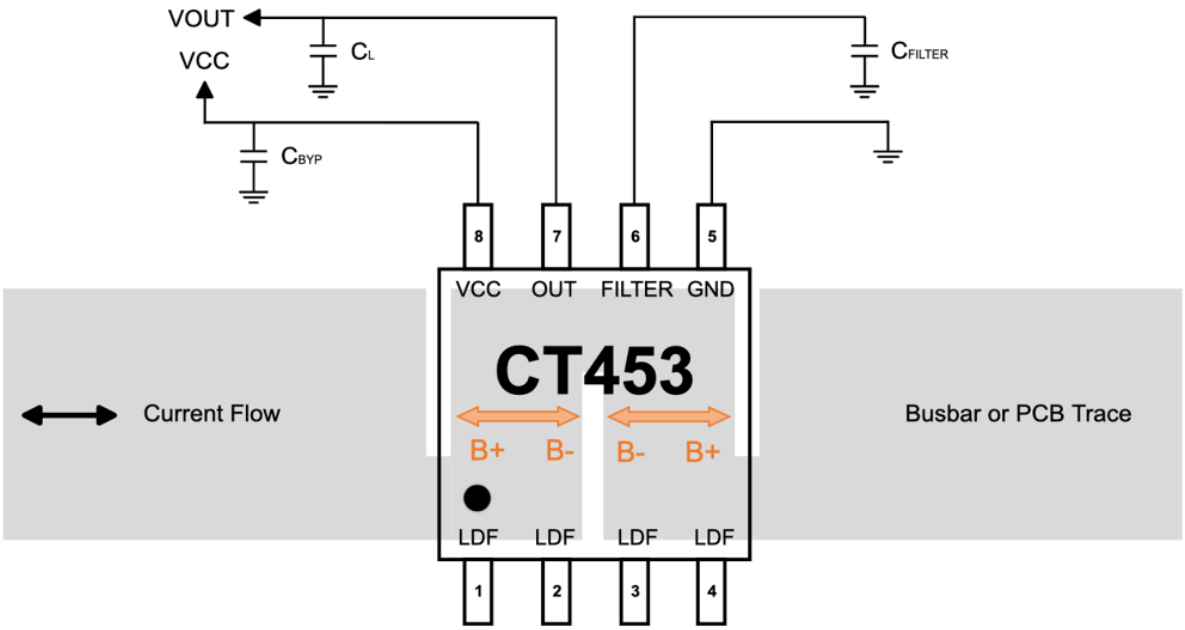

Figure 3: CT453 Application Diagram for SOIC-8

Table 1: Recommended External Components

Component	Description	Vendor and Part Number	Min.	Typ.	Max.	Unit
C_{BYP}	1.0 µF, X5R or better	Murata GRM155C81A105KA12	–	1.0	–	µF
C_{FILTER}	Various, X5R or better	Murata	–	Figure 16	–	pF

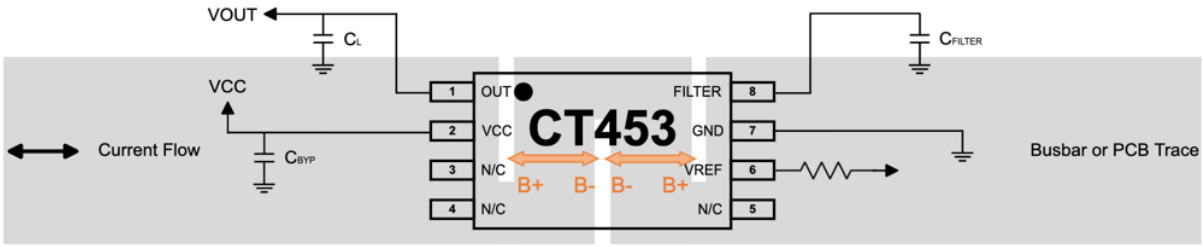

Figure 4: CT453 Application Diagram for TSSOP-8

Table 2: Recommended External Components

Component	Description	Vendor and Part Number	Min.	Typ.	Max.	Unit
C_{BYP}	1.0 µF, X5R or better	Murata GRM155C81A105KA12	–	1.0	–	µF
C_{FILTER}	Various, X5R or better	Murata	–	Figure 16	–	pF
R_{VREF}	10 kΩ resistor	Various	–	10	–	kΩ

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PINOUT DIAGRAMS AND TERMINAL LISTS

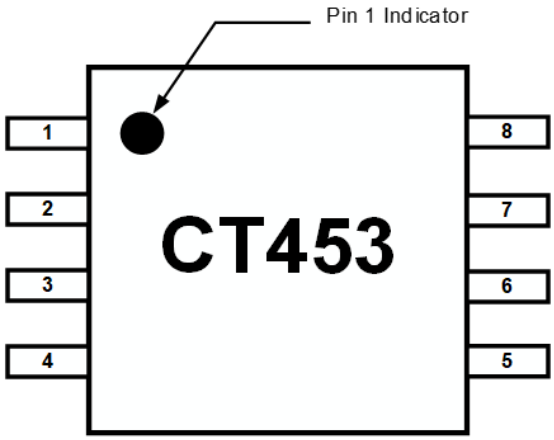

Figure 5: CT453 Pinout Diagram for 8-lead SOIC Package (Top-Down View)

Terminal List

Number	Name	Function
1, 2, 3, 4	LDF	Lead frame Pin – A single (1) LDF pin should be connected to GND. The other three (3) LDF pins should be left unconnected to avoid ground loops through the lead frame.
5	GND	Ground.
6	FILTER	Filter pin to improve noise performance by connecting an external capacitor to set the cutoff frequency. No connect if the FILTER pin is not used.
7	OUT	Analog output voltage that represents the measured current/field.
8	VCC	Supply voltage.

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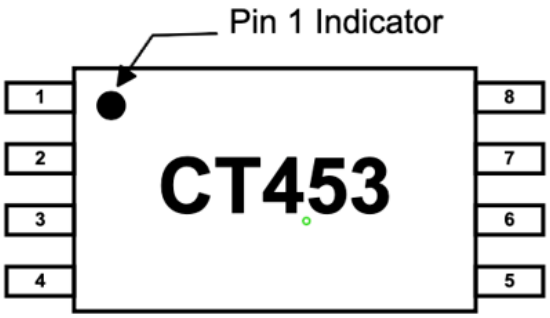

Figure 6: CT453 Pinout Diagram for 8-lead TSSOP Package (Top-Down View)

Terminal List

Number	Name	Function
1	OUT	Analog output voltage that represents the measured current/field.
2	VCC	Supply voltage.
3, 4, 5	NC	No connect (do not use).
6	VREF	Reference voltage output. If not used, then do not connect.
7	GND	Ground.
8	FILTER	Filter pin to improve noise performance by connecting an external capacitor to set the cutoff frequency. No connect if the FILTER pin is not used.

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ELECTRICAL CHARACTERISTICS: Valid for V_{CC} = 3.0 to 3.6 V, C_{BYP} = 1.0 µF, and T_A = –40°C to 125°C, typical values are V_{CC} = 3.3 V and T_A = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLIES						
Supply Current	I_{CC}	f_{BW} = 1 MHz, no load, B_{OP} = 0 mT	–	6.0	9.0	mA
OUT Maximum Drive Capability	I_{OUT}	OUT covers 10% to 90% of V_{CC} span	–1.0	–	+1.0	mA
OUT Capacitive Load	C_{L_OUT}		–	–	100	pF
OUT Resistive Load	R_{L_OUT}		–	100	–	kΩ
Internal Filter Resistance [1]	R_{FILTER}		–	15	–	kΩ
Power Supply Rejection Ratio [1]	PSRR		–	35	–	dB
Sensitivity Power Supply Rejection Ratio [1]	SPSRR		–	35	–	dB
Offset Power Supply Rejection Ratio [1]	OPSRR		–	40	–	dB
Common Mode Field Rejection Ratio [1]	CMFRR		–	–50	–	dB
ANALOG OUTPUT (OUT)						
OUT Voltage Linear Range	V_{OUT}	V_{SIG_AC} = ±2.00 V, V_{SIG_DC} = +4.00 V	0.65	–	2.65	V
Output High Saturation Voltage	V_{OUT_SAT}	T_A = 25°C	V_{CC} – 0.30	V_{CC} – 0.25	–	V
REFERENCE VOLTAGE (VREF) FOR TSSOP-8 ONLY						
Reference Voltage	V_{REF}	Unipolar variant	–	0.65	–	V
		Bipolar variant	–	1.65	–	V
VREF Maximum Drive Capability	I_{VREF}		–50	–	50	µA
VREF Capacitive Load	C_{L_VREF}		–	–	10	pF
VREF Resistive Load	R_{L_VREF}		–	10	–	kΩ
TIMINGS						
Power-On Time	t_{ON}	V_{CC} ≥ 4.0 V	–	100	200	µs
Rise Time [1]	t_{RISE}	B_{OP} = $B_{OP(MAX)}$, T_A = 25°C, C_L = 100 pF	–	200	–	ns
Response Time [1]	$t_{RESPONSE}$	B_{OP} = $B_{OP(MAX)}$, T_A = 25°C, C_L = 100 pF	–	300	–	ns
Propagation Delay [1]	t_{DELAY}	B_{OP} = $B_{OP(MAX)}$, T_A = 25°C, C_L = 100 pF	–	250	–	ns
PROTECTION						
Undervoltage Lockout	V_{UVLO}	Rising V_{CC}	–	2.50	–	V
		Falling V_{CC}	–	2.45	–	V
UVLO Hysteresis	V_{UV_HYS}		–	50	–	mV

[1] Guaranteed by design and characterization; not tested in production.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3 V, T_A = 25°C, and C_{BYP} = 1.0 µF (unless otherwise specified)

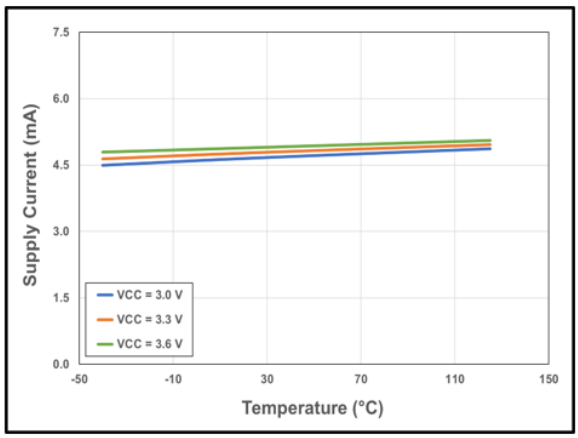

Figure 7: CT453 Supply Current vs. Temperature vs. Supply Voltage

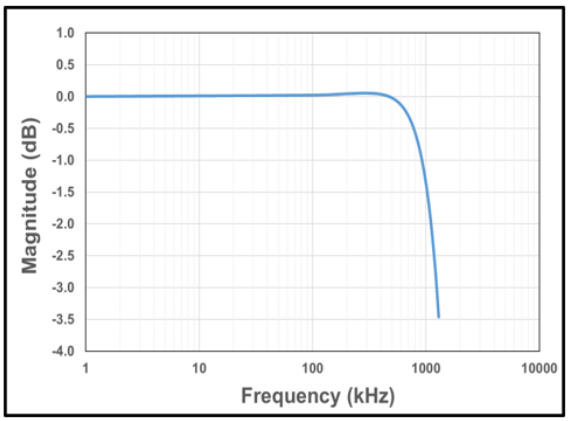

Figure 8: CT453 Bandwidth with C_{FILTER} = 1.0 pF

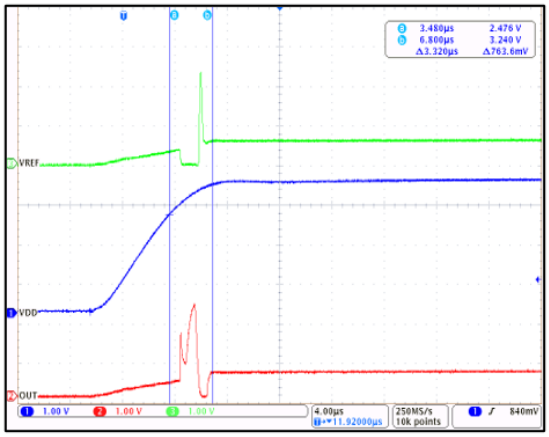

Figure 9: CT453 Startup Waveforms for V_{OQ} = 0.65 V (Unipolar Field)

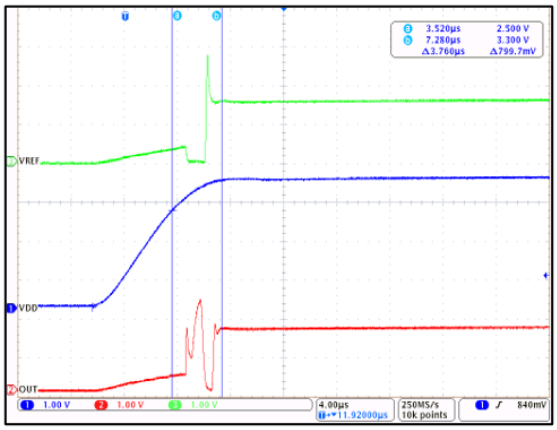

Figure 10: CT453 Startup Waveforms for V_{OQ} = 1.65 V (Bipolar Field)

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CT453-x06DR: 0 to 6 mT – ELECTRICAL CHARACTERISTICS: Valid for V_{CC} = 3.0 to 3.6 V, C_{BYP} = 1.0 µF, and T_A = –40°C to 125°C, typical values are V_{CC} = 3.3 V and T_A = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Magnetic Field Range	B_{RNG}		0	–	6	mT
Voltage Output Quiescent	V_{OQ}	T_A = 25°C, B_{OP} = 0 mT	0.645	0.650	0.655	V
Sensitivity	S	$B_{RNG(MIN)} < B_{OP} < B_{RNG(MAX)}$	–	333.3	–	mV/mT
Bandwidth [1]	f_{BW}	Small Signal = –3 dB	–	1.0	–	MHz
Noise [1]	e_N	T_A = 25°C, f_{BW} = 100 kHz	–	0.81	–	mV_{RMS}
			–	2.42	–	$µT_{RMS}$
OUT ACCURACY PERFORMANCE						
Non-Linearity Error	E_{LIN}		–	±0.2	–	% FS
Sensitivity Error	E_{SENS}		–	±0.2	–	% FS
Offset Voltage	V_{OFFSET}	B_{OP} = 0 mT	–	±0.4	–	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift	E_{TOT_DRIFT}		–	±1.0	–	% FS

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS FOR CT453-x06DR

V_{CC} = 3.3 V, T_A = 25°C, and C_{BYP} = 1.0 µF (unless otherwise specified)

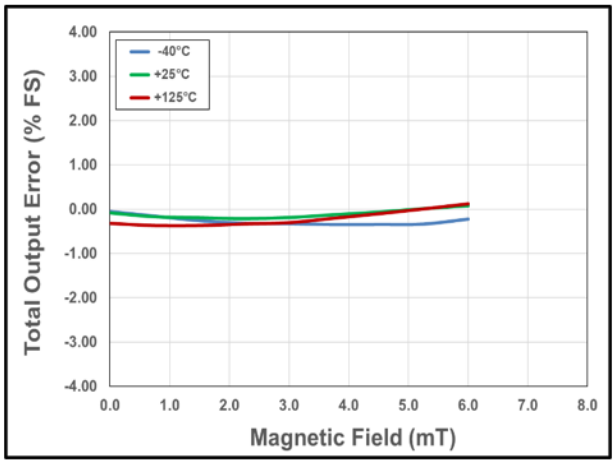

Figure 11: Total Output Error vs. B Field vs. Temperature

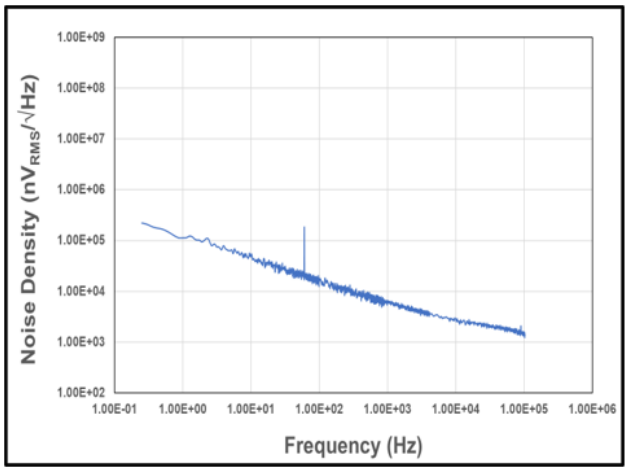

Figure 12: Noise Density vs. Frequency

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CT453-x06MR: ±6 mT – ELECTRICAL CHARACTERISTICS: Valid for V_{CC} = 3.0 to 3.6 V, C_{BYP} = 1.0 µF, and T_A = –40°C to 125°C, typical values are V_{CC} = 3.3 V and T_A = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Magnetic Field Range	B_{RNG}		–6	–	6	mT
Voltage Output Quiescent	V_{OQ}	T_A = 25°C, B_{OP} = 0 mT	1.645	1.650	1.655	V
Sensitivity	S	$B_{RNG(MIN)} < B_{OP} < B_{RNG(MAX)}$	–	166.7	–	mV/mT
Bandwidth [1]	f_{BW}	Small Signal = –3 dB	–	1.0	–	MHz
Noise [1]	e_N	T_A = 25°C, f_{BW} = 100 kHz	–	0.45	–	mV_{RMS}
			–	2.69	–	$µT_{RMS}$
OUT ACCURACY PERFORMANCE						
Non-Linearity Error	E_{LIN}		–	±0.1	–	% FS
Sensitivity Error	E_{SENS}		–	±0.2	–	% FS
Offset Voltage	V_{OFFSET}	B_{OP} = 0 mT	–	±0.4	–	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift	E_{TOT_DRIFT}		–	±1.0	–	% FS

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS FOR CT453-x06MR

V_{CC} = 3.3 V, T_A = 25°C, and C_{BYP} = 1.0 µF (unless otherwise specified)

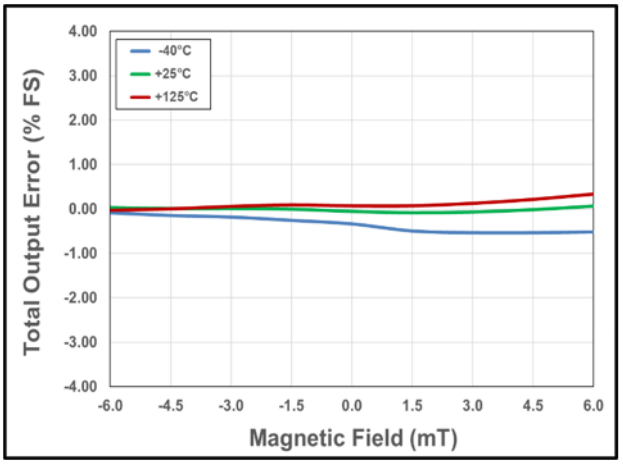

Figure 13: Total Output Error vs. B Field vs. Temperature

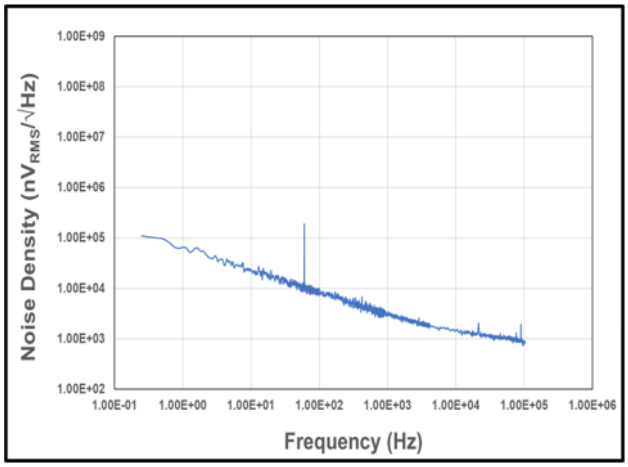

Figure 14: Noise Density vs. Frequency

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CT453-x00MR: Programmable Gain – ELECTRICAL CHARACTERISTICS: Valid for V_{CC} = 3.0 to 3.6 V, C_{BYP} = 1.0 µF, and T_A = –40°C to 125°C, typical values are V_{CC} = 3.3 V and T_A = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Programmable Magnetic Field Range	B_{PRNG}		±6	–	±8	mT
			±12	–	±24	mT
Voltage Output Quiescent	V_{OQ}	T_A = 25°C, B_{OP} = 0 mT	1.645	1.650	1.655	V
Maximum Programmable Sensitivity	S_{PMAX}	$B_{RNG(MIN)} < B_{OP} < B_{RNG(MAX)}$	–	333.3	–	mV/mT
Minimum Programmable Sensitivity	S_{PMIN}	$B_{RNG(MIN)} < B_{OP} < B_{RNG(MAX)}$	–	83.4	–	mV/mT
Bandwidth [1]	f_{BW}	Small Signal = –3 dB	–	1.0	–	MHz
OUT ACCURACY PERFORMANCE						
Non-Linearity Error	E_{LIN}		–	±0.2	–	% FS
Sensitivity Error	E_{SENS}		–	±0.3	–	% FS
Offset Voltage	V_{OFFSET}	B_{OP} = 0 mT	–	±0.4	–	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift	E_{TOT_DRIFT}		–	±1.0	–	% FS

[1] Guaranteed by design and characterization; not tested in production.

Calibration Description

The CT453-x00MR is factory-trimmed for sensitivity and offset temperature drift. The sensor provides the ability to adjust gain to allow for all the mechanical tolerances during manufacturing. Gain calibration is recommended to be performed at room temperature (25°C) using the Allegro CTC4000 Calibration Box.

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CT453-x00DR: Programmable Gain – ELECTRICAL CHARACTERISTICS: Valid for V_{CC} = 3.0 to 3.6 V, C_{BYP} = 1.0 µF, and T_A = –40°C to 125°C, typical values are V_{CC} = 3.3 V and T_A = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Programmable Magnetic Field Range	B_{PRNG}		6	–	8	mT
			12	–	24	mT
Voltage Output Quiescent	V_{OQ}	T_A = 25°C, B_{OP} = 0 mT	0.645	0.650	0.655	V
Maximum Programmable Sensitivity	S_{PMAX}	$B_{RNG(MIN)} < B_{OP} < B_{RNG(MAX)}$	–	666.7	–	mV/mT
Minimum Programmable Sensitivity	S_{PMIN}	$B_{RNG(MIN)} < B_{OP} < B_{RNG(MAX)}$	–	166.7	–	mV/mT
Bandwidth [1]	f_{BW}	Small Signal = –3 dB	–	1.0	–	MHz
OUT ACCURACY PERFORMANCE						
Non-Linearity Error	E_{LIN}		–	±0.3	–	% FS
Sensitivity Error	E_{SENS}		–	±0.3	–	% FS
Offset Voltage	V_{OFFSET}	B_{OP} = 0 mT	–	±0.3	–	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift	E_{TOT_DRIFT}		–	±1.0	–	% FS

[1] Guaranteed by design and characterization; not tested in production.

Calibration Description

The CT453-x00DR is factory-trimmed for sensitivity and offset temperature drift. The sensor provides the ability to adjust gain to allow for all the mechanical tolerances during manufacturing. Gain calibration is recommended to be performed at room temperature (25°C) using the Allegro CTC4000 Calibration Box.

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FUNCTIONAL DESCRIPTION

Overview

The CT453 is a very high accuracy coreless and contactless current sensor that can sense magnetic fields from 6 to 24 mT. The device has high sensitivity and a wide dynamic range with excellent accuracy (low total output error) across temperature. This current sensor supports two field ranges as standard and can also be user-programmable up to 24 mT:

- 0 to 6 mT
- ±6 mT

The CT453 is also available in a user-programmable variant which enables end-of-line calibration of gain. While the sensor is pre-programmed to adjust sensitivity and offset temperature drift, the ability to adjust gain relaxes mechanical tolerances during sensor mounting.

When current is flowing through a busbar above or below the CT453, the XtremeSense TMR sensor inside the chip senses the field which in turn generates a differential voltage signals that then goes through the Analog Front-End (AFE) to output a current measurement as low as ±1.0% full-scale total output error (E_{OUT}).

The chip is designed to enable a fast response time of 300 ns for the current measurement from the OUT pin as the bandwidth for the CT453 is 1.0 MHz. Even with a high bandwidth, the chip consumes a minimal amount of power.

Linear Output Current Measurement

The CT453 provides a continuous linear analog output voltage which represents the current measurement. The output voltage range of OUT is from 0.65 to 2.65 V with a V_{OQ} of 0.65 V and 1.65 V for unidirectional and bidirectional currents, respectively. Figure 15 illustrates the output voltage range of the OUT pin as a function of the measured current.

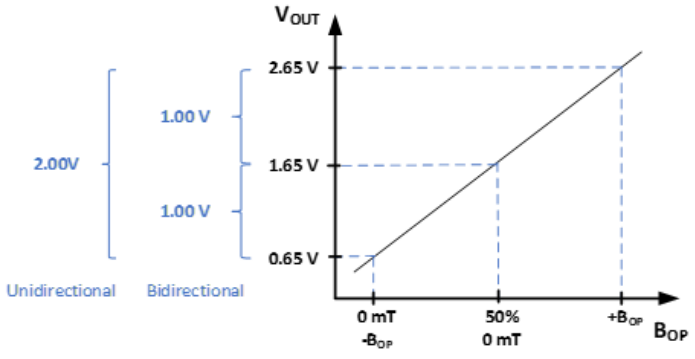

Figure 15: Linear Output Voltage Range (OUT) vs. Measured Magnetic Field (B_{OP})

Voltage Reference Function (VREF)

The CT453 in TSSOP-8 package has a reference voltage (VREF) pin that may be used as an output voltage reference for AC or DC field/current measurements. The VREF pin should be connected to a buffer circuit.

If VREF is not used, then it should be left unconnected.

Filter Function (FILTER)

The CT453 has a pin for the FILTER function which will enable it to improve the noise performance by changing the cutoff frequency. The bandwidth of the CT453 is 1.0 MHz; however, adding a capacitor to the FILTER pin—which will be in-series with an internal resistance of approximately 15 kΩ—will set the cutoff frequency to reduce noise. Figure 16 shows the capacitor values required to achieve different cutoff frequencies.

Experimentally measured bandwidth does not necessarily match the calculated bandwidth value obtained by using the equation $f_{BW} = {}^{1}/_{2\pi RC}$ because of the parasitic capacitances due to PCB manufacturing and layout. This is further impacted by the small, picofarad level C_{FILTER} recommendations.

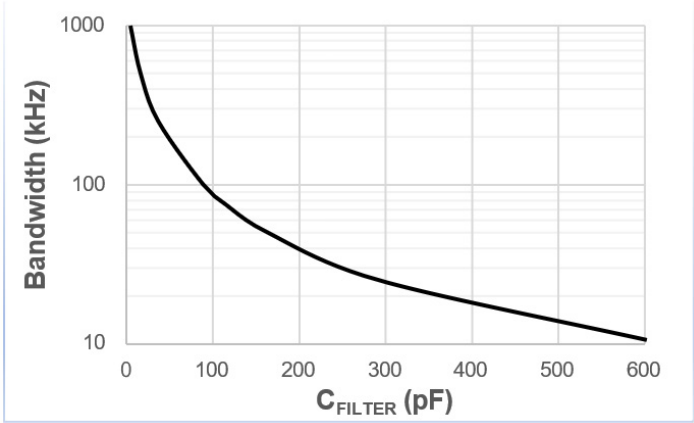

Figure 16: Bandwidth vs. C_{FILTER}

Total Output Error

The Total Output Error (E_{OUT}) is the maximum deviation of the sensor output from the ideal sensor transfer curve over the full temperature range relative to the sensor full scale.

The Total Output Error is measured by performing a full-scale primary current (IP) sweep and measuring V_{OUT} at multiple points.

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$$E_{OUT} = 100 * \frac{\max\left(V_{OUT_{IDEAL}}(I) - V_{OUT}(I)\right)}{F.S.}$$

The Ideal Transfer Curve is calculated based on datasheet parameters as described below.

$$V_{OUT_{IDEAL}}(I_P) = V_{OQ} + S * I_P$$

E_{OUT} incorporates all sources of error and is a function of the sensed current (I_P) from the current sensor.

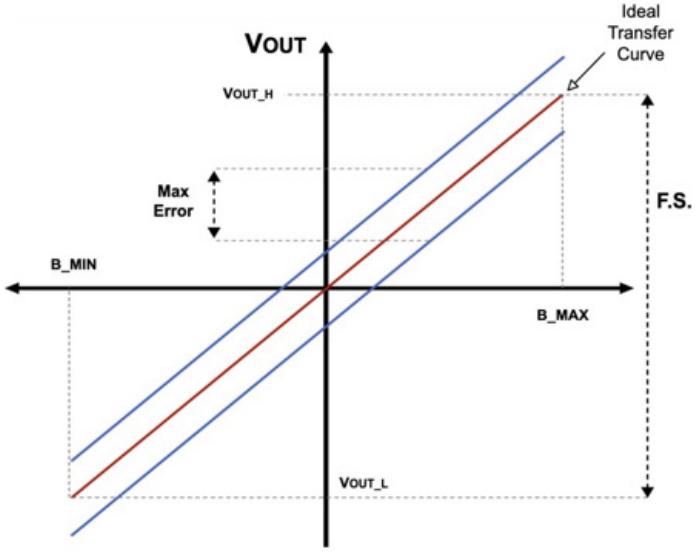

Figure 17: Total Output Error (E_{OUT}) vs. Field (B_{OP})

The CT453 achieves, after gain calibration, a total output error (E_{OUT}) that is less than ±1.0% of Full-Scale (FS) over supply voltage and temperature. It is designed with innovative and proprietary TMR sensors and circuit blocks to provide very accurate magnetic field measurements regardless of the operating conditions.

Common Mode Field Rejection (CMFR) Mode

The CT453 has a built-in CMFR mode that combines the design ease of contactless current sensing with excellent common mode field rejection. This is achieved by placing notches in the current-carrying busbar or PCB trace to generate a differential magnetic field in the vicinity of the CT453 sensor. The current sensor uses two full-bridge XtremeSense TMR sensors to achieve differential magnetic sensing capability, which allows the CT453 to greatly attenuate external magnetic fields and only capture the magnetic field generated by the current flowing in the busbar. Using this technique achieves better than –50 dB of CMFR without compromising the accuracy or the signal-to-noise ratio (SNR) of the CT453.

Figure 18 and Figure 19 shows an example of a 2-layer printed circuit board (PCB) where the CT453 is placed on the top layer of the PCB and the bottom layer is designed to generate differential magnetic fields as the current flows through this trace. The snake-like shape of the PCB trace produces the differential magnetic fields that almost completely eliminates the effects of stray magnetic fields to the CT453. This ensures that the CT453 outputs an accurate output voltage/current measurement to the host system.

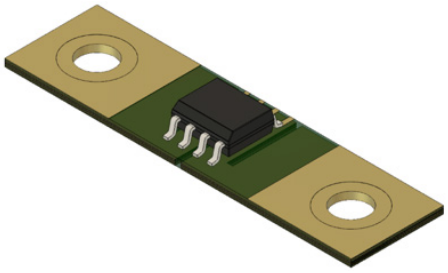

Figure 18: 3D View of CT453 and PCB Trace Design

Figure 19: PCB Trace Design to Generate Differential Magnetic Field for CT453 to Measure

An exploded view of the differential magnetic field generated by the PCB trace is illustrated in Figure 20. It demonstrates the IP+ current generating a clockwise field and goes around the bend or corner of the trace and coming out is IP- with a counter-clockwise field.

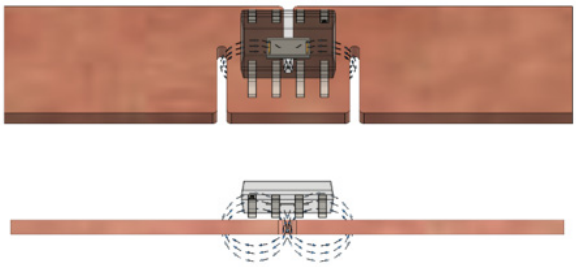

Figure 20: Differential Magnetic Fields Generated Current Through the Busbar (or PCB Trace) and Measured by the CT453

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This concept is not restricted to PCB layers and can be extended to busbars carrying current in the hundreds to thousands of amperes. Figure 21 shows a graphic of the CT453 placed over a busbar that generates differential magnetic fields when 300 A or greater steady-state current through it which will also give CMFR ratio of –50 dB or greater than 90% immunity.

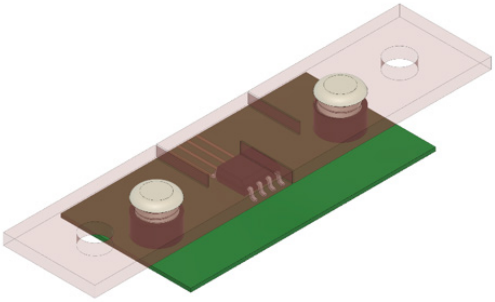

Figure 21: CT453 for Contactless Current Sensing Using Busbar

For more information on how to design the PCB trace and busbar to achieve this CMFR performance, see application note AN134, Fuse Time vs. Current for the CT43x Contact Current Sensors.

Sensitivity Error

The sensitivity error (E_{SENS}) is the sensitivity temperature drift error for unipolar or DC current. It is calculated using the equation below:

$$E_{SENS} = 100 \times \left(\frac{S_{MEASURED}}{S} - 1\right)$$

For bipolar or AC current, the E_{SENS} is calculated by dividing the equation by 2.

Power-On Time (t_{ON})

Power-On Time (t_{ON}) of 100 µs is the amount of time required by CT453 to start up, fully power the chip, and becoming fully operational from the moment the supply voltage is greater than the UVLO voltage. This time includes the ramp-up time and the settling time (within 10% of steady-state voltage under an applied magnetic field) after the power supply has reached the minimum V_{CC}.

Response Time ($t_{RESPONSE}$)

Response Time ($t_{RESPONSE}$) of 300 ns for the CT453 is the time interval between the following terms:

1. When the primary current signal reaches 90% of its final value,
2. When the chip reaches 90% of its output corresponding to the applied current.

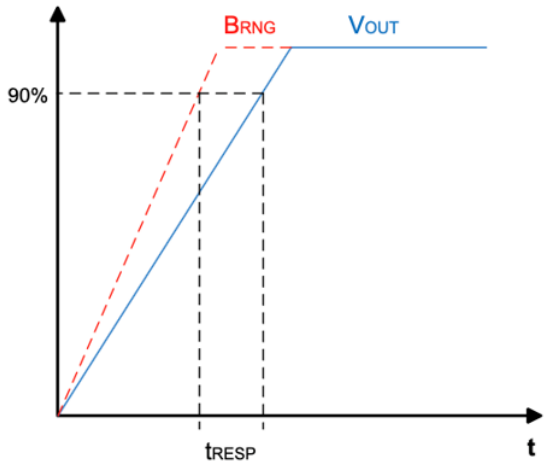

Figure 22: CT453 Response Time Curve

Rise Time (t_{RISE})

Rise Time (t_{RISE}) is the time interval of when it reaches 10% and 90% of the full-scale output voltage. The t_{RISE} of the CT453 is 200 ns.

Propagation Delay (t_{DELAY})

Propagation Delay (t_{DELAY}) is the time difference between these two events:

1. When the primary current reaches 20% of its final value
2. When the chip reaches 20% of its output corresponding to the applied current.

The CT453 has a propagation delay of 250 ns.

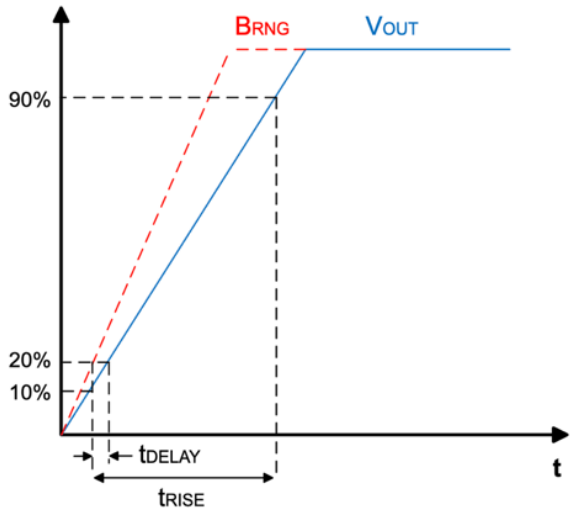

Figure 23: CT453 Propagation Delay and Rise Time Curve

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Undervoltage Lockout (UVLO)

The Undervoltage Lockout protection circuitry of the CT453 is activated when the supply voltage (V_{CC}) falls below 2.45 V. The CT453 remains in a low quiescent state until V_{CC} rises above the UVLO threshold (2.50 V). In this condition where V_{CC} is less than 2.45 V and UVLO is triggered, the output from the CT453 is not valid. Once V_{CC} rises above 4.0 V, then the UVLO is cleared.

Recommended PCB Trace Design

The CT453 requires a different PCB trace or busbar design than the standard current trace or busbar to enable common mode field rejection. Figure 24 and Figure 25 show the shape and design of a PCB trace or busbar.

Other considerations in the PCB layout include the thickness of the trace and the amount of copper to support the current. Also placing the PCB trace on the bottom layer of the board will increase the isolation voltage. The greater distance between the CT453 and the current trace will result in a higher isolation voltage.

For more information on how to design the current-carrying busbar or PCB trace, see AN135 application note, CT453/3 Busbar Design.

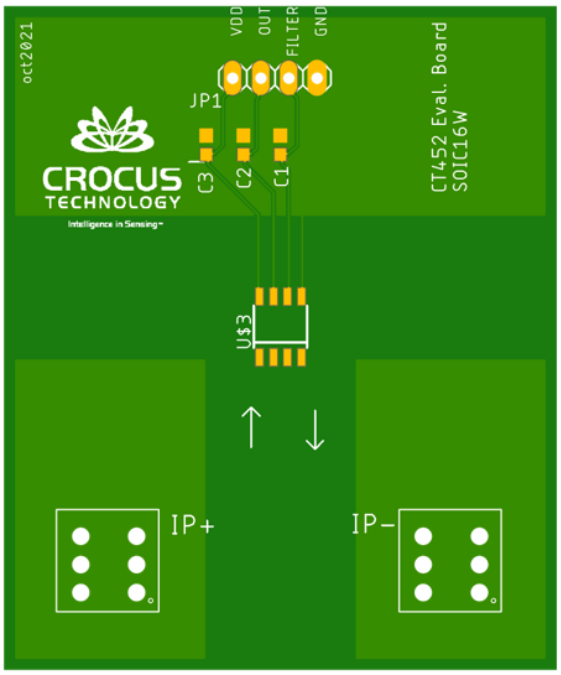

Figure 24: Recommended PCB Layout (Top Layer) for CT453

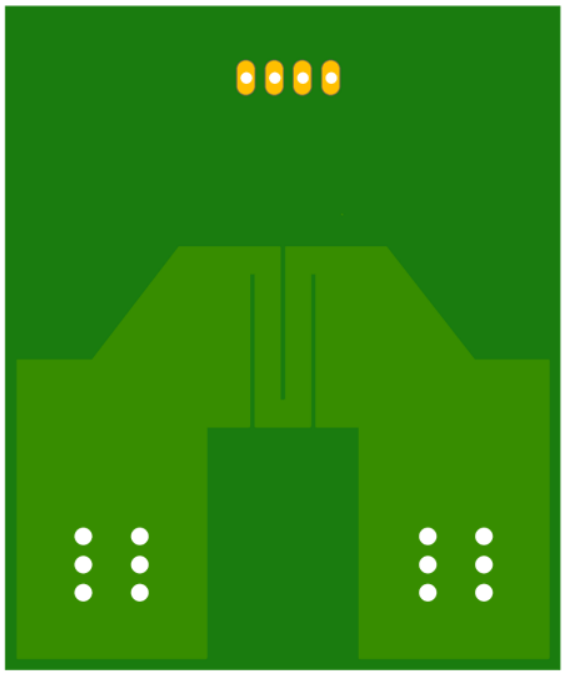

Figure 25: Recommended PCB Layout (Bottom Layer) for CT453

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XtremeSense TMR Current Sensor Location

The XtremeSense TMR current sensor location of the CT453 is shown below. All dimensions in the figures are nominal.

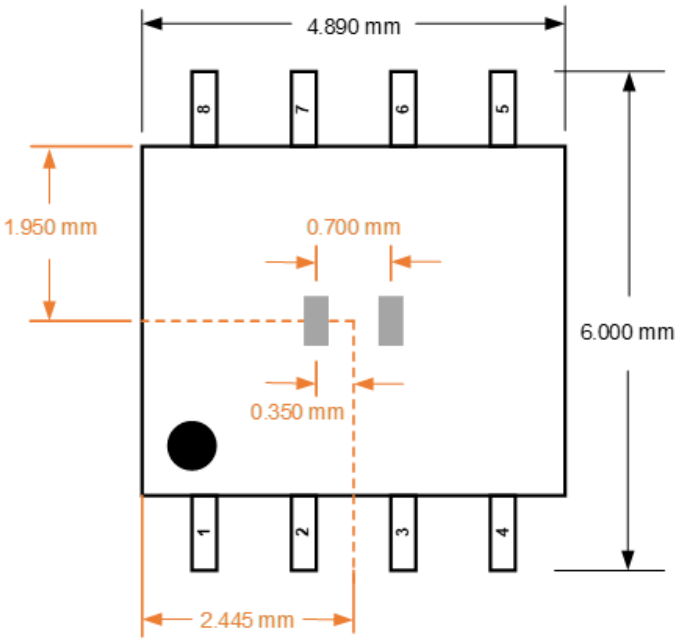

Figure 26: XtremeSense TMR Current Sensor Location in x-y Plane for CT453 in SOIC-8 Package

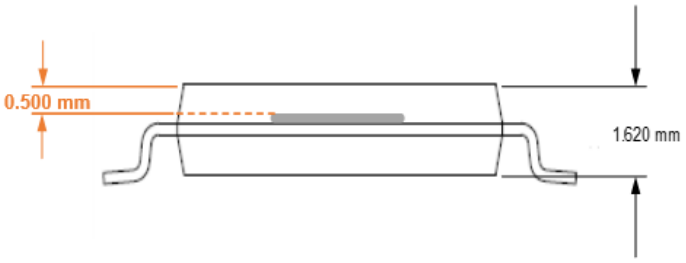

Figure 27: XtremeSense TMR Current Sensor Location in z Dimension for CT453 in SOIC-8 Package

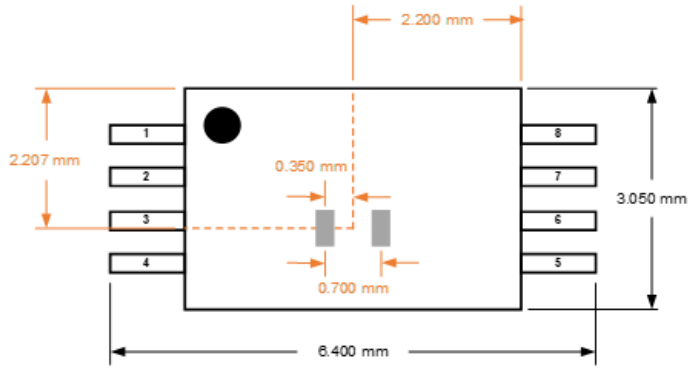

Figure 28: XtremeSense TMR Current Sensor Location in x-y Plane for CT453 in TSSOP-8 Package

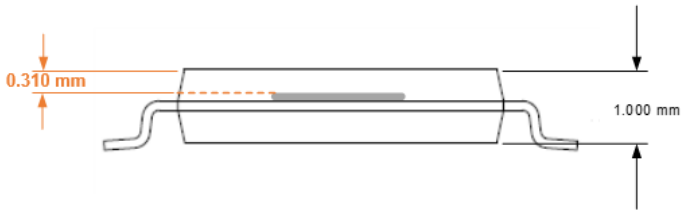

Figure 29: XtremeSense TMR Current Sensor Location in z Dimension for CT453 in TSSOP-8 Package

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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

Dimensions in millimeters – NOT TO SCALE

Dimensions exclusive of mold flash, gate burs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown

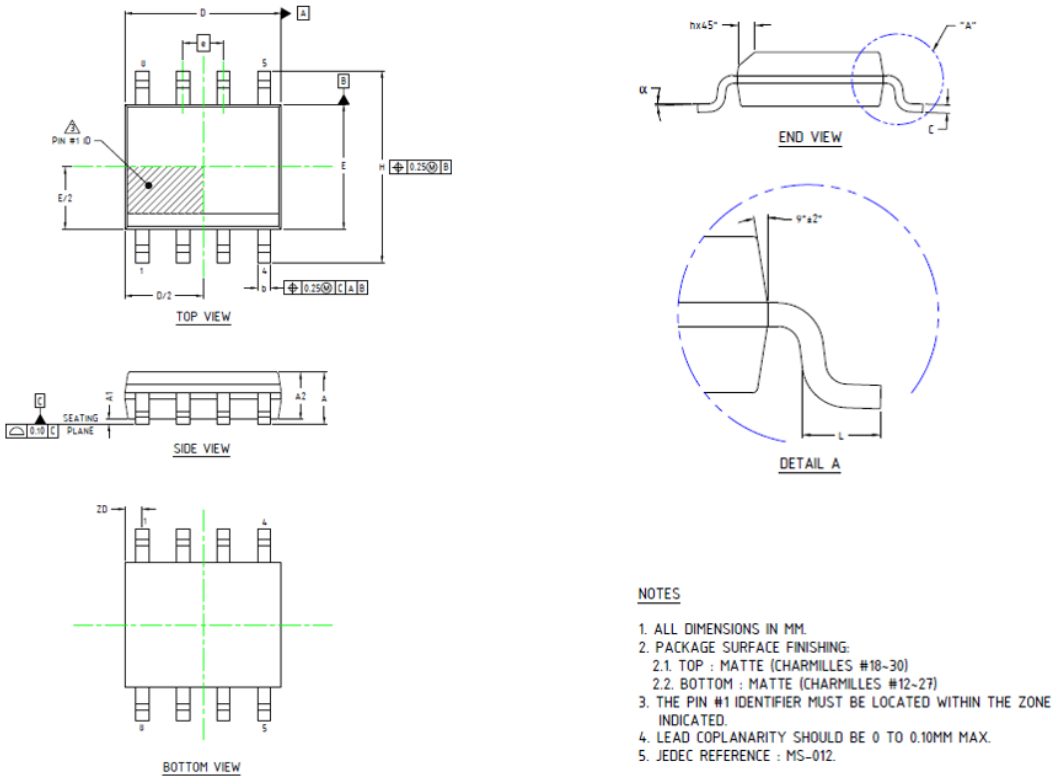

Figure 30: SOIC-8 Package Drawing and Dimensions

Table 3: CT453 SOIC-8 Package Dimensions

Symbol	Dimensions in Millimeters (mm)		
	Min.	Typ.	Max.
A1	0.10	0.18	0.25
b	0.36	0.41	0.46
C	0.19	0.22	0.25
D	4.80	4.89	4.98
E	3.81	3.90	3.99
e	1.27 BSC		
H	5.80	6.00	6.20
h	0.25	0.37	0.50
L	0.41	–	1.27
A	1.52	1.62	1.72
α	0°	–	8°
ZD	0.53 REF		
A2	1.37	1.47	1.57

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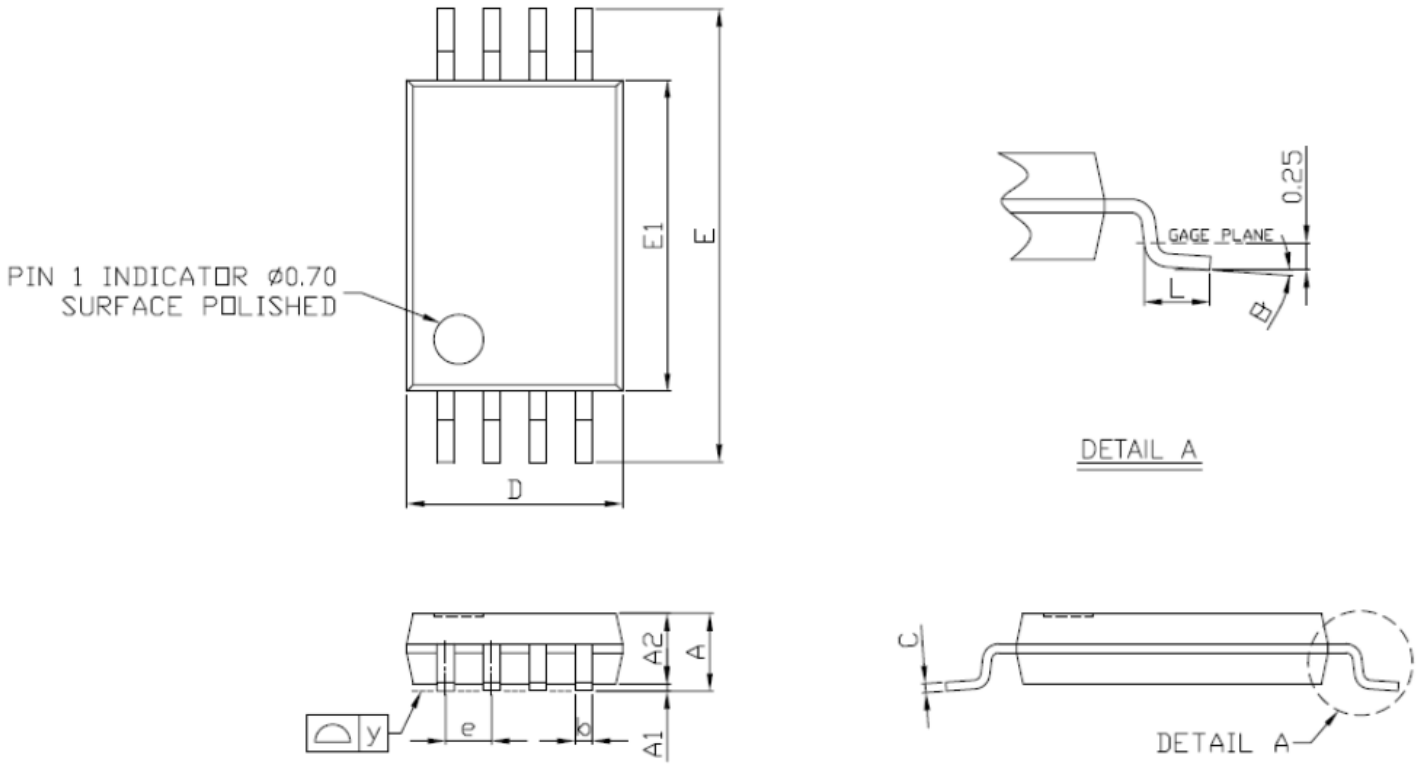

Figure 31: TSSOP-8 Package Drawing and Dimensions

Table 4: CT453 TSSOP-8 Package Dimensions

Symbol	Dimensions in Millimeters (mm)		
	Min.	Typ.	Max.
A	1.05	1.10	1.20
A1	0.05	0.10	0.15
A2	–	1.00	1.05
b	0.25	–	0.30
C	–	0.127	–
D	2.90	3.05	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	–	0.65	–
L	0.50	0.60	0.70
y	–	–	0.076
θ	0°	4°	8°

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TAPE AND REEL POCKET DRAWINGS AND DIMENSIONS

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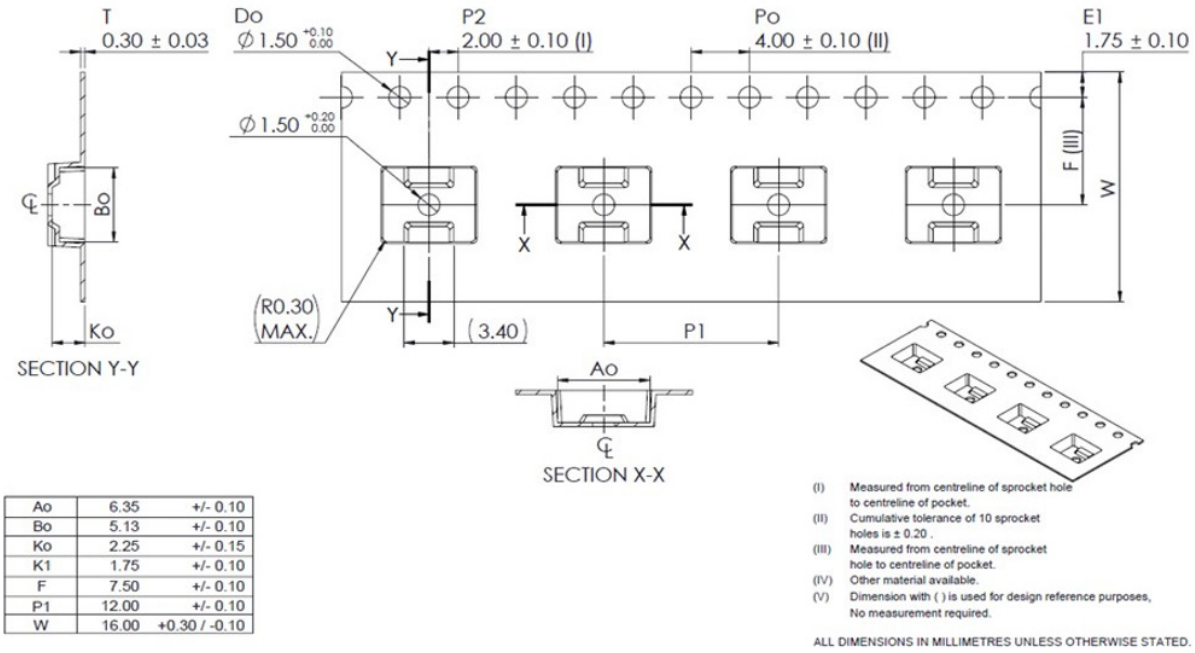
Dimensions in millimeters – NOT TO SCALE

Dimensions exclusive of mold flash, gate burs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown



Ao	6.35	+/- 0.10
Bo	5.13	+/- 0.10
Ko	2.25	+/- 0.15
K1	1.75	+/- 0.10
F	7.50	+/- 0.10
P1	12.00	+/- 0.10
W	16.00	+0.30 / -0.10

Figure 32: Tape and Pocket Drawing for SOIC-8 Package

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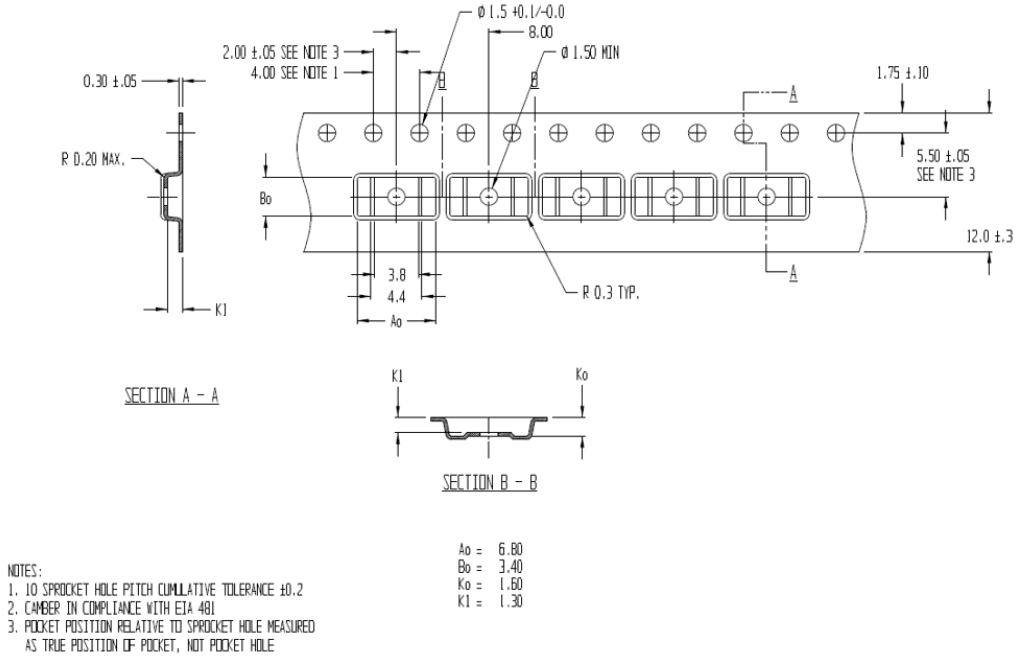

Figure 33: Tape and Pocket Drawing for TSSOP-8 Package

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PACKAGE INFORMATION

Table 5: CT453 Package Information

Part Number	Package Type	# of Leads	Package Quantity	Lead Finish	MSL Rating [2]	Operating Temperature (°C) [3]	Device Marking [4]
CT453-H06MRTS08	TSSOP	8	3000	Sn	1	–40 to 125	CT453-06MR YYWWLL
CT453-H06MRSN08	SOIC	8	2000	Sn	3	–40 to 125	CT453 06MR YYWWLL
CT453-H06DRTS08	TSSOP	8	3000	Sn	1	–40 to 125	CT453-06DR YYWWLL
CT453-H06DRSN08	SOIC	8	2000	Sn	3	–40 to 125	CT453 06DR YYWWLL
CT453-H00MRTS08	TSSOP	8	3000	Sn	1	–40 to 125	CT453-00MR YYWWLL
CT453-H00DRTS08	TSSOP	8	3000	Sn	1	–40 to 125	CT453-00DR YYWWLL
CT453-H00MRSN08	SOIC	8	2000	Sn	3	–40 to 125	CT453 00MR YYWWLL
CT453-H00DRSN08	SOIC	8	2000	Sn	3	–40 to 125	CT453 00DR YYWWLL

[1] RoHS is defined as semiconductor products that are compliant to the current EU RoHS requirements. It also will meet the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Green is defined as the content of chlorine (Cl), bromine (Br), and antimony trioxide based flame retardants satisfy JS709B low halogen requirements of ≤ 1,000 ppm.

[2] MSL Rating = Moisture Sensitivity Level Rating as defined by JEDEC standard classifications.

[3] Package will withstand ambient temperature range of –40°C to 125°C and storage temperature range of –65°C to 150°C.

[4] For the CT453, device marking for the SOIC-8 is defined as CT453 xxZR YYWWLL where the first 2 lines = part number, and third line is YY = year, WW = work week, and LL = lot code. Device marking for the TSSOP-8 is defined as CT450 xxZR YYWWLL where the first line = part number, and second line is YY = year, WW = work week, and LL = lot code.

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DEVICE MARKINGS

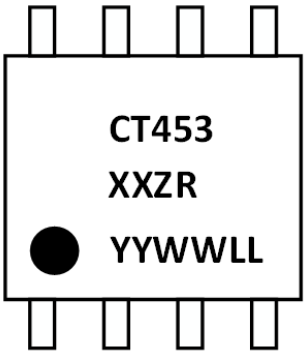

Figure 34: CT453 Device Marking for 8-Lead SOIC Package

Table 6: CT453 Device Marking Definition for 8-lead SOIC Package

Row No.	Code	Definition
3	•	Pin 1 Indicator
1	CT453	Allegro Part Number
2	XX	Maximum Field Rating
2	ZR	Polarity
3	YY	Calendar Year
3	WW	Work Week
3	LL	Lot Code

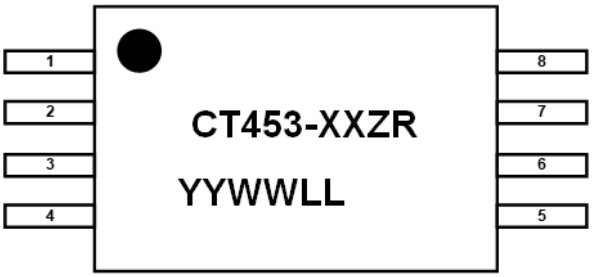

Figure 35: CT453 Device Marking for 8-Lead TSSOP Package

Table 7: CT453 Device Marking Definition for 8-lead TSSOP Package

Row No.	Code	Definition
1	•	Pin 1 Indicator
2	CT453	Allegro Part Number
2	XX	Maximum Magnetic Field Rating
2	ZR	Magnetic Field Range
3	YY	Calendar Year
3	WW	Work Week
3	LL	Lot Code

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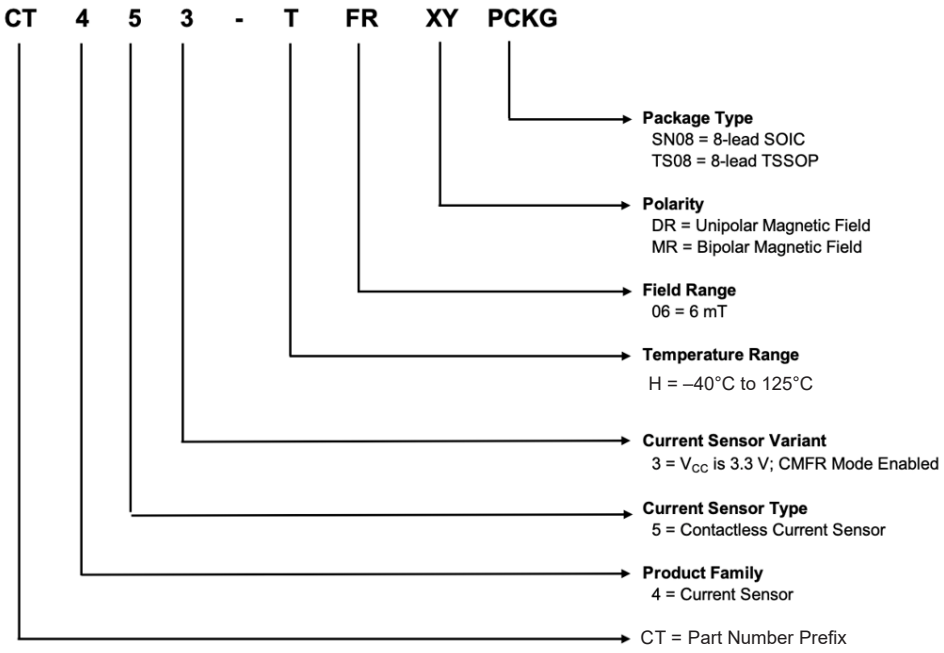
PART ORDERING NUMBER LEGEND



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Revision History

Number	Date	Description
1	November 2, 2023	Document rebranded and minor editorial updates
2	February 15, 2024	Removed AEC-Q100 (pages 1, 2, 21-23) and updated Selection Guide (page 2) and MSL levels (page 21)
3	February 29, 2024	Updated Offset Voltage (pages 9-12); removed Out Accuracy Performance and Lifetime Drift footnotes (pages 9-12); updated Sensitivity and removed Noise (pages 11-12); and updated branding information (page 22)
4	June 5, 2024	Added notes to package drawings (pages 18 and 20)

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