CTH5002NS-T52

N-Channel Enhancement MOSFET

Features

- Drain-Source Breakdown Voltage V_{DSS} 25V
- Drain-Source On-Resistance
  $R_{DS(ON)}$ 6.5mΩ, *at* V_{GS}*= 10V,* I_D*= 30A*
  $R_{DS(ON)}$ 10mΩ, *at* V_{GS}*= 4.5V,* I_D*= 30A*
- *Continuous D*rain Current at T_C=25°C I_D *=50A*
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

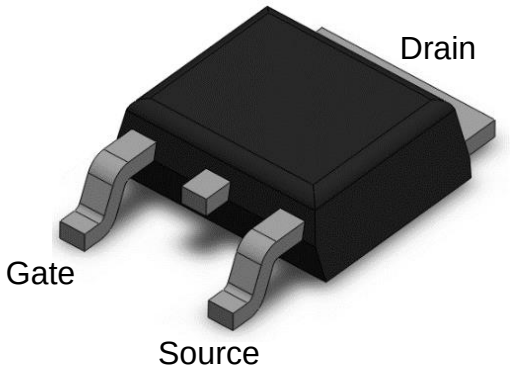
Description

The CTH5002NS-T52 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application.

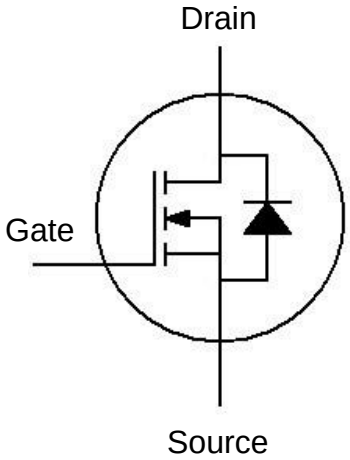
Applications

- DC/DC Converter
- Load Switch
- LCD Display inverter
- Power Management

Package Outline



Schematic



Absolute Maximum Rating at 25ºC

Symbol	Parameters	Test Conditions	Min	Note
V_{DS}	Drain-Source Voltage	25	V	
V_{GS}	Gate-Source Voltage	±20	V	
I_D	Continuous Drain Current @T_C=25˚C	50	A	1
I_{DM}	Pulsed Drain Current	100	A	1
P_D	Total Power Dissipation @T_C=25˚C	50	W	2
T_{STG}	Storage Temperature Range	-55 to 150	°C	
T_J	Operating Junction Temperature Range	-55 to 150	°C	

Thermal Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{\theta JC}$	Thermal Resistance Junction-Case		--	--	20	ºC /W	1,4

Electrical Characteristics T_A = 25°C (unless otherwise specified)

Static Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS}= 0V, I_D= 250μA	25	-	-	V	
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 20V, V_{GS} = 0V	-	-	1	μA	
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA	

On Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS} = 10V, I_D = 30A	-	6.5	8.5	mΩ	3
		V_{GS} = 4.5V, I_D = 30A		10	13	mΩ	3
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS} = V_{DS}, I_D =250μA	1.0	1.6	3.0	V	3

Dynamic Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
C_{ISS}	Input Capacitance	V_{GS} =0V,	-	1100	1300	pF	
C_{OSS}	Output Capacitance	V_{DS} =15V	-	240	-		
C_{RSS}	Reverse Transfer Capacitance	f=1MHz	-	190	-		

Switching Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$T_{D(ON)}$	Turn-On Delay Time	V_{DS} = 15V ,	-	13	17	ns	
T_R	Rise Time	V_{GS} = 10V,	-	10	13		
$T_{D(OFF)}$	Turn-Off Delay Time	R_G = 24Ω,	-	46	58		
T_F	Fall Time	R_L = 15Ω,	-	7	10		
Q_G	Total Gate Charge	V_{DS} = 15V ,	-	22	25	nC	
Q_{GS}	Gate-Source Charge	V_{GS} = 10V,	-	4.5	-		
Q_{GD}	Gate-Drain (Miller) Charge	I_D =35A	-	4	-		

Drain-Source Diode Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
V_{SD}	Body Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 20A	-	0.87	1.5	V	1
I_{SD}	Body Diode Continuous Current		-	-	20	A	1

Note:

1. The power dissipation is limited by 150°C junction temperature.
2. The data tested by pulsed , pulse width ≦ 300μs , duty cycle ≦ 2%
3. Thermal Resistance follow JESD51-3.

Typical Characteristic Curves

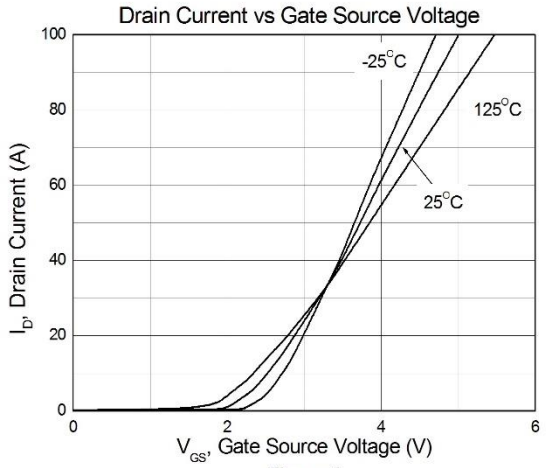


Figure 1

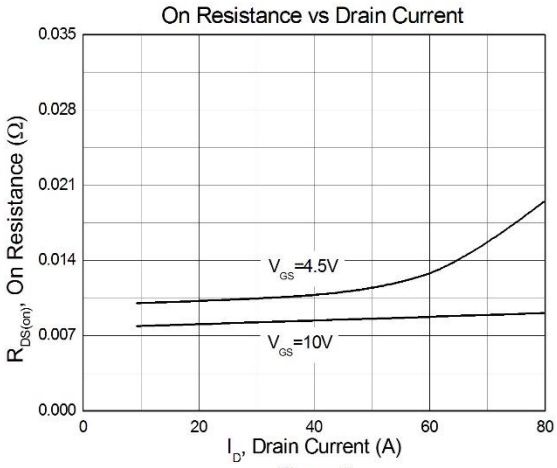


Figure 2

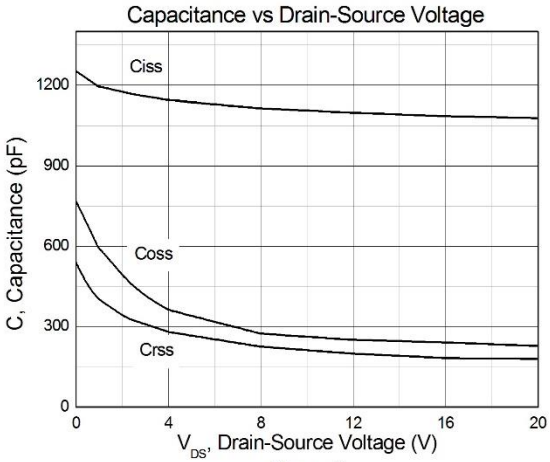


Figure 3

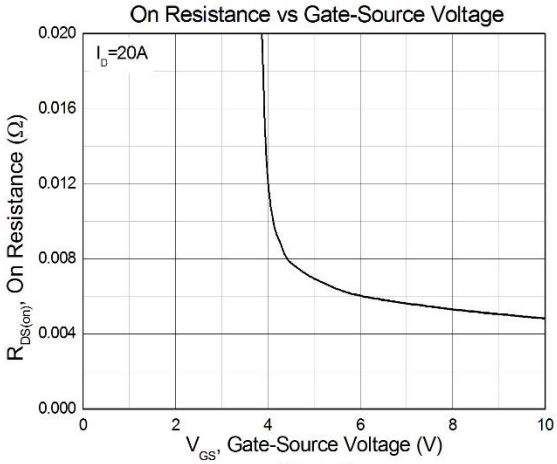


Figure 4

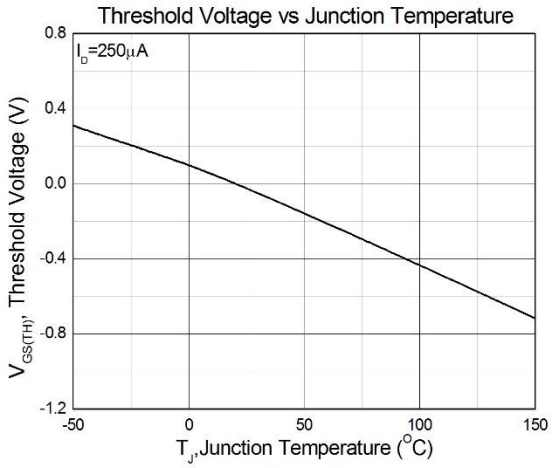


Figure 5

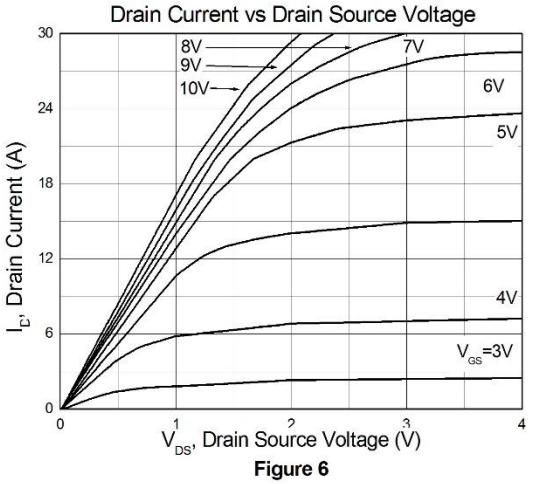


Figure 6

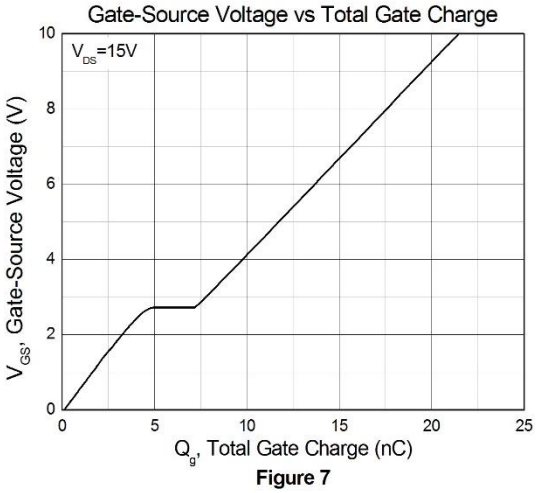


Figure 7

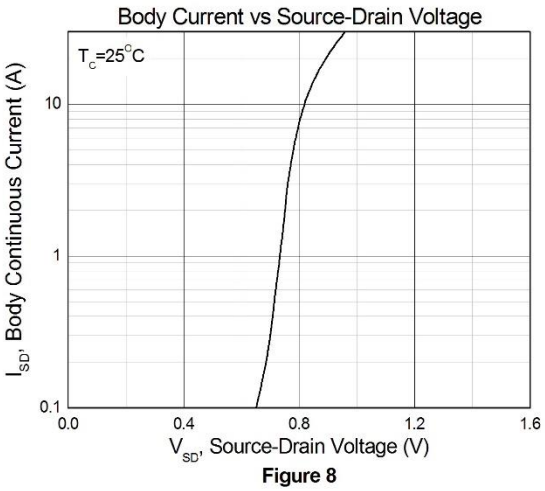


Figure 8

Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

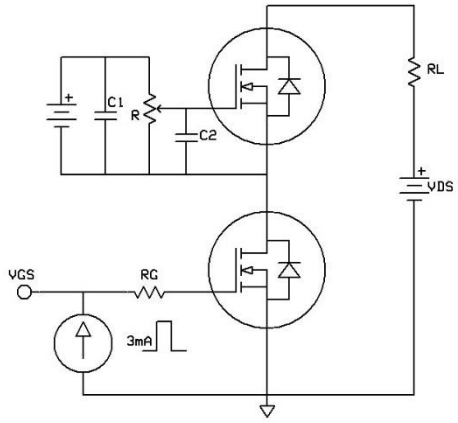


Figure 10: Gate Charge Waveform

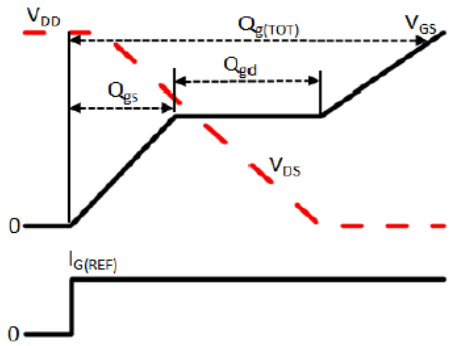


Figure 11: Switching Time Test Circuit

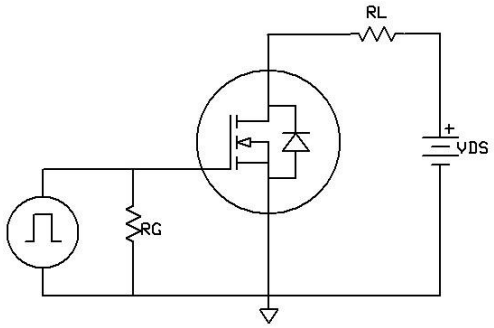
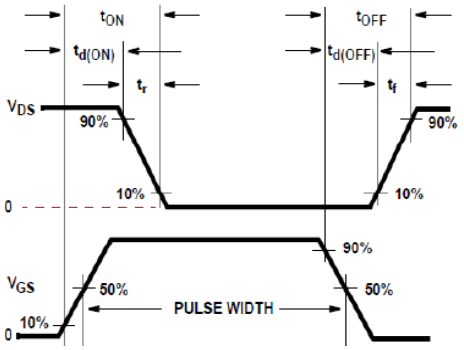
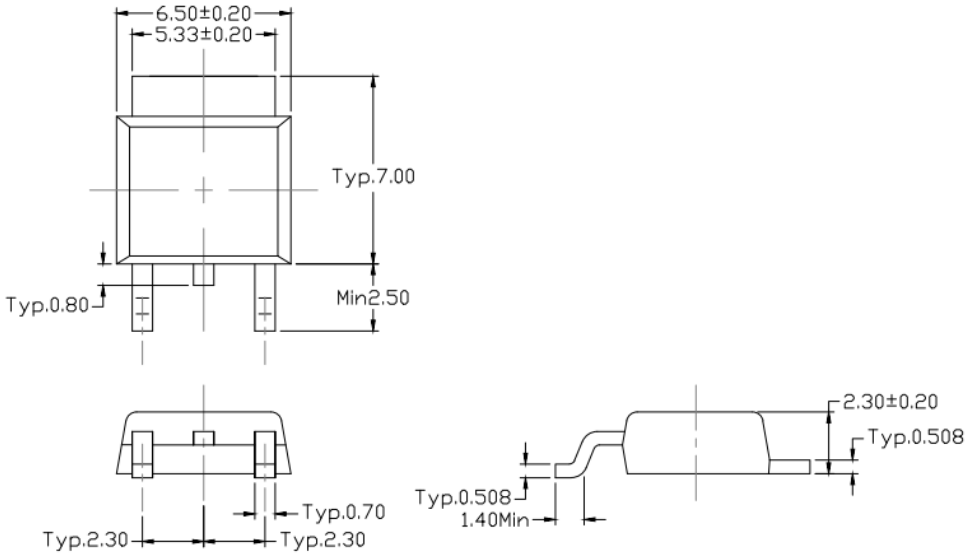


Figure 12: Switching Time Waveform

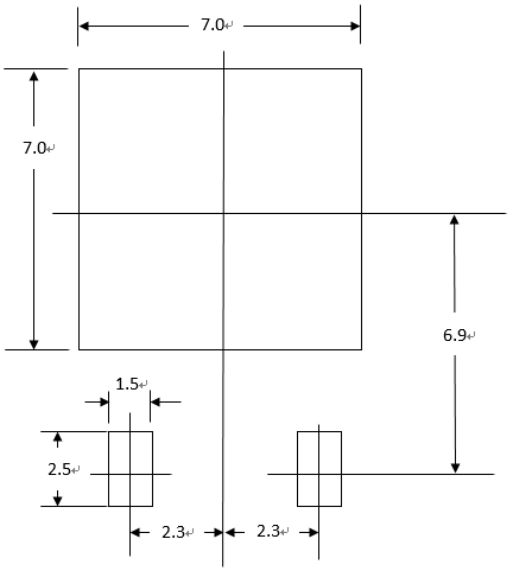


Package Dimension (TO-252)



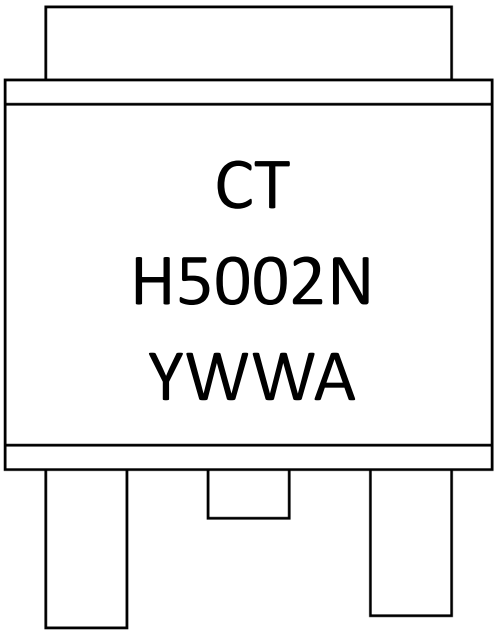
Dimensions in mm unless otherwise stated

Recommended pad layout for surface mount leadform



Dimensions in mm unless otherwise stated

Marking Information

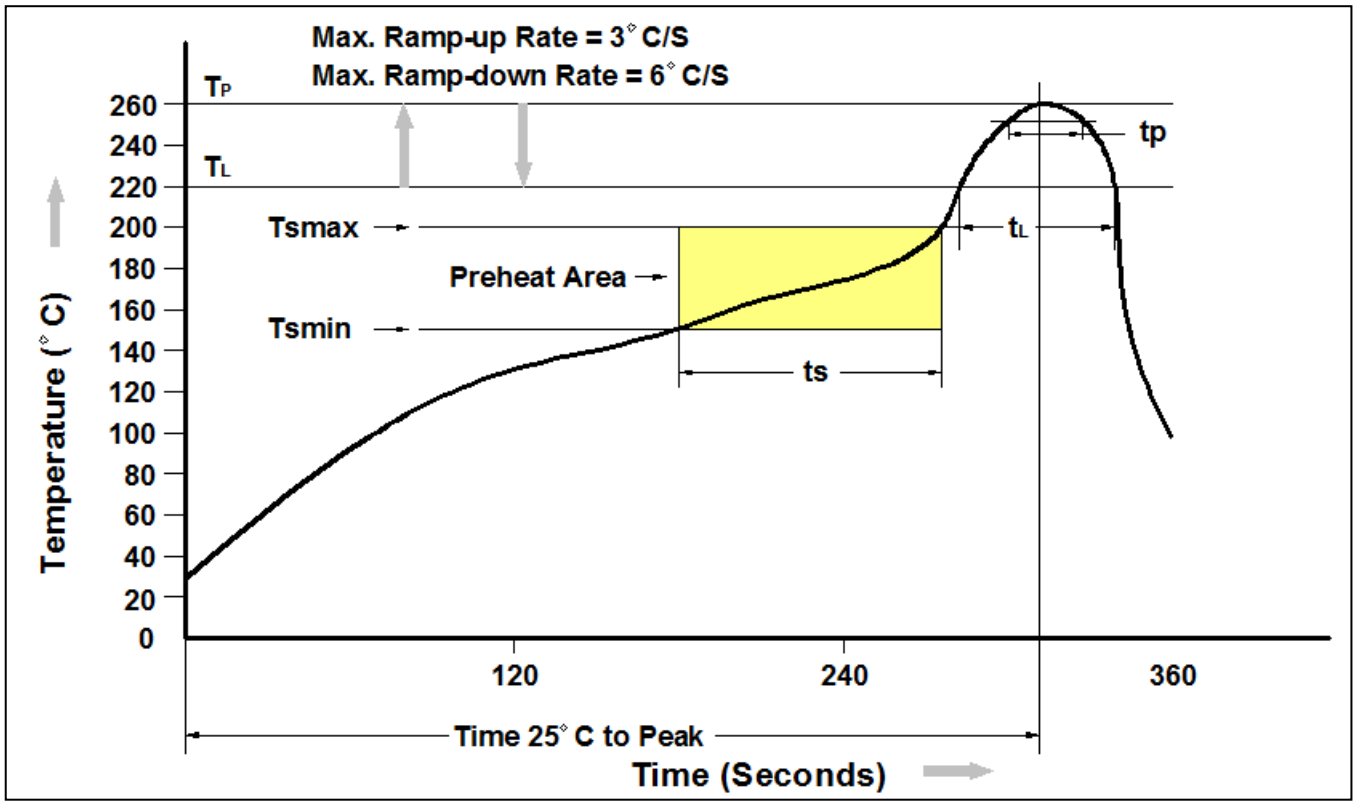


CT	: Denotes " CT Micro"
H5002N	: Device Number
Y	: Fiscal Year
WW	: Work Week
A	: Production Code

Ordering Information

Part Number	*Description*	*Quantity*
CTH5002NS-T52	TO-252 Reel	2500 pcs

Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (ts) from (Tsmin to Tsmax)	60-120 seconds
Ramp-up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 – 150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second max
Time 25°C to Peak Temperature	8 minutes max.

DISCLAIMER

CT MICRO RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. CT MICRO DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

CT MICRO ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT EXPRESS WRITTEN APPROVAL OF CT MICRO INTERNATIONAL CORPORATION.

1. *Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instruction for use provided in the labelling, can be reasonably expected to result in significant injury to the user.*
2. *A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.*