2-Wire Serial EEPROMs 1K/2K/4K/8K/16K

CTK24BC01-16Q8

Description

The CTK24BC family provides 1K, 2K, 4K, 8K and 16K of serial electrically erasable and programmable read-only memory (EEPROM). The wide Vdd range allows for low-voltage operation down to 1.8V. The device, fabricated using traditional CMOS EEPROM technology, is optimized for many industrial and commercial applications where low-voltage and low-power operation is essential. The device is accessed via a 2-wire serial interface.

Features

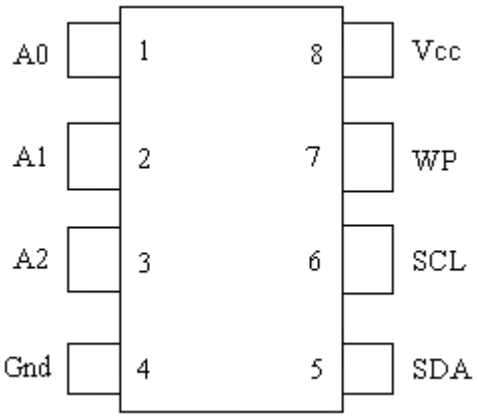
- Internally organized as 128×8(1K), 256×8(2K) 512×8(4K), 1024×8(8K), 2048×8(16K)
- Low-voltage and standard-voltage operation : 1.8~5.5V
- 2-wire serial interface bus
- Date retention : 100 years
- High endurance : 1,000,000 write cycles
- 100kHz(1.8V)& 400kHz(5V) compatibility
- Bi-directional data transfer protocol
- Self-timed write cycle (5ms max)
- Write protect pin for hardware data protection
- 8-byte page (1K, 2K) and 16-byte page (4K, 8K, 16K) write modes
- Allows for partial page write

Absolute Maximum Ratings

Parameter	Ratings	Unit
Voltage on any pin with respect to ground	-0.8 to V_{CC}+1.5	V
Maximum operating voltage	6.25	V
DC output current	5.0	mA
Operating temperature range	-55 ~ +125	℃
Storage temperature range	-65 ~ +150	℃

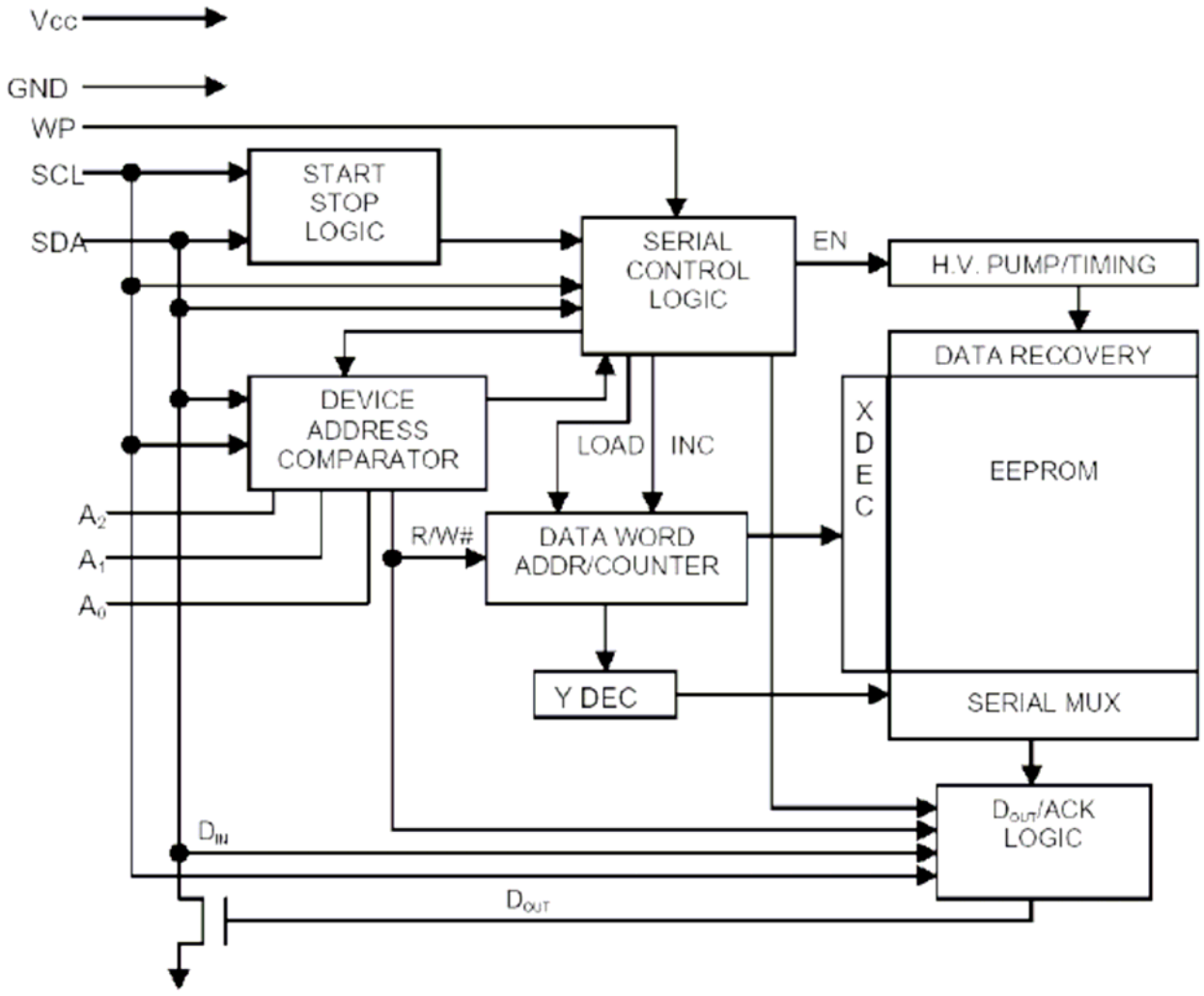
Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of these specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configurations



Pin Name	Function
A0-A2	Address inputs
SDA	Serial data
SCL	Serial clock input
WP	Write protect
Gnd	Ground
Vcc	Power supply

Block Diagram



Pin Descriptions

Serial Data(SDA): The SDA pin used for sending and receiving data bits in serial mode. Since the SDA pin is defined as an open-drain connection, a pull-up resistor is needed.

Serial Clock(SCL): The SCL input is used to synchronize data input and output with clocked out on the falling edge of SCL.

Device/Page Addresses(A_2, A_1, A_0): The A_2, A_1, and A_0 pins are used to address multiple devices on a single bus system and should be hard-wired.

- The CTK24BC01 and CTK24BC02 use the A_2, A_1 and A_0 pins to provide the capability for addressing up to eight 1K/2K devices on a single bus system (please see the Device Addressing section for further details)
- The CTK24BC04 uses the A_2 and A_1 inputs and a total of for 4K device may be addressed on a single bus system. The A_0 pin is not used, but should be grounded if possible.
- The CTK24BC08 only uses the A_2 input hardware addressing. On a single bus system, a total of two 8K devices may be addressed. The A_0 and A_1 pins are not used, but should be grounded if possible.
- The CTK24BC16 does not use the device address pins, so only one device can be connected to a single bus system. Therefore, the A_0, A_1, and A_2 pins are not used, but should be grounded if possible.

Write Protect (WP): The CTK24BC01/02/04/08/16 has a Write Protect pin that provides hardware data protection. When connected to ground, the Write Protect pin allows for normal read/write operations. If the WP pin is connected to V_{CC}, no data can be overwritten.

Memory Organization

The internal memory organization for the CTK24BC family is arranged differently for each of the densities. The CTK24BC01, for instance, is internally organized as 16 pages of 8 bytes each and requires a 7-bit data word address. The CTK24BC16, on the other hand, is organized as 128 pages of 16 bytes each with an 11-bit data word address. The table below summarizes these differences.

Density	# of pages	Bytes per page	Data word address length
CTK24BC01 (1K)	16 pages	8 bytes	7 bits
CTK24BC02 (2K)	32 pages	8 bytes	8 bits
CTK24BC04 (4K)	32 pages	16 bytes	9 bits
CTK24BC08 (8K)	64 pages	16 bytes	10 bits
CTK24BC16 (16K)	128 pages	16 bytes	11 bits

Pin Capacitance

Applicable over recommended operating range :T_A=25℃, f=1MHz, V_{CC}=+1.8V

Symbol	Test Condition	Max	Unit	Condition
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$=0V
C_{IN}	Input Capacitance (A_0, A_1,A_2, SCL)	6	pF	V_{IN}=0V

Note : These parameters are characterized and not 100% tested.

DC Characteristics

Applicable over recommended operating range: T_A=-40~+85℃, V_{CC}=+1.8V~+5.0V(unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC} 1		1.8	-	5.5	V
Supply Voltage	V_{CC} 2		2.7	-	5.5	V
Supply Voltage	V_{CC} 3		4.5	-	5.5	V
Supply Current V_{CC}=5.0V	I_{CC}	READ at 100KHz	-	0.4	1.0	mA
Supply Current V_{CC}=5.0V	I_{CC}	WRITE at 100KHz	-	2.0	3.0	mA
Standby Current V_{CC}=1.8V	I_{SB} 1	V_{IN}=V_{CC} or V_{SS}	-	0.6	3.0	μA
Standby Current V_{CC}=2.5V	I_{SB} 2	V_{IN}=V_{CC} or V_{SS}	-	1.4	4.0	μA
Standby Current V_{CC}=5.5V	I_{SB} 3	V_{IN}=V_{CC} or V_{SS}	-	5.0	18	μA
Input Leakage Current	I_{LI}	V_{IN}=V_{CC} or V_{SS}	-	0.2	5.0	μA
Output Leakage Current	I_{LO}	V_{OUT}=V_{CC} or V_{SS}	-	0.1	5.0	μA
Input Low Level (Note 1)	V_{IL}		-0.6	-	V_{CC}×0.3	V
Input High Level (Note 1)	V_{IH}		V_{CC}×0.7	-	V_{CC}+0.5	V
Output Low Level V_{CC}=3.0V	V_{OL} 2	I_{OL} =2.1mA	-	-	0.4	V
Output Low Level V_{CC}=3.0V	V_{OL} 1	I_{OL} =0.15mA	-	-	0.2	V

Note : V_{IL} and V_{IH} Max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range: TA=-40~+85℃, VCC=+1.8V~+5.0V, CL=1 TTL Gate & 100pF(unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency, SCL	f_{SCL}	V_{CC}=1.8V V_{CC}=2.7~5.5V	- -	-	100 400	KHz
Clock Pulse Width Low	t_{LOW}	V_{CC}=1.8V V_{CC}=2.7~5.5V	4.7 1.2	-	-	μs
Clock Pulse Width High	t_{HIGH}	V_{CC}=1.8V V_{CC}=2.7~5.5V	4.0 0.6	-	-	μs
Noise Suppression Time (Note 1)	t_I	V_{CC}=1.8V V_{CC}=2.7~5.5V	- -	-	100 50	ns
Clock Low to Data Out Valid	t_{AA}	V_{CC}=1.8V V_{CC}=2.7~5.5V	0.1 0.1	-	4.5 0.9	μs
Time the bus must be free before A new transmission can start (Note 1)	t_{BUF}	V_{CC}=1.8V V_{CC}=2.7~5.5V	4.7 1.2	-	-	μs
Start Hold Time	$t_{HD.STA}$	V_{CC}=1.8V V_{CC}=2.7~5.5V	4.0 0.6	-	-	μs
Start Setup Time	$t_{SU.STA}$	V_{CC}=1.8V V_{CC}=2.7~5.5V	4.7 0.6	-	-	μs
Data in Hold Time	$t_{HD.DAT}$	V_{CC}=1.8V V_{CC}=2.7~5.5V	0 0	-	-	μs
Data in Setup Time	$t_{SU.DAT}$	V_{CC}=1.8V V_{CC}=2.7~5.5V	200 100	-	-	ns
Input Rise Time (Note 1)	t_R	V_{CC}=1.8V V_{CC}=2.7~5.5V	- -	-	1.0 0.3	μs
Input Fall Time (Note 1)	t_F	V_{CC}=1.8V V_{CC}=2.7~5.5V	- -	-	300 300	ns

AC Characteristics(Cont.)

Applicable over recommended operating range: T_A=-40~+85℃, V_{CC}=+1.8V~+5.0V, C_L=1TTL Gate & 100pF(unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Stop Setup Time	$t_{SU.STO}$	V_{CC}=1.8V V_{CC}=2.7~5.5V	4.7 0.6	-	-	μs
Data out Hold Time	t_{DH}	V_{CC}=1.8V V_{CC}=2.7~5.5V	100 50	-	-	ns
Write Cycle Time	t_{WR}	V_{CC}=1.8V V_{CC}=2.7~5.5V	-	-	5 5	ms
5.0V, 25℃, Byte Mode	Endurance (Note 1)	V_{CC}=1.8V V_{CC}=2.7~5.5V	1M 1M	-	-	Write Cycles

Note: 1. This parameter is characterized and not 100% tested.

Device Operation

Clock and Data Transitions: Transitions on the SDA pin should only occur when SCL is low(refer to the Data Validity timing diagram in Figure 3). If the SDA pin changes when SCL is high, then the transition will be interpreted as a START or STOP condition.

START Condition: A START condition occurs when the SDA transitions from high to low when SCL is high. The START signal is usually used to initiate a command(refer to the START and STOP definition timing diagram in Fig 4)

STOP Condition: A STOP condition occurs when the SDA transitions from low to high when SCL is high. (refer to the START and STOP definition timing diagram in Fig 4) The STOP command will put the device into standby mode after no acknowledgement is issued during the read sequence.

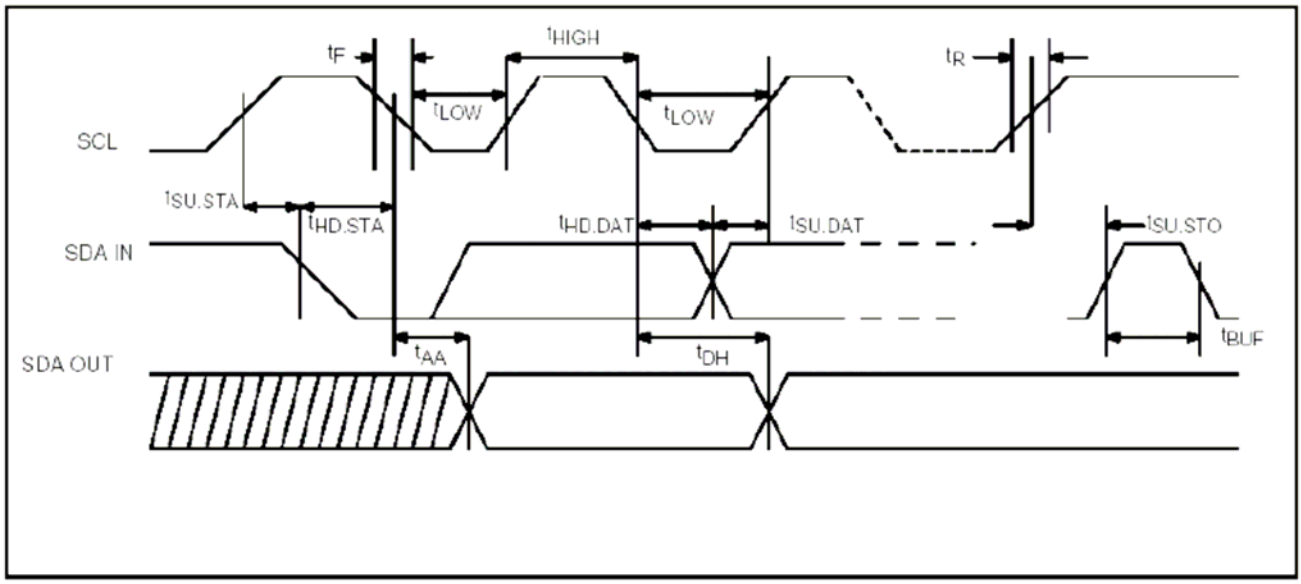
Acknowledge: An acknowledgement is sent by pulling the SDA low to confirm that a word has been successfully received. All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words, so acknowledgements are usually issued during the 9^{th} clock cycle.

Standby Mode: Standby mode is entered when the chip is initially powered-on or after a STOP command has been issued and any internal operations have been completed.

Memory Reset: In the event of unexpected power or connection loss, a START condition can be issued to restart the input command sequence. If the device is currently in write cycle mode, this command will be ignored.

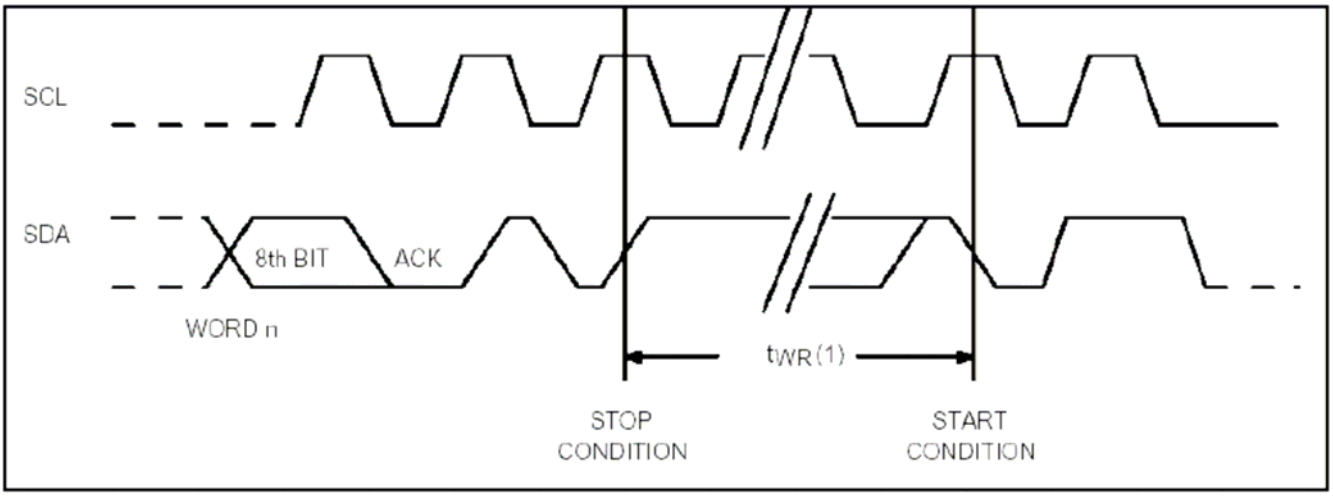
Bus Timing

Figure 1. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 2. SCL: Serial Clock, SDA: Serial Data I/O



Note : 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 3. Data Validity

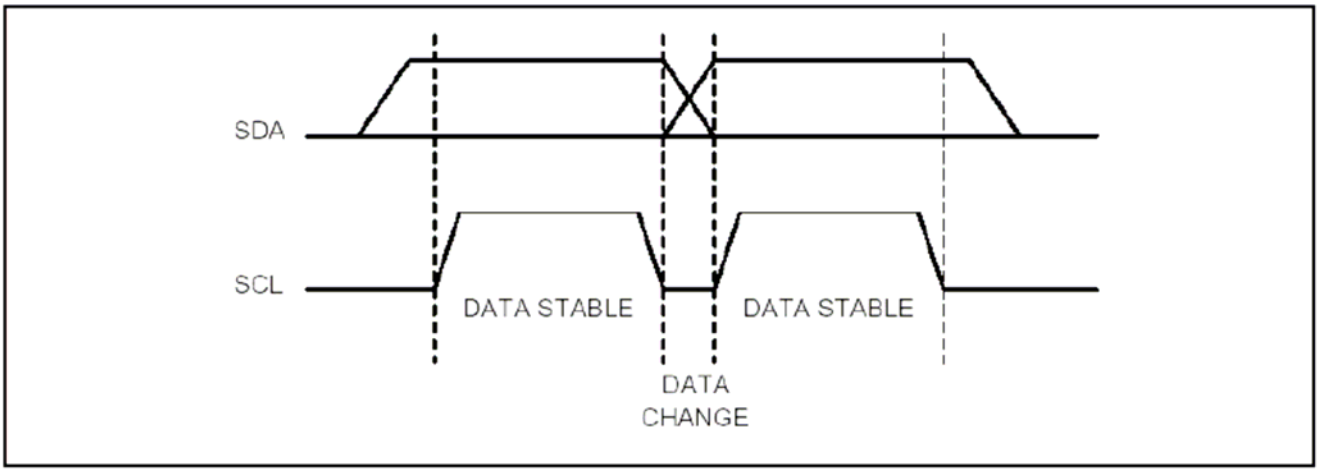


Figure 4. START and STOP Definition

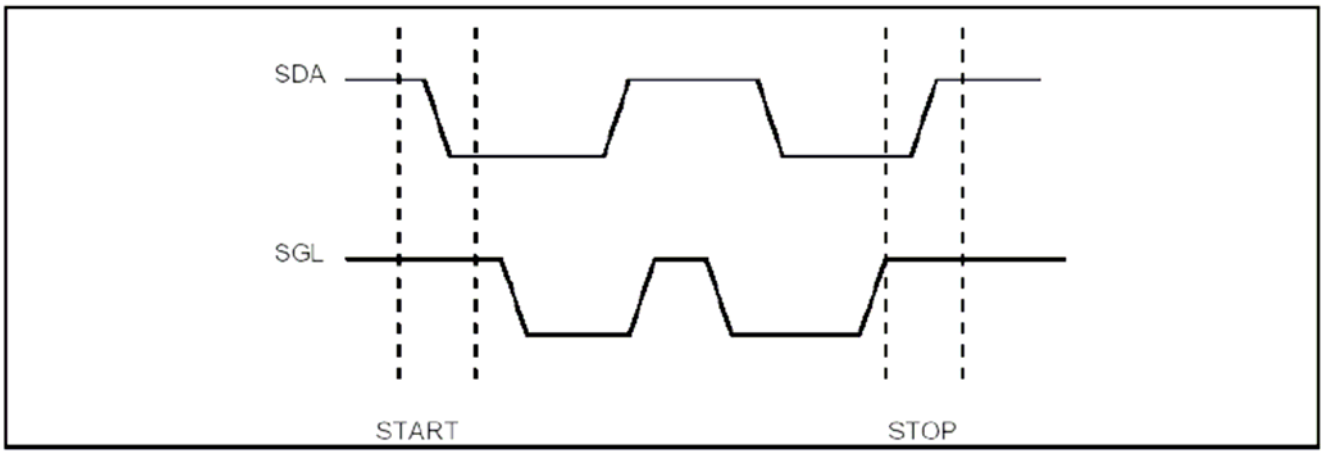
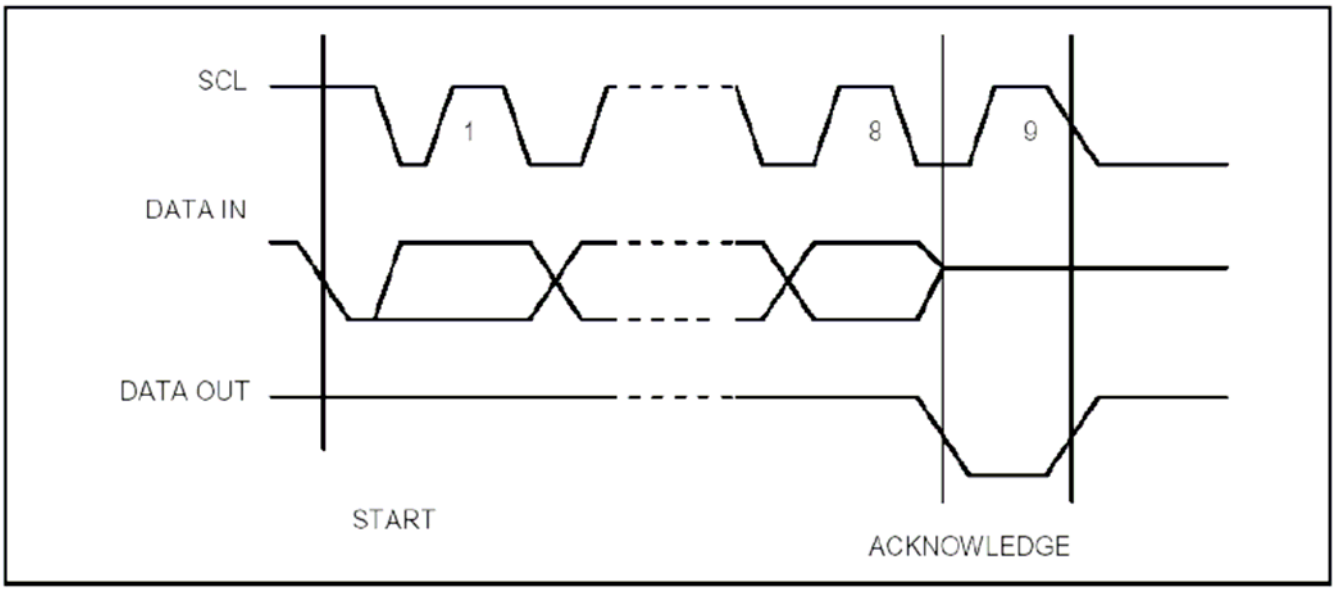


Figure 5. OUTPUT Acknowledge



Device Addressing

To enable the chip for a read or write operation, an 8-bit device address word followed by a START condition must be issued. The 1st four bits of the device address word consist of a mandatory '1010' pattern, while the 2nd four bits depend on the particular density being used(refer to Figure 6):

- In the 1K/2K chip, the next 3 bits should correspond to the hard-wired input A_2, A_1, and A_0 device address bits.
- In the 4K chip, the next 3 bits are the A_2 and A_1 device address bits and a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins.
- In the 8K chip, the next 3 bits include the A_2 device address bit with the next 2 bits used for memory page addressing. The A_2 bit must compare to its corresponding hard-wired input pin.
- The 16K chip does not use any device address bits but instead the 3 bits are used for memory page addressing.

Figure 6. Device address

	MSB							LSB
1K/2K	1	0	1	0	A_2	A_1	A_0	R/W
4K	1	0	1	0	A_2	A_1	P0	R/W
8K	1	0	1	0	A_2	P1	P0	R/W
16K	1	0	1	0	P2	P1	P0	R/W

The memory page address bits , P_2, P_1, and P_0 are used to select the page in the array. P_2 represents the most significant bit, while P_1 and P_0 are considered the next most significant bits.

The eight bit of the device address determines read or write operation. If the R/W bit is high, then a read operation is initiated. Otherwise, if the R/W bit is low, then a write operation is started.

After comparing the device address and finding a match, the EEPROM device will issue an acknowledgement by pulling SDA low. If the comparison fails, the chip will return to standby mode.

Figure 7. Byte Write

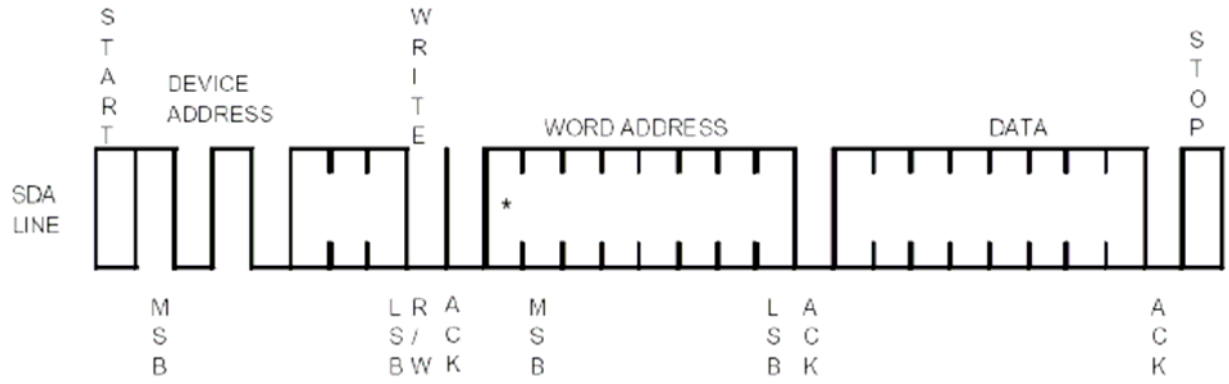
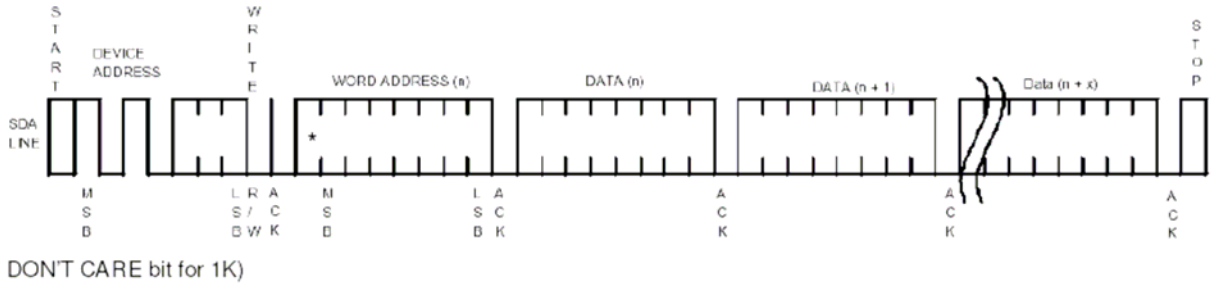


Figure 8. Page Write



(* = DON'T CARE bit for 1K)

Write Operation

Byte/Page Write:

If a write operation is entered (R/W=0) and an acknowledgement is sent, then the next sequence requires an 8-bit data word address. After an acknowledgement is received from this word address, the 1st byte of data can be loaded. The device will send an acknowledgement after each byte to confirm the transmission.

To being the write cycle, a STOP condition must be issued (refer to Figure 7). Both byte and page write operations are supported, so the STOP condition can be issued after the 1st byte or the last byte in the page. When the STOP condition occurs, an internal time is started, all inputs are disabled, and the EEPROM will not respond to any more commands until the write cycle is completed.

Note: The number of bytes in a page depends on the density used. If 1K density is used, then the page size is 8 bytes. In contrast, if the 16K density is used, then the page size is 16 bytes. Refer to the Memory Organization section for more details.

The internal page counter is incremented after each byte received, but the row location of the memory page will always remain the same. Therefore the device will wrap around to the 1st byte in the page after the last byte in the page is received. Any further data loaded into the page buffer will overwrite the previous data loaded.

Acknowledge Polling:

After the STOP condition is issued, the write cycle begins. Acknowledge polling can be initiated by sending a START condition followed by the device address word. If the EEPROM has completed the internal write cycle and returned to standby mode, the device will respond by sending back an acknowledgement by pulling the SDA pin low. Otherwise, the sequence will be ignored and no acknowledgement will be sent.

Read Operations

There are three types of read operations: current address read, random address read, and sequence read. A random address read can be considered a current address read operation with an additional sequence in the beginning to load a different address into the internal counter. A sequential read occurs when subsequent bytes are clocked out after a current address read or random address read occurs.

Current Address Read : A current address read operation is initiated by issuing R/W=1 in the device address word(refer to Figure 9). Since the internal address counter maintains the last address incremented by one accessed during the last read or write operation, the internal address counter will always retain the last address incremented by one.

Random Read : To access a different address location that the one currently stored in the internal counter, a random read operation is provided. The random read is actually a combination of a "dummy" byte write sequence with a current address read command (refer to Figure 10). The "dummy" byte write loads a different address into the internal counter, and the data can then be accessed using the current address read.

Sequential Read : In order to access subsequent data word after a current address read or random read has been initiated, the user should send an acknowledgement to the EEPROM chip after each data byte received. If an acknowledgement is not received, then the chip will not send any more data and expect a STOP condition on the next cycle to reset back to standby mode(refer to Figure 11).

Sequential reads can be used to perform an entire chip read. Unlike the page write operation, the internal counter will increment to the next row after the last byte of the page has been reached. When the address reaches the last byte of the last memory page, the next address will increment to the 1st byte of the 1st memory page.

Once the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. When the microcontroller does not respond with a zero but does generate a following stop condition, the sequential read operation is terminated.

Figure 9. Current Address Read

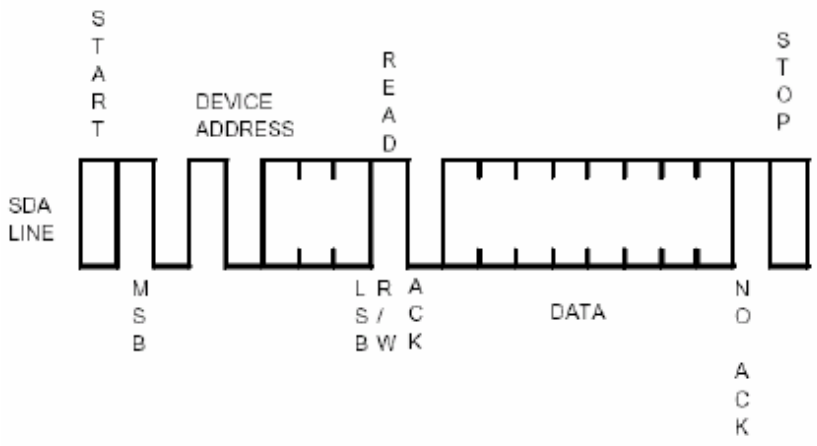
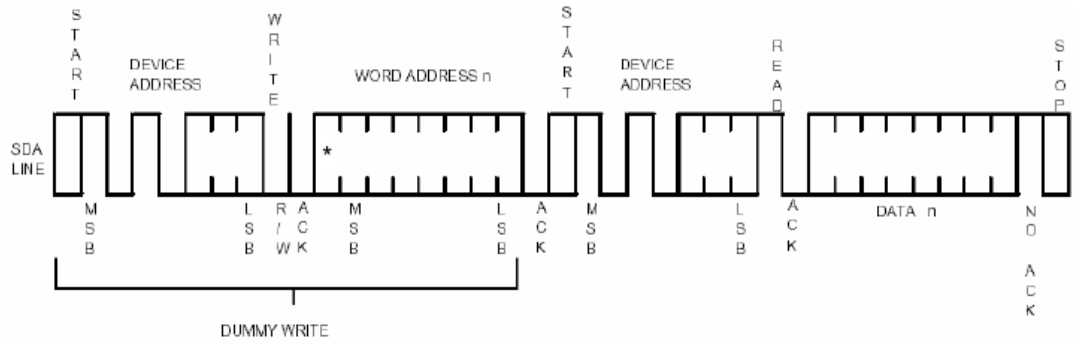
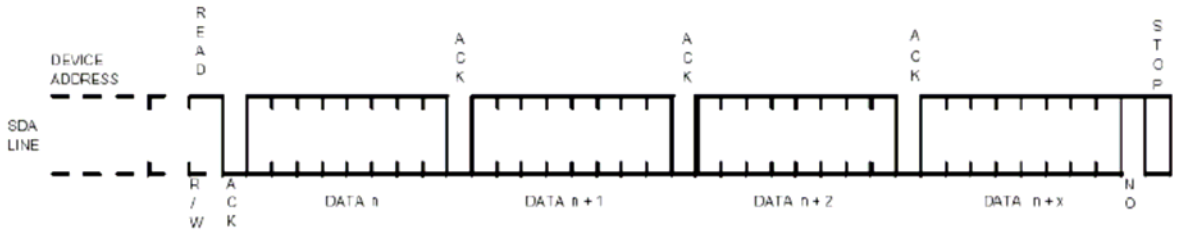


Figure 10. Random Read



(* = DON'T CARE bit for 1K)

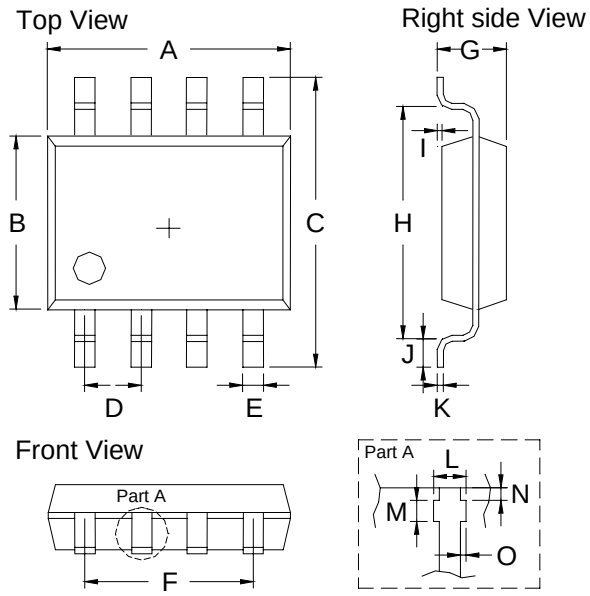
Figure 11. Sequential Read

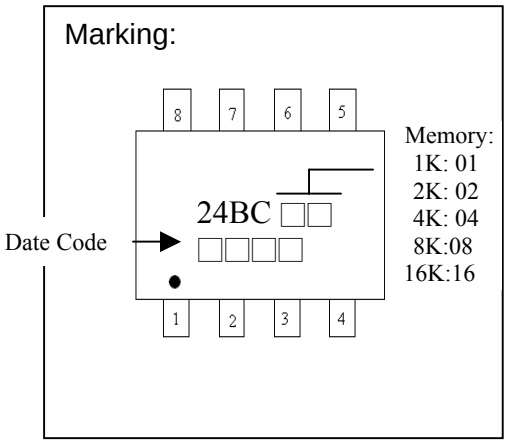


Ordering Information

Ordering Code	Package	Device Function	Operating Ranges
CTK24BC01Q8	SOP-8	1K bit(128x8)	Industrial (-40~+85℃)
CTK24BC02Q8		2K bit(256x8)	
CTK24BC04Q8		4K bit(512x8)	
CTK24BC08Q8		8K bit(1024x8)	
CTK24BC16Q8		16K bit(2048x8)	

SOP-8 Dimension





8-Lead SO-8 Plastic Package
CYStek Package Code: Q8

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1909	0.2007	4.85	5.10	I	0.0019	0.0078	0.05	0.20
B	0.1515	0.1555	3.85	3.95	J	0.0118	0.0275	0.30	0.70
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0098	0.19	0.25
D	0.0480	0.0519	1.22	1.32	L	0.0145	0.0204	0.37	0.52
E	0.0145	0.0185	0.37	0.47	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0570	0.0649	1.45	1.65	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0