CTL0196PS-R3

P-Channel Enhancement MOSFET

Features

- Drain-Source Breakdown Voltage V_{DSS} -60 V
- Drain-Source On-Resistance
  $R_{DS(ON)}$ 170mΩ, at V_{GS}= -10V, I_D= -1.8A
  $R_{DS(ON)}$ 200mΩ, at V_{GS}= -4.5V, I_D= -1.4A
- Continuous Drain Current at T_C=25°C I_D = -1.9A
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

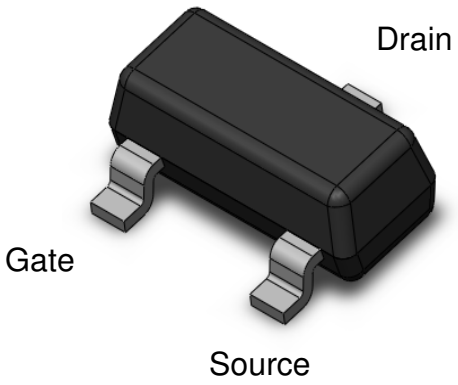
Description

The CTL0196PS-R3 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

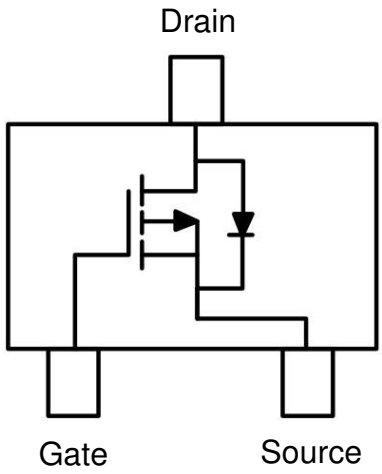
Applications

- Power Management
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

Package Outline



Schematic



Absolute Maximum Rating at 25°C

Symbol	Parameters	Test Conditions	Min	Notes
V_{DS}	Drain-Source Voltage	-60	V	
V_{GS}	Gate-Source Voltage	±20	V	
I_D	Continuous Drain Current	-1.9	A	1
I_{DM}	Pulsed Drain Current	-7.6	A	1
P_D	Total Power Dissipation	1.4	W	2
T_{STG}	Storage Temperature Range	-55 to 150	℃	
T_J	Operating Junction Temperature Range	-55 to 150	℃	

Thermal Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{\Theta JA4}$	Thermal Resistance Junction-Ambient (t=10s)		--	90	--	°C /W	1,4

Electrical Characteristics T_A = 25℃ (unless otherwise specified)

Static Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS}= 0V, I_D= -250μA	-60	-	-	V	
I_{DSS}	Drain-Source Leakage Current	V_{DS} = -60V, V_{GS} = 0V	-	-	-1	μA	
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA	

On Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS} = -4.5V, I_D = -1.4A	-	170	215	mΩ	3
		V_{GS} = -10V, I_D = -1.8A	-	200	260	mΩ	
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS} = V_{DS}, I I_D =-250μA	-1	---	-3	V	3

Dynamic Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
C_{ISS}	Input Capacitance	V_{GS} =0V,	-	365	-	pF	
C_{OSS}	Output Capacitance	V_{DS} =-25V	-	40	-		
C_{RSS}	Reverse Transfer Capacitance	f=1MHz	-	12	-		

Switching Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$T_{D(ON)}$	Turn-On Delay Time	V_{DS} = -30V ,	-	20	-	ns	
T_R	Rise Time	V_{GS} = -10V,	-	33	-		
$T_{D(OFF)}$	Turn-Off Delay Time	R_G = 3.3Ω,	-	5.2	-		
T_F	Fall Time	R_L= 30Ω,	-	3.8	-		
Q_G	Total Gate Charge	V_{DS} = -48V ,	-	6.3	-	nC	
Q_{GS}	Gate-Source Charge	V_{GS} = -4.5V,	-	2.3	-		
Q_{GD}	Gate-Drain Charge	I_D = -1A	-	1.8	-		

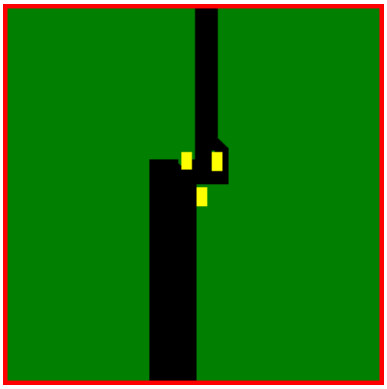
Drain-Source Diode Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
V_{SD}	Body Diode Forward Voltage	V_{GS} = 0V, I_D = -1.9A	-	-	-1.2	V	
I_{SD}	Body Diode Continuous Current		-	-	-1.9	A	1

Note:

1. The power dissipation is limited by 150°C junction temperature.

2. Device mounted on a glass-epoxy board



FR-4

25.4 × 25.4 mm .

2 Oz Copper

Test Board

3. The data tested by pulsed , pulse width ≦ 300μs , duty cycle ≦ 2%

4. Thermal Resistance follow JESD51-3.

Typical Characteristic Curves

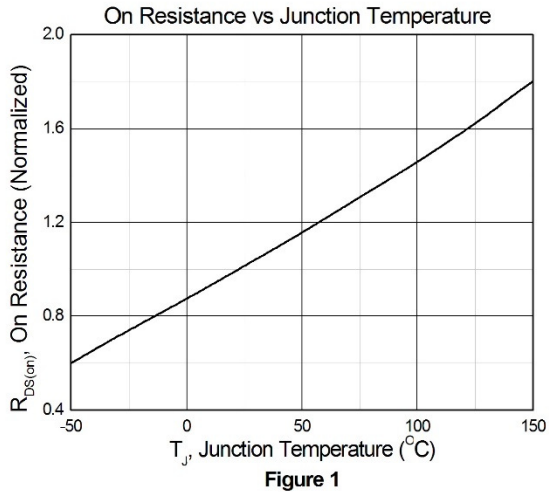


Figure 1

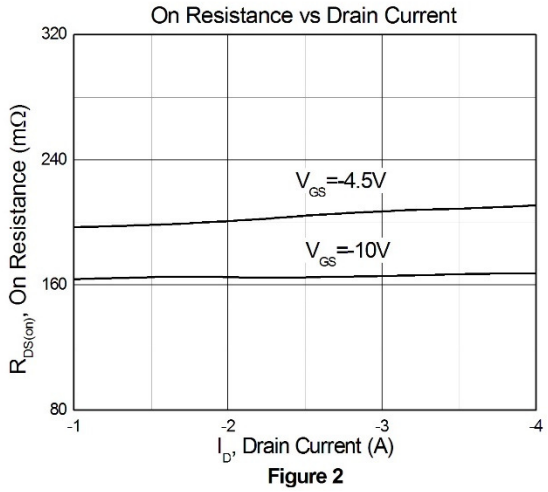


Figure 2

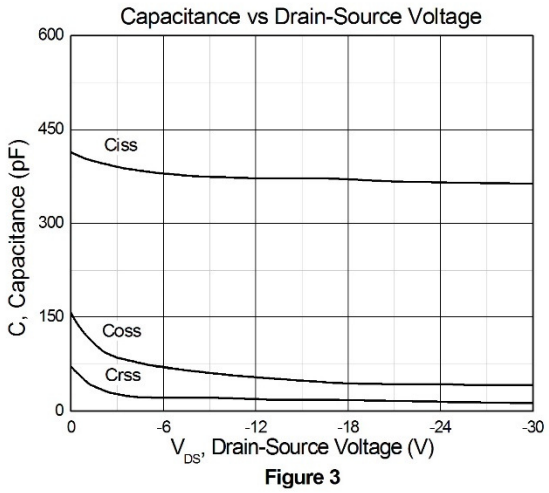


Figure 3

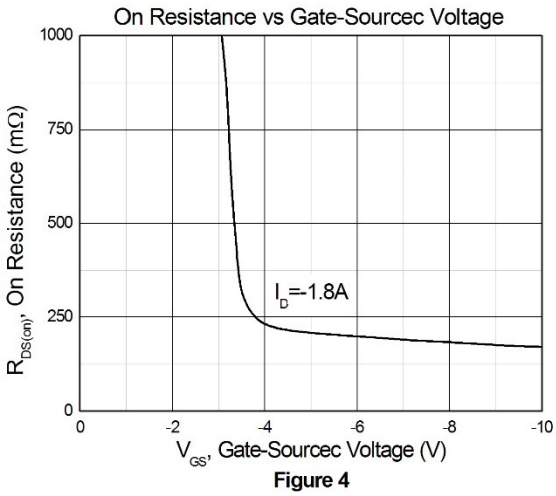


Figure 4

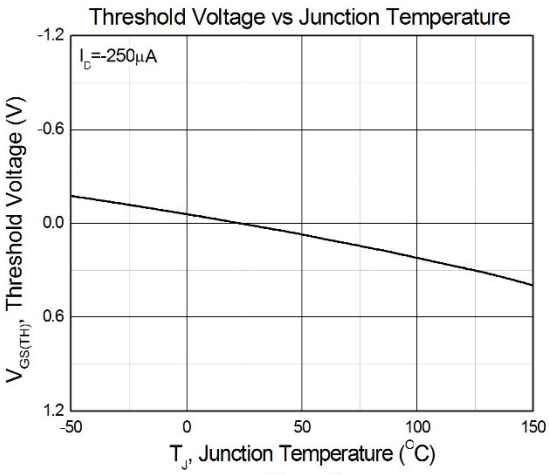


Figure 5

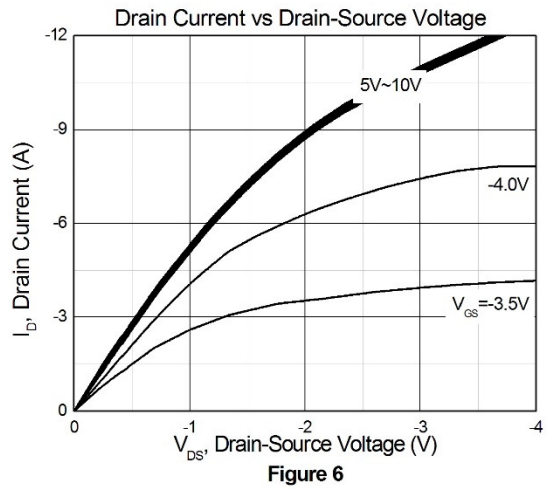


Figure 6

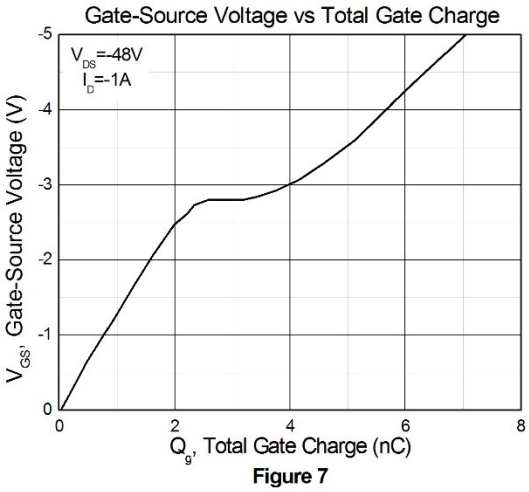


Figure 7

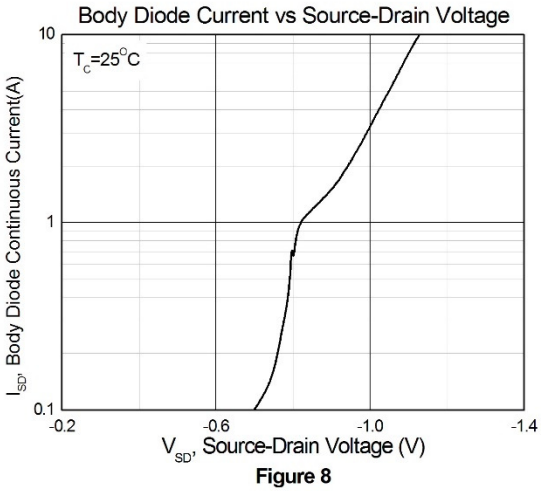


Figure 8

Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

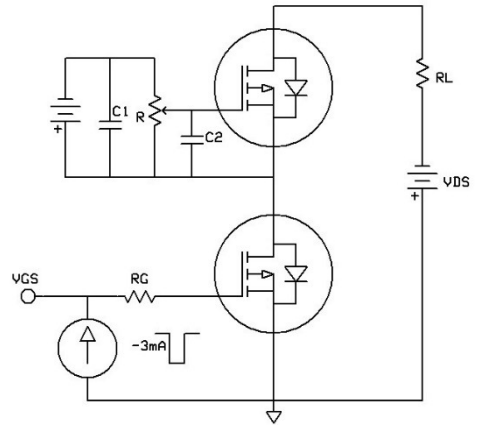


Figure 10: Gate Charge Waveform

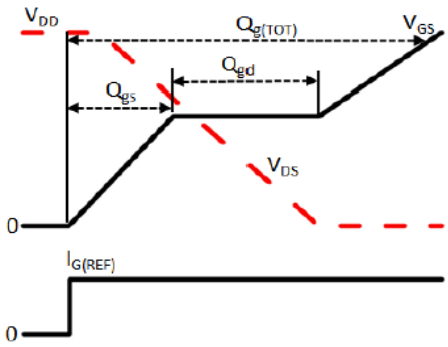


Figure 11: Switching Time Test Circuit

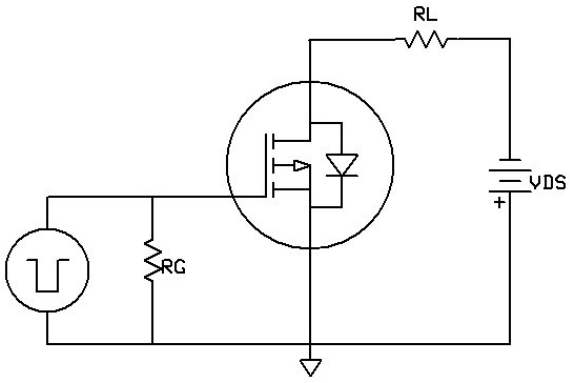
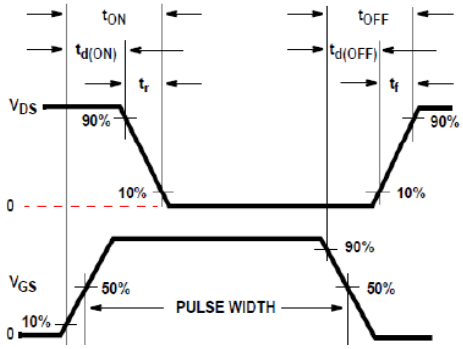
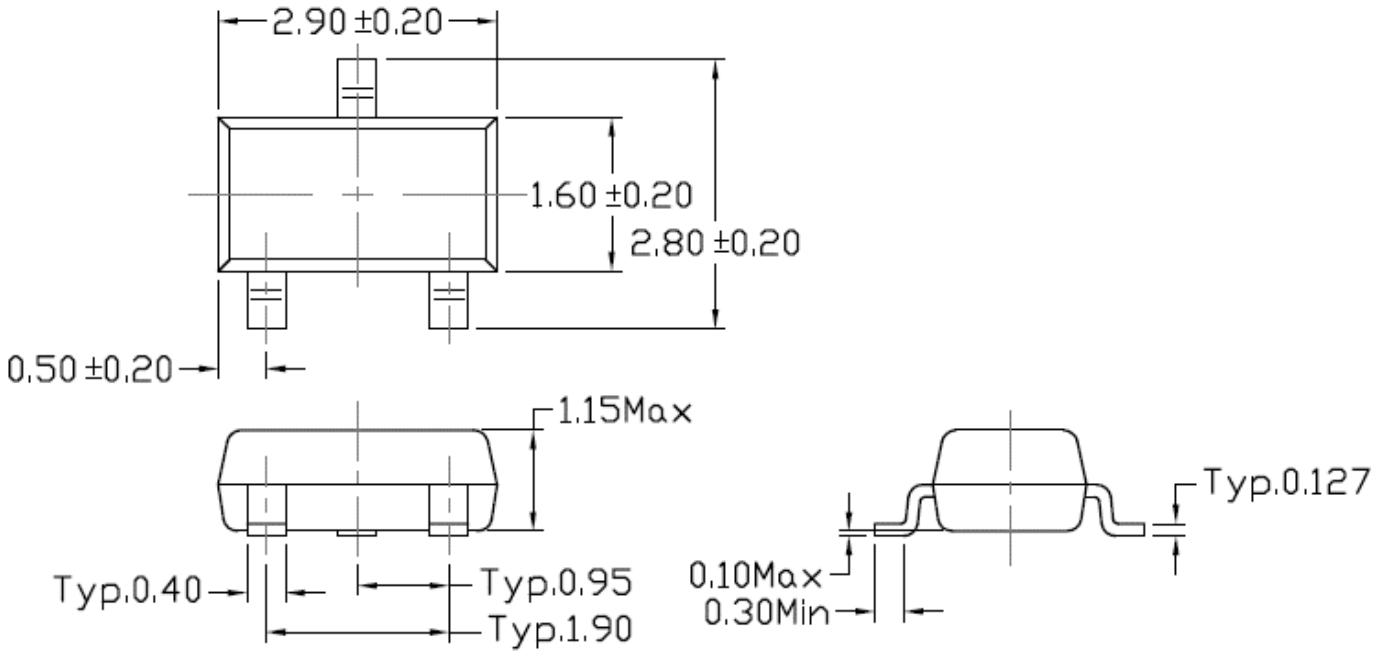


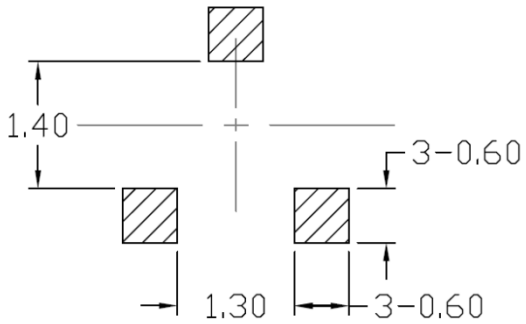
Figure 12: Switching Time Waveform



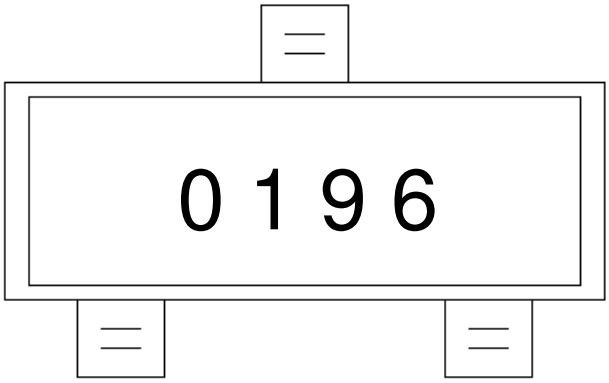
Package Dimension (SC-59)



Recommended pad layout for surface mount leadform



Marking Information

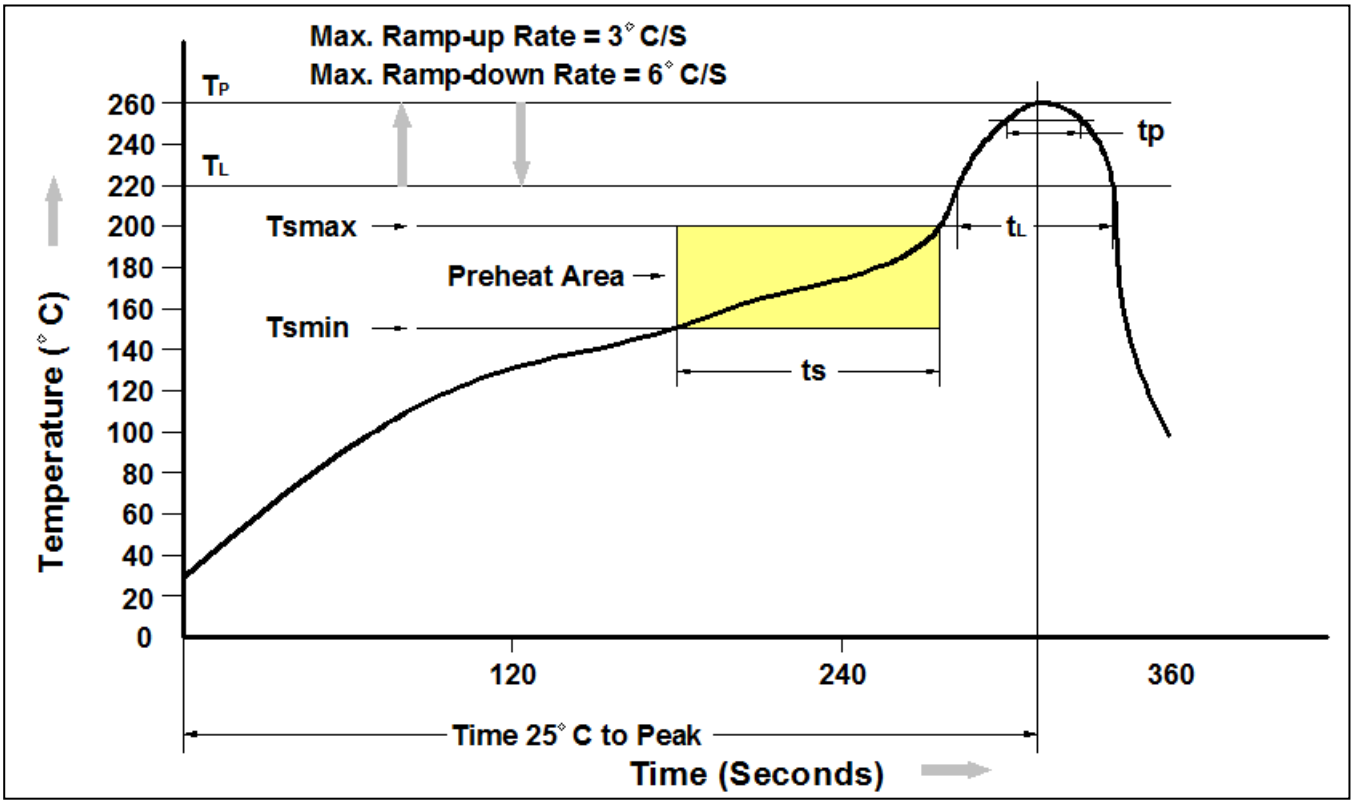


0196: Device Number

Ordering Information

Part Number	*Description*	*Quantity*
CTL0196PS-R3	SC-59 Reel	3000 pcs

Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150℃
Temperature Max. (Tsmax)	200℃
Time (ts) from (Tsmin to Tsmax)	60-120 seconds
Ramp-up Rate (t_L to t_P)	3℃/second max.
Liquidous Temperature (T_L)	217℃
Time (t_L) Maintained Above (T_L)	60 – 150 seconds
Peak Body Package Temperature	260℃ +0℃ / -5℃
Time (t_P) within 5℃ of 260℃	30 seconds
Ramp-down Rate (T_P to T_L)	6℃/second max
Time 25℃ to Peak Temperature	8 minutes max.

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