CTL505NS10-T52

N-Channel Enhancement MOSFET

Features

- Drain-Source Breakdown Voltage V_{DSS} 100V
- Drain-Source On-Resistance
  $R_{DS(ON)}$ 14mΩ, *at* V_{GS}*= 10V,* I_D*= 25A*
- *Continuous D*rain Current at T_C=25˚C I_D *=50.5A*
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

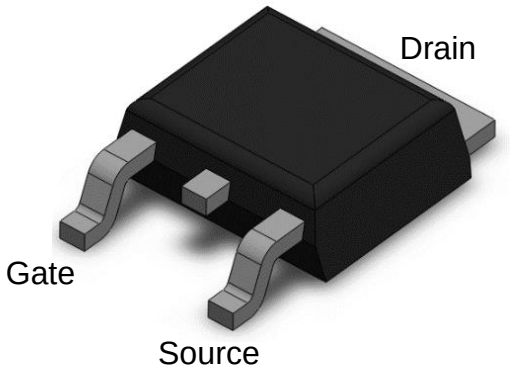
Description

The CTL505NS10-T52 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application.

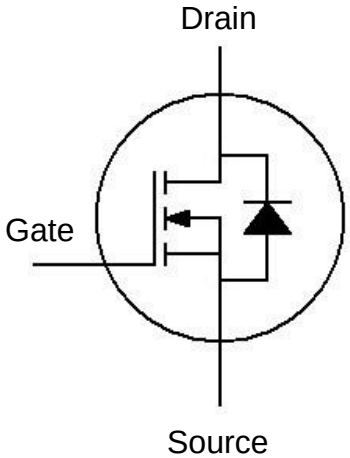
Applications

- DC/DC Converter
- Load Switch
- Power Management

Package Outline



Schematic



Absolute Maximum Rating at 25ºC

Symbol	Parameters	Test Conditions	Min	Note
V_{DS}	Drain-Source Voltage	100	V	
V_{GS}	Gate-Source Voltage	±20	V	
I_D	Continuous Drain Current @T_C=25˚C	50.5	A	1
I_{DM}	Pulsed Drain Current	202	A	1
P_D	Total Power Dissipation @T_C=25˚C	69.4	W	2
T_{STG}	Storage Temperature Range	-55 to 150	°C	
T_J	Operating Junction Temperature Range	-55 to 150	°C	

Thermal Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{\theta JC}$	Thermal Resistance Junction-Case		--	--	1.8	ºC /W	1,4

Electrical Characteristics T_A = 25°C (unless otherwise specified)

Static Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS}= 0V, I_D= 250μA	100	-	-	V	
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 100V, V_{GS} = 0V	-	-	1	μA	
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA	

On Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS} = 10V, I_D = 25A	-	14	17	mΩ	3
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS} = V_{DS}, I_D =250μA	2.0	-	4.0	V	3

Dynamic Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
C_{ISS}	Input Capacitance	V_{GS} =0V,	-	6170	-	pF	
C_{OSS}	Output Capacitance	V_{DS} =15V	-	427	-		
C_{RSS}	Reverse Transfer Capacitance	f=1MHz	-	307	-		

Switching Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$T_{D(ON)}$	Turn-On Delay Time	V_{DS} = 50V ,	-	42.5	-	ns	
T_R	Rise Time	R_G = 2.5Ω ,	-	85.5	-		
$T_{D(OFF)}$	Turn-Off Delay Time	V_{GS} = 10V,	-	154	-		
T_F	Fall Time	R_L = 1.8Ω ,	-	25	-		
Q_G	Total Gate Charge	V_{DS} = 80V ,	-	28	-	nC	
Q_{GS}	Gate-Source Charge	V_{GS} = 4.5V ,	-	28.5	-		
Q_{GD}	Gate-Drain (Miller) Charge	I_D =28A ,	-	34.5	-		

Drain-Source Diode Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
V_{SD}	Body Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 1A	-	0.9	1.2	V	1
I_{SD}	Body Diode Continuous Current		-	-	1	A	1

Note:

1. The power dissipation is limited by 150°C junction temperature.
2. The data tested by pulsed , pulse width ≤ 300μs , duty cycle ≤ 2%
3. Thermal Resistance follow JESD51-3.

Typical Characteristic Curves

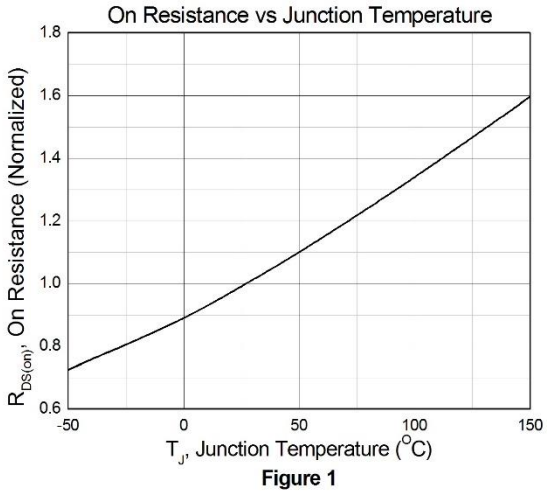


Figure 1

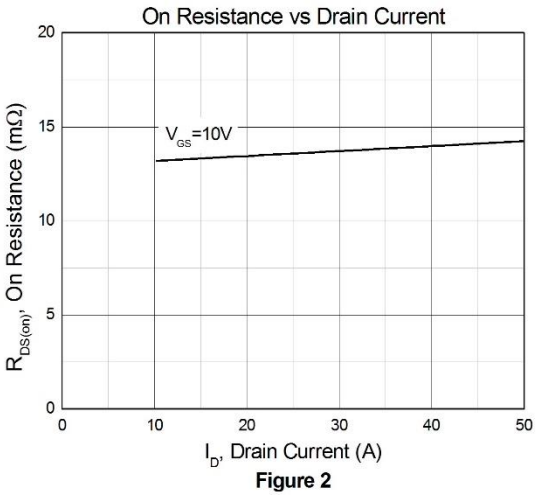


Figure 2

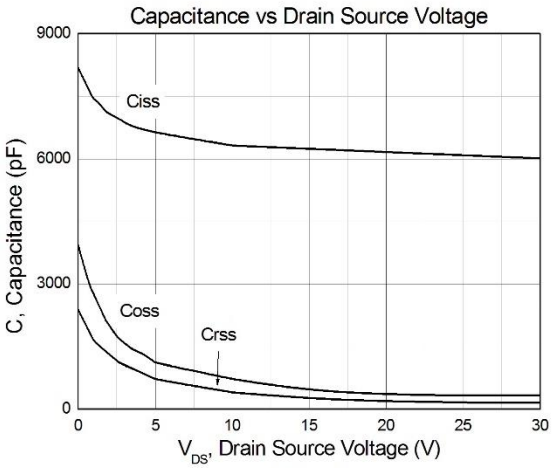


Figure 3

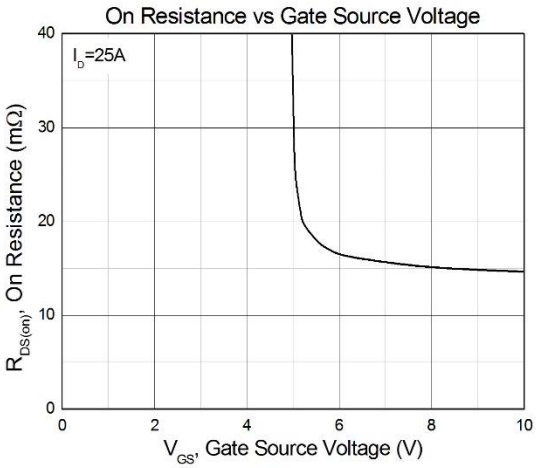


Figure 4

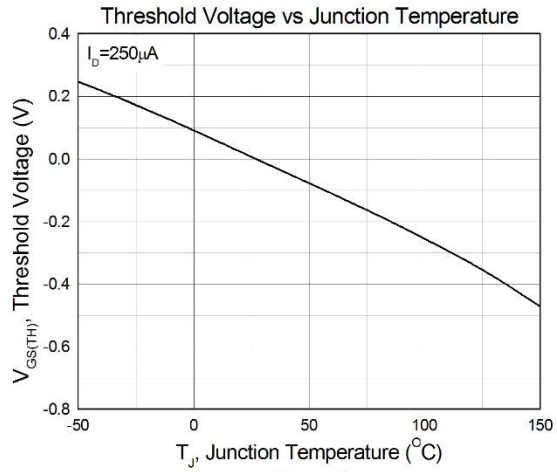


Figure 5

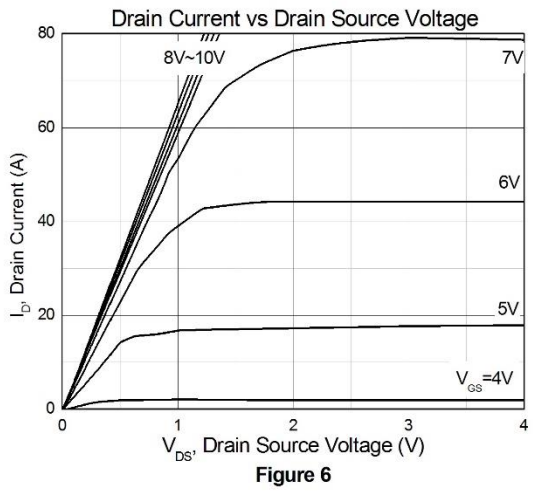


Figure 6

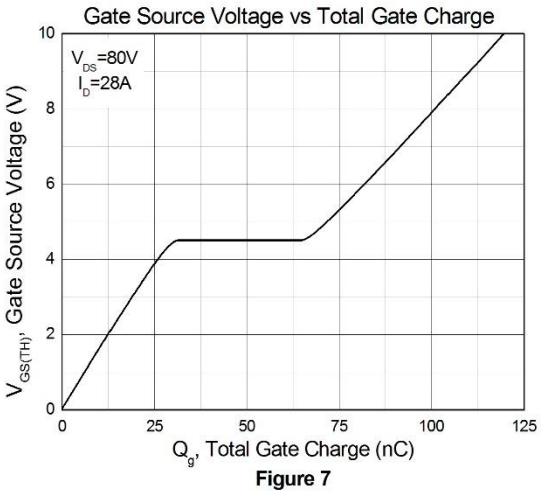


Figure 7

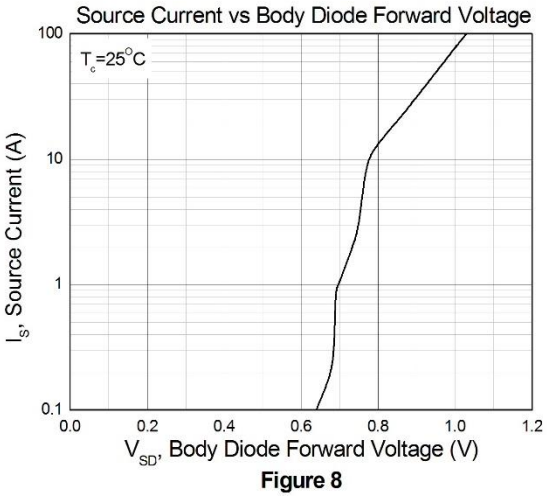


Figure 8

Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

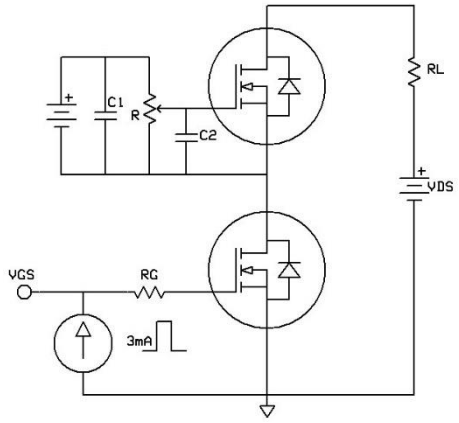


Figure 10: Gate Charge Waveform

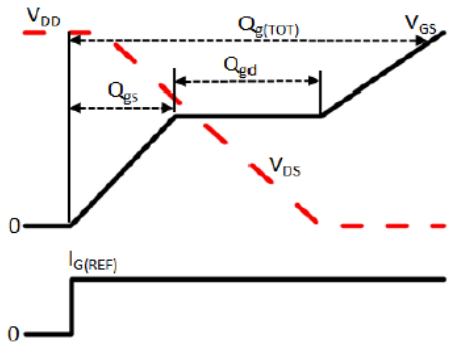


Figure 11: Switching Time Test Circuit

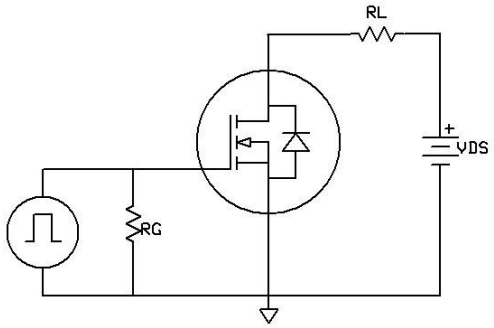
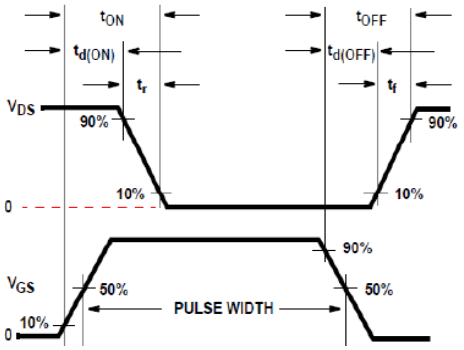
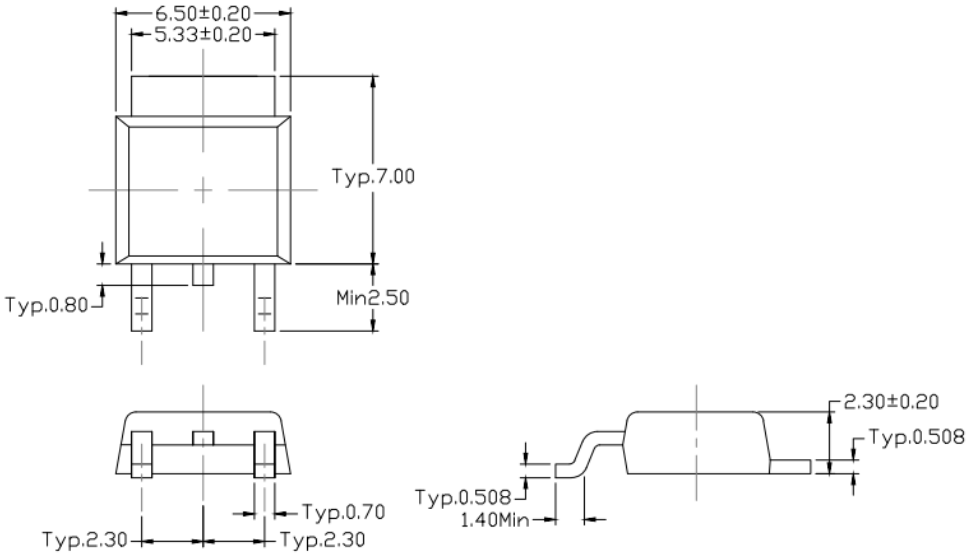


Figure 12: Switching Time Waveform

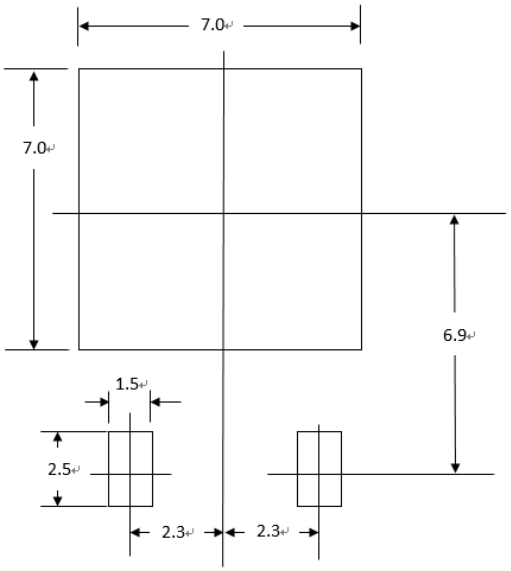


Package Dimension (TO-252)



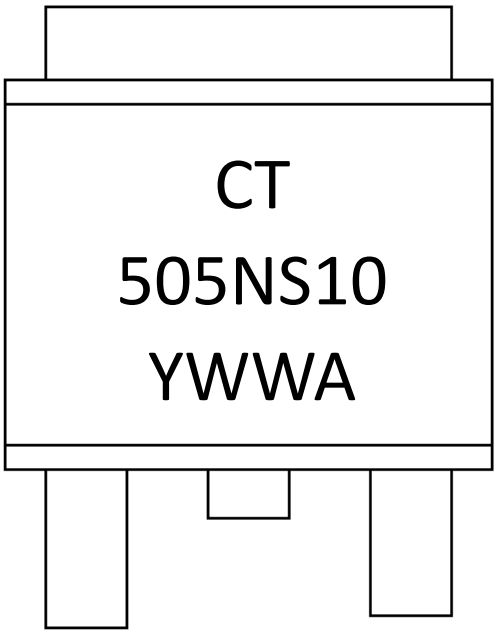
Dimensions in mm unless otherwise stated

Recommended pad layout for surface mount leadform



Dimensions in mm unless otherwise stated

Marking Information

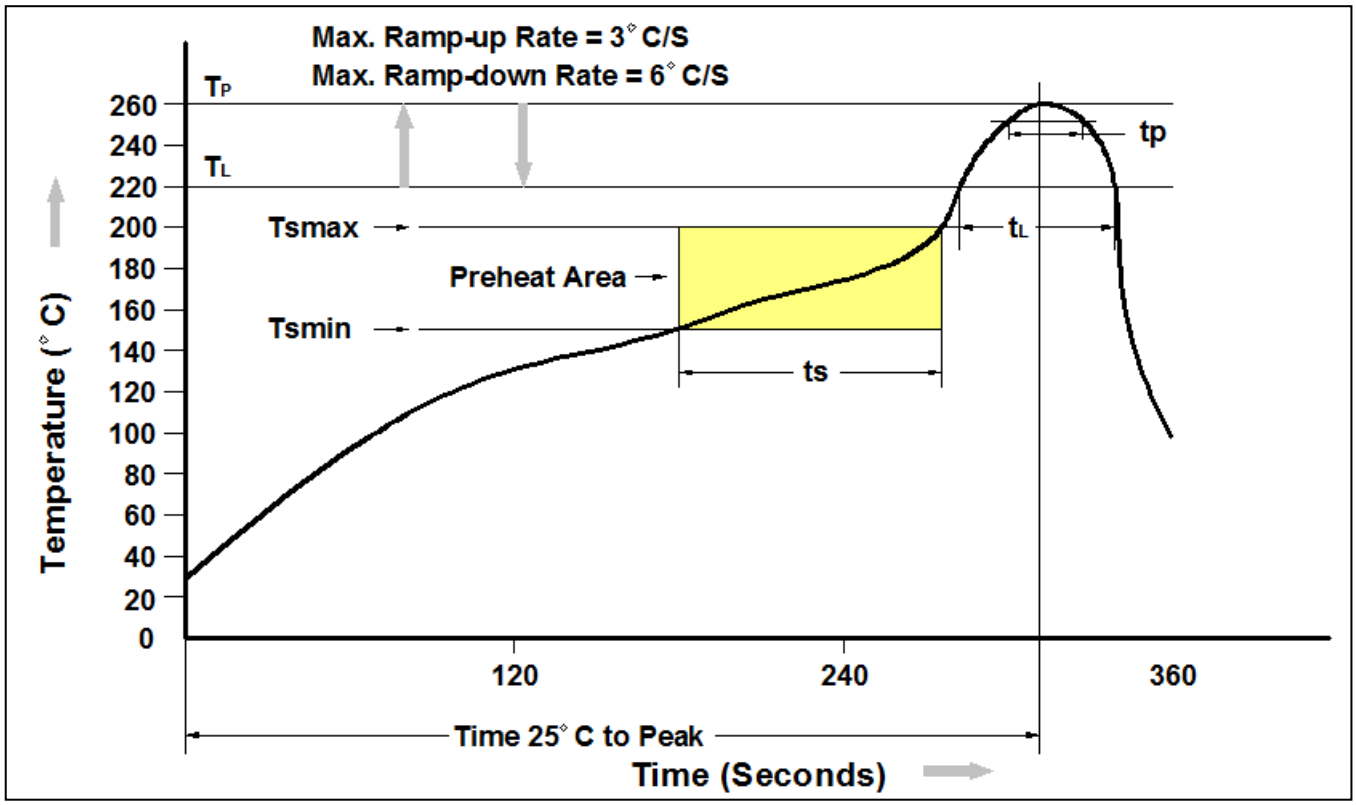


CT	：Denotes “ CT Micro”
505NS10	：Device Number
Y	：Fiscal Year
WW	：Work Week
A	：Production Code

Ordering Information

Part Number	*Description*	*Quantity*
CTL505NS10-T52	TO-252 Reel	2500 pcs

Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (ts) from (Tsmin to Tsmax)	60-120 seconds
Ramp-up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 – 150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second max
Time 25°C to Peak Temperature	8 minutes max.

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